

FIG. 1

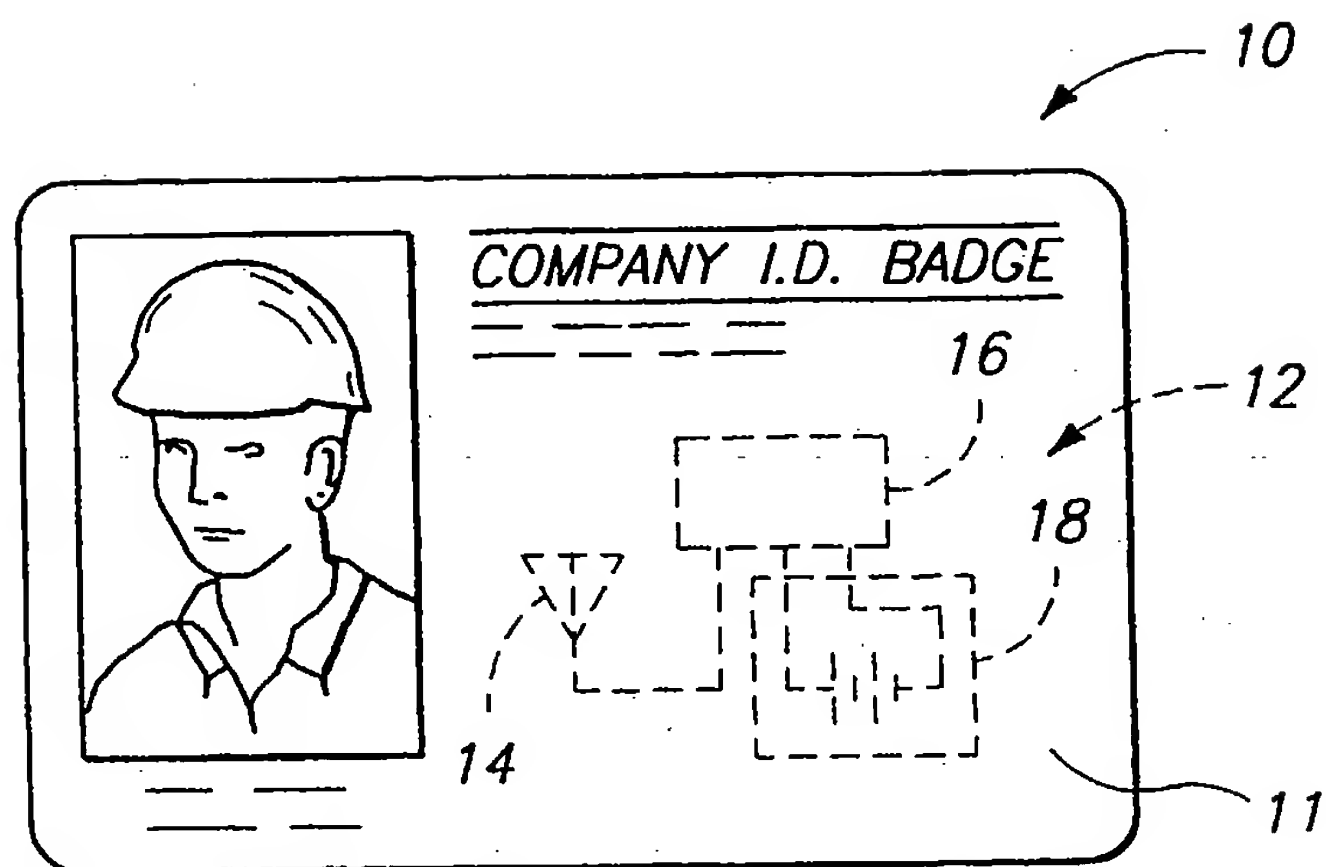


FIG. 2

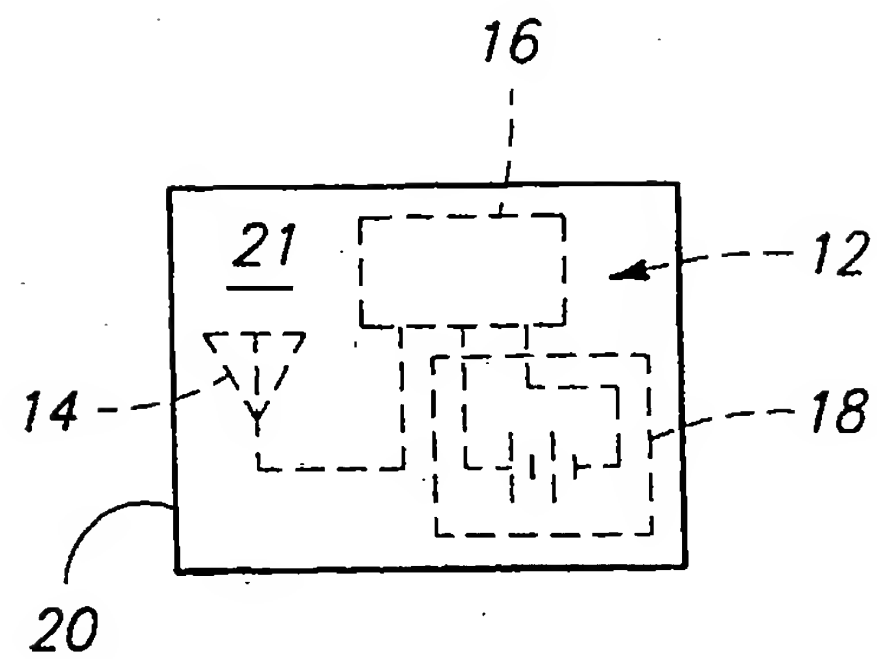


FIG. 1

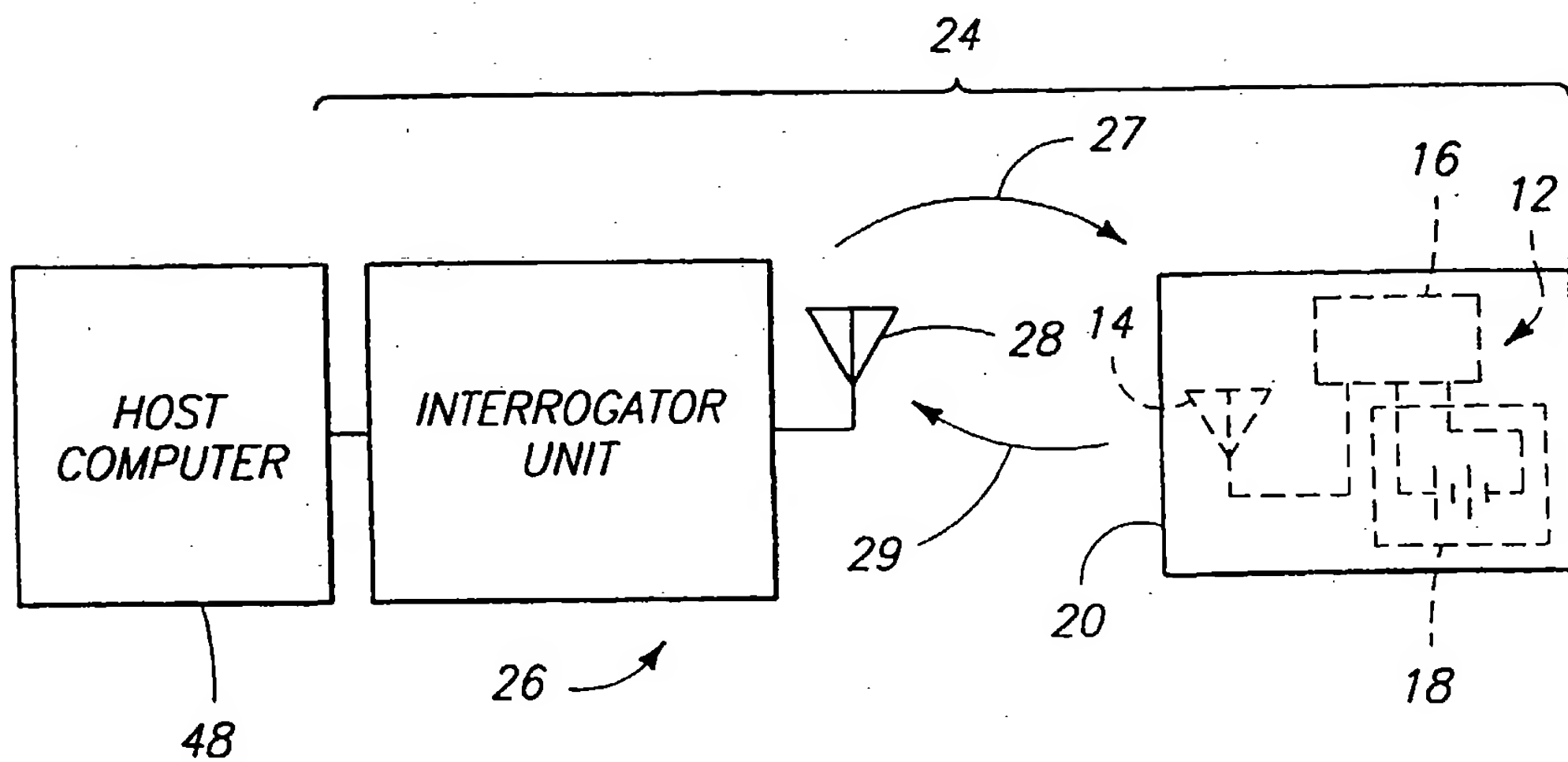


FIG. 2

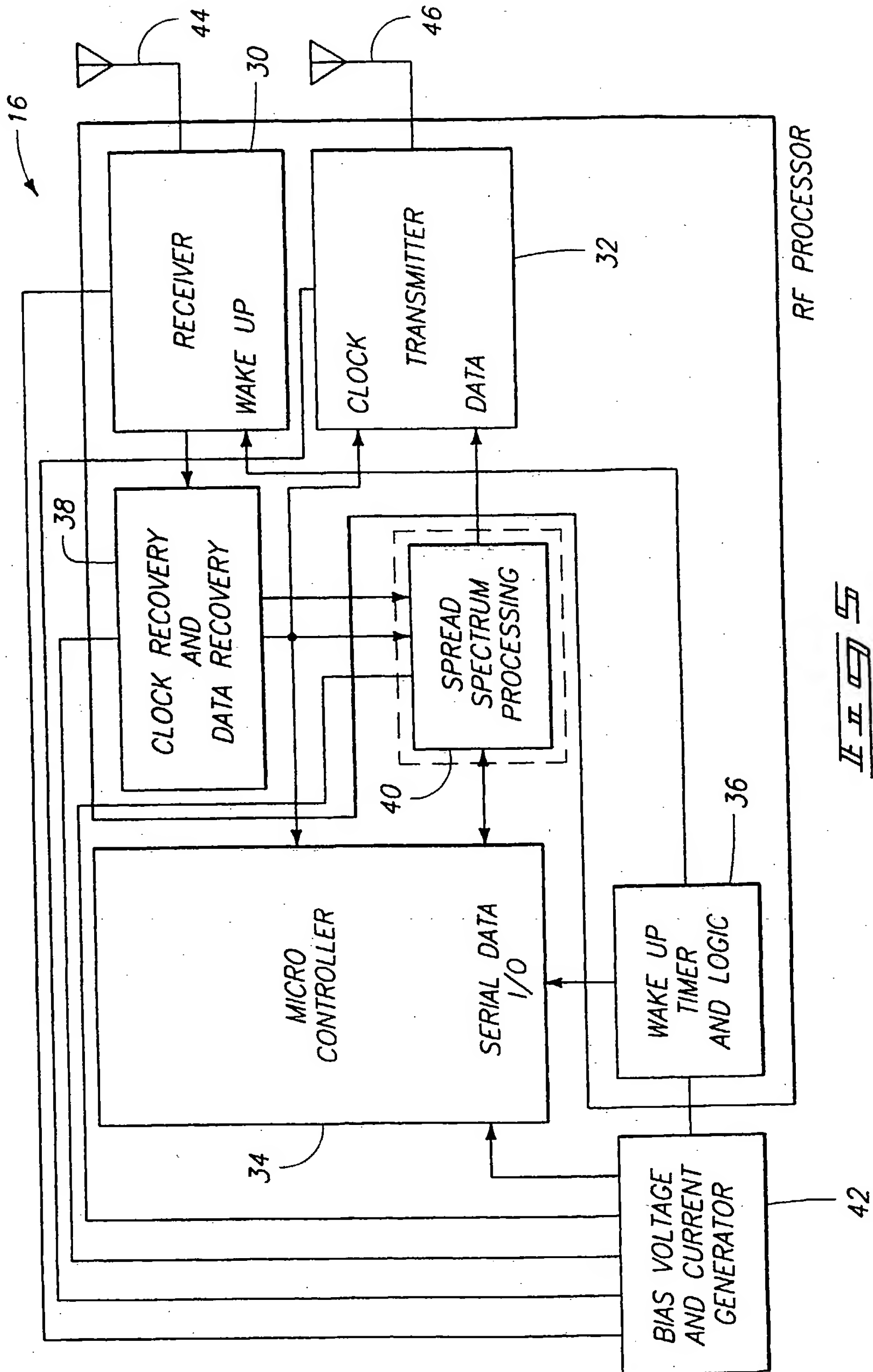


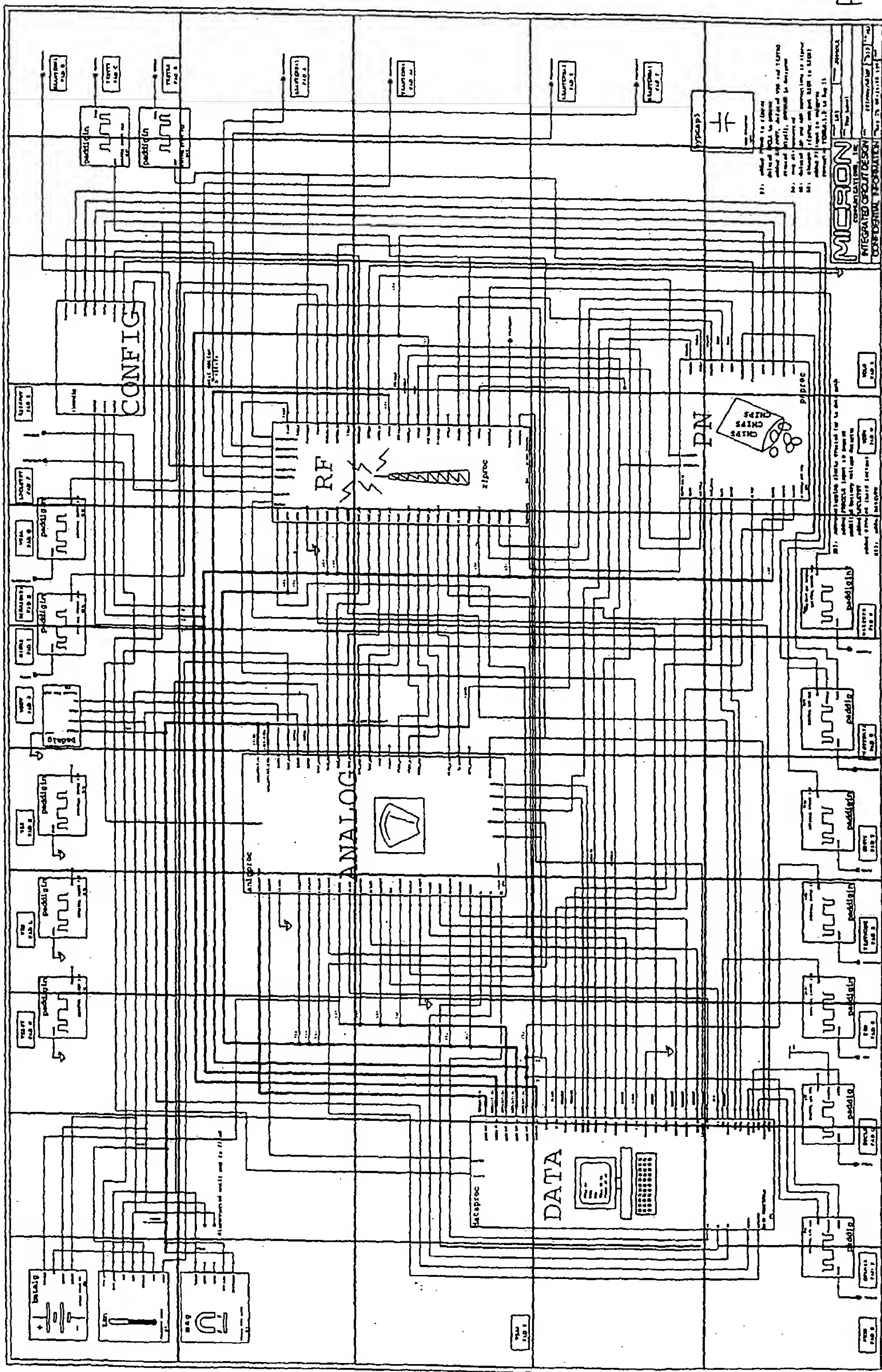
FIG. 5

6AA	6AB	6AC	6AD	6AE	6AF	6AG	6AH	6AI	6AJ	6AK
6BA	6BB	6BC	6BD	6BE	6BF	6BG	6BH	6BI	6BJ	6BK
6CA	6CB	6CC	6CD	6CE	6CF	6CG	6CH	6CI	6CJ	6CK
6DA	6DB	6DC	6DD	6DE	6DF	6DG	6DH	6DI	6DJ	6DK
6EA	6EB	6EC	6ED	6EE	6EF	6EG	6EH	6EI	6EJ	6EK

II II II II



FIG. 6AA-EK



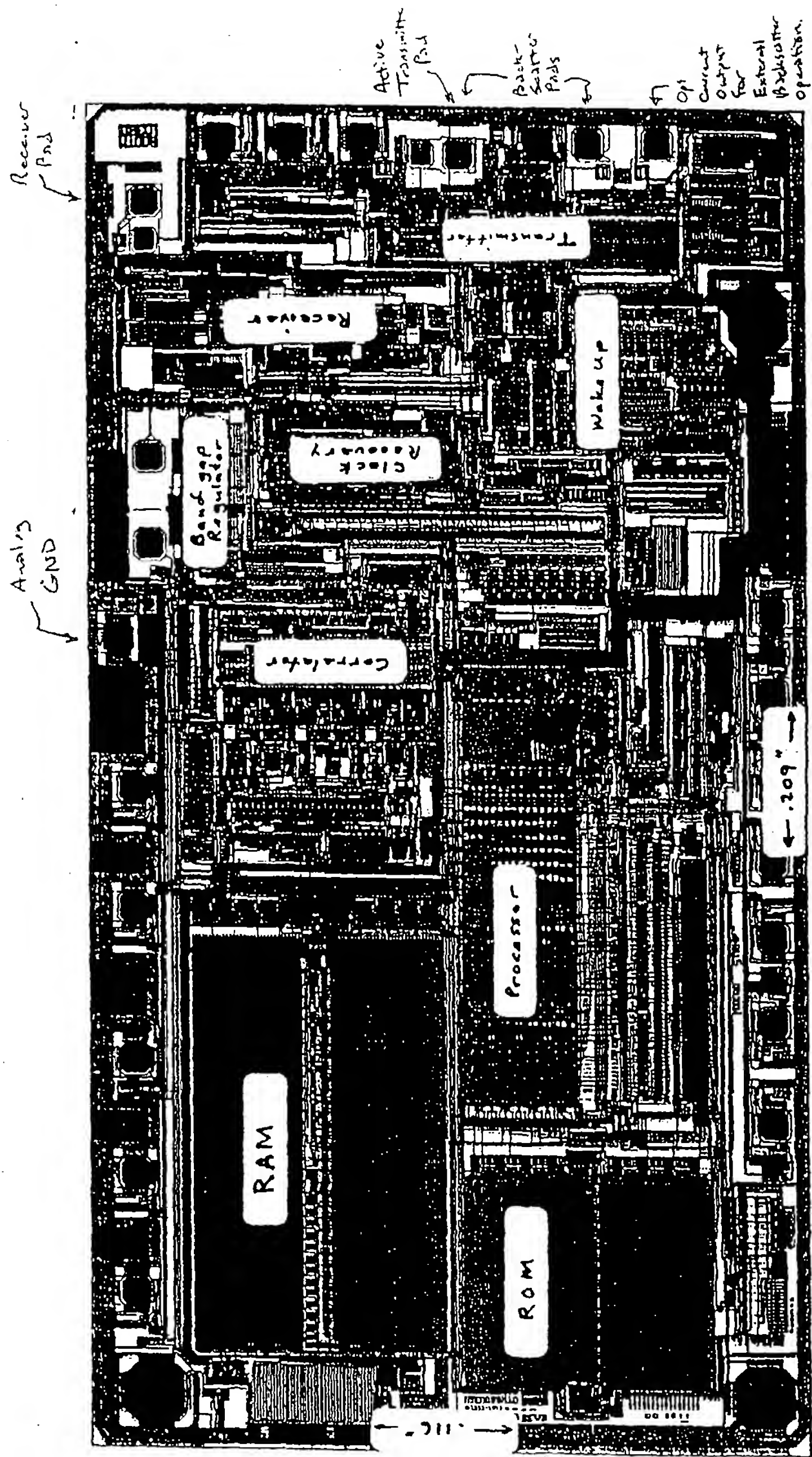
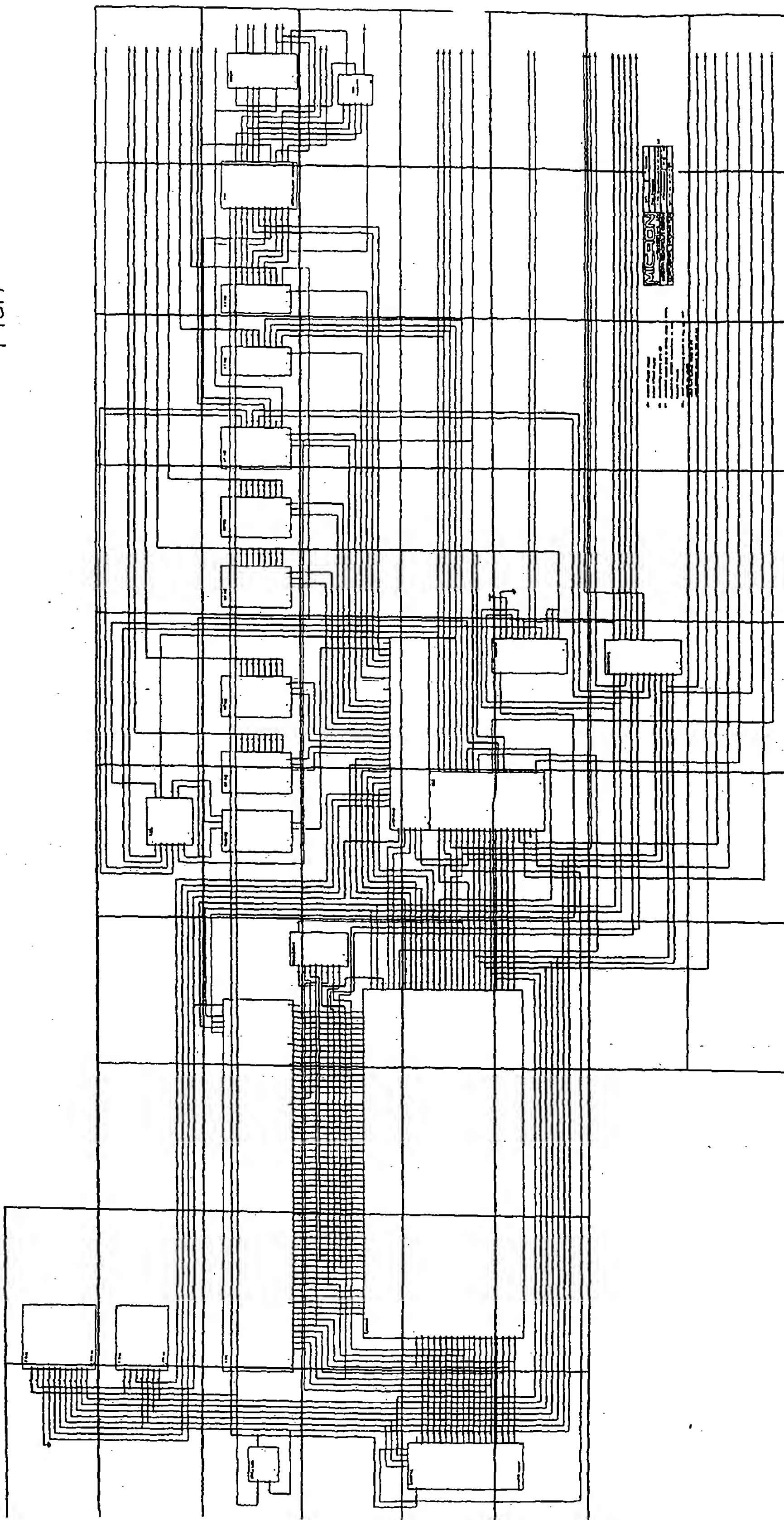


FIG. 6.01

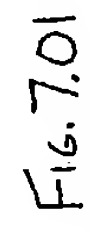


FIG. 7



7.01AA	7.01AB
7.01BA	7.01BB

II. II. II. II



**MICRON COMMUNICATIONS, INC.**  
INTEGRATED CIRCUIT DESIGN  
CONFIDENTIAL INFORMATION

PRODUCT: 1.03	DATE ISSUED: 06/20/2011
---------------	-------------------------

Processor Clock Generator	
---------------------------	--

2-Phase/4-State/8-Cycle

103 reva/clock	Rev. B11
----------------	----------

DATE: 2001-03-13 09:58:52 1996

7.0101AA	7.0101AB
7.0101BA	7.0101BB

IL 7.0101BB

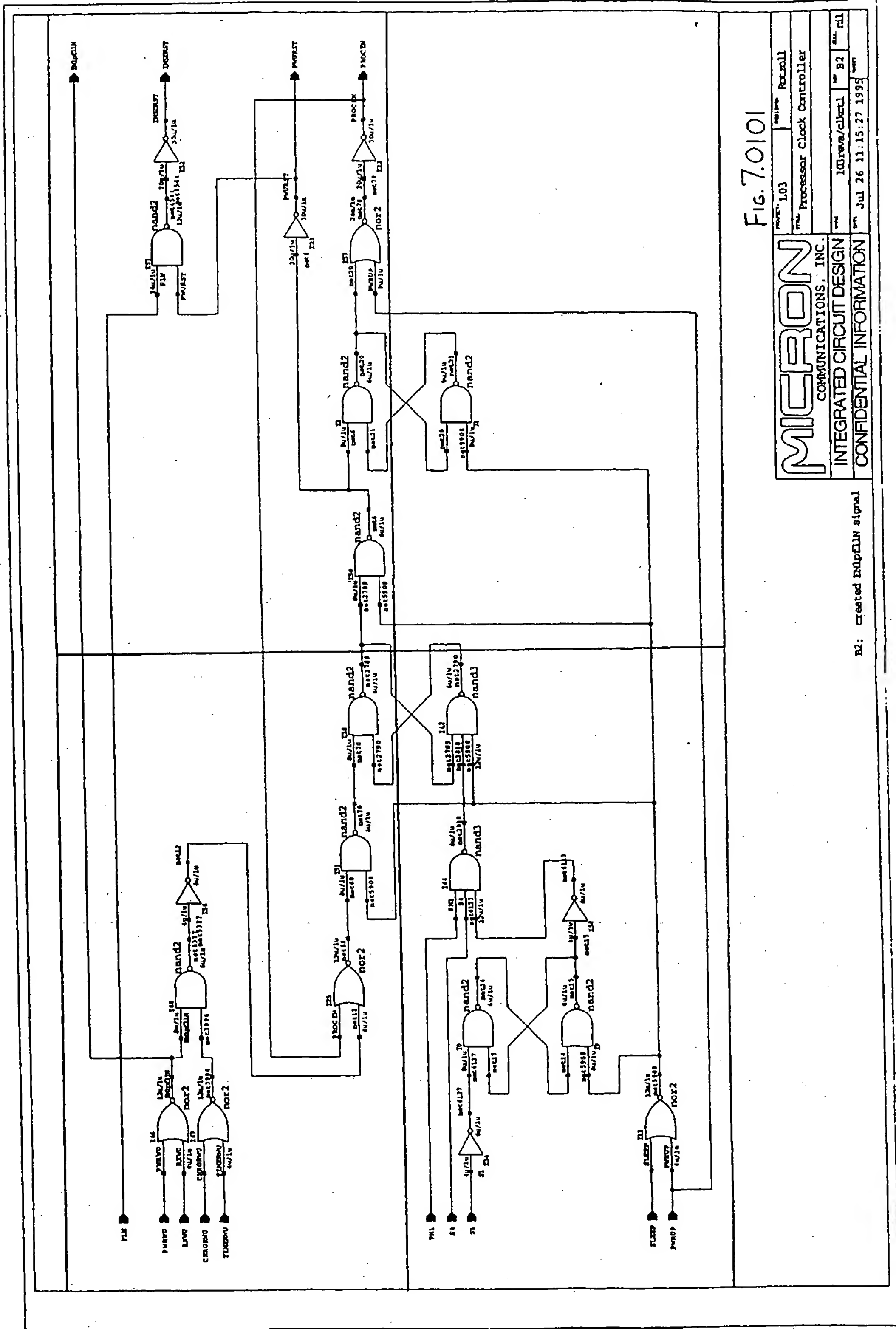


Fig. 7.0101

MICRON		PROJECT L03	REVISION R0001
COMMUNICATIONS, INC.		PROCESSOR Clock Controller	
INTEGRATED CIRCUIT DESIGN		DATE 10/19/94/01/01	BY B2
CONFIDENTIAL INFORMATION		DATE Jul 26 11:15:27 1995	BY B2

B2: created EXPFLIN signal



7.0102BA	7.0102BB	7.0102BC	7.0102BD	7.0102BE	7.0102BF	7.0102AG	7.0102AH	7.0102AI	7.0102AJ
7.0102CA	7.0102CB	7.0102CC	7.0102CD	7.0102CE	7.0102CF	7.0102CG	7.0102CH	7.0102CI	7.0102CJ
7.0102DA	7.0102DB	7.0102DC	7.0102DD	7.0102DE	7.0102DF	7.0102DG	7.0102DH	7.0102DI	7.0102DJ

2007.11.11

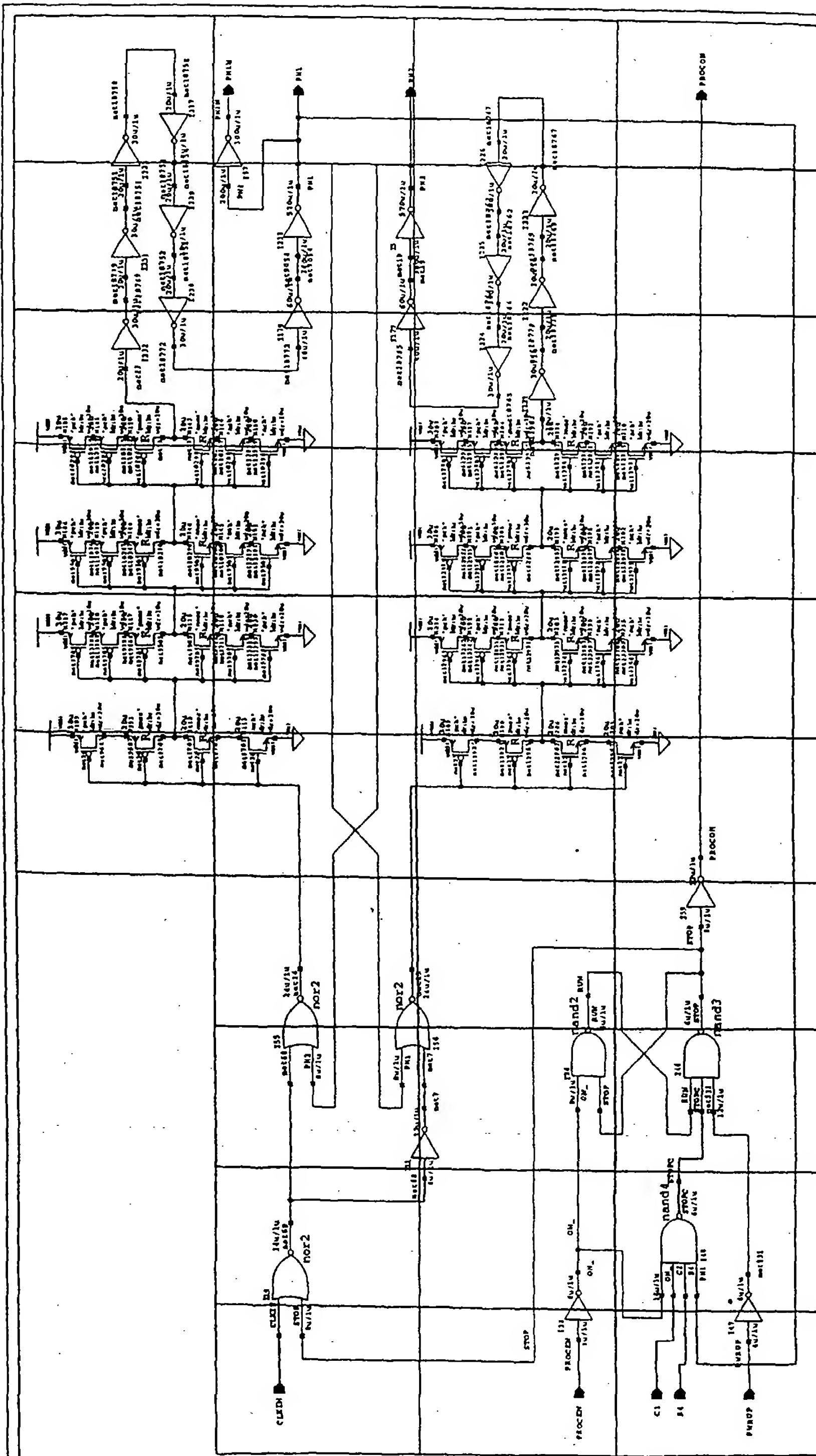


Fig. 7.0102

B2: Pin name changes

B8: Added 6 inverters to non-overlap time

Make the number of inverters adjustable on metal

<b>MICRON</b>		Version: R02011
COMMUNICATIONS, INC.		Processor Phase Generator
INTEGRATED CIRCUIT DESIGN		2-Phase Non-overlapping
CONFIDENTIAL INFORMATION		Rev. B8
		Dec 5 17:55:56 1995

7.0103AA	7.0103AB	7.0103AC	7.0103AD
7.0103BA	7.0103BB	7.0103BC	7.0103BD

SECRET

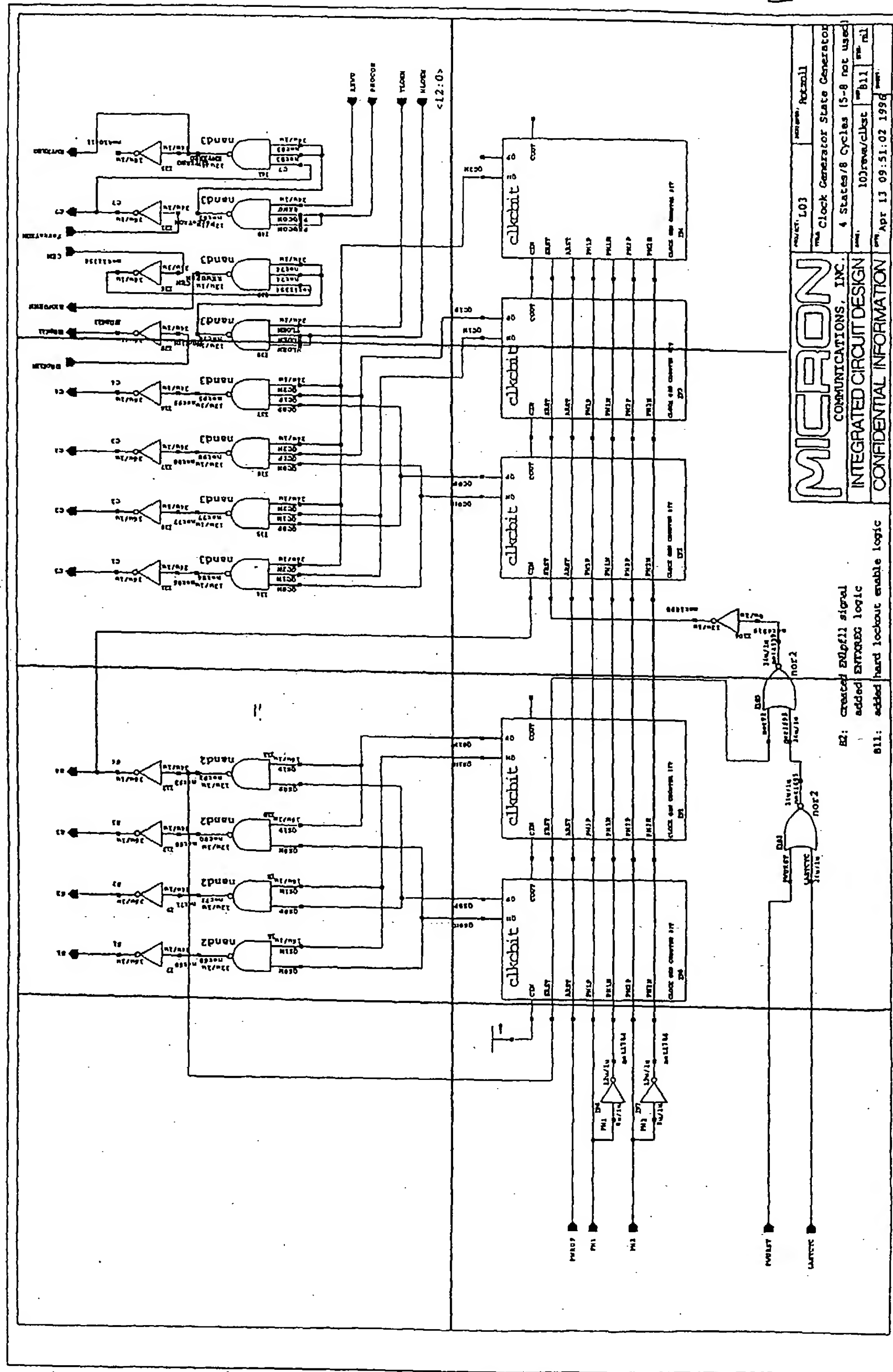
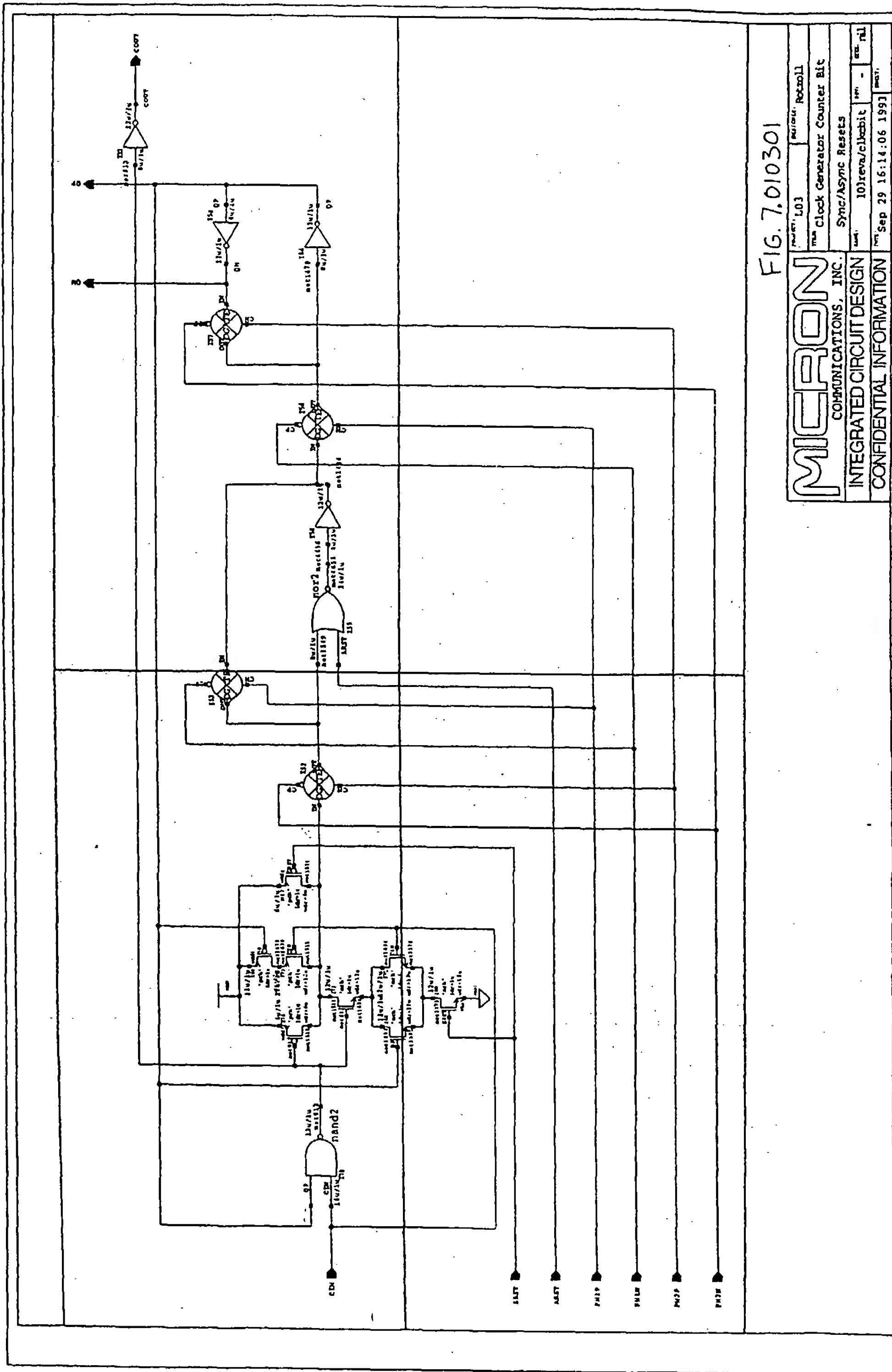


Fig. 7.0103





7.02AA	7.02AB	7.02AC	7.02AD	7.02AE	7.02AF
7.02BA	7.02BB	7.02BC	7.02BD	7.02BE	7.02BF

II II II II II II

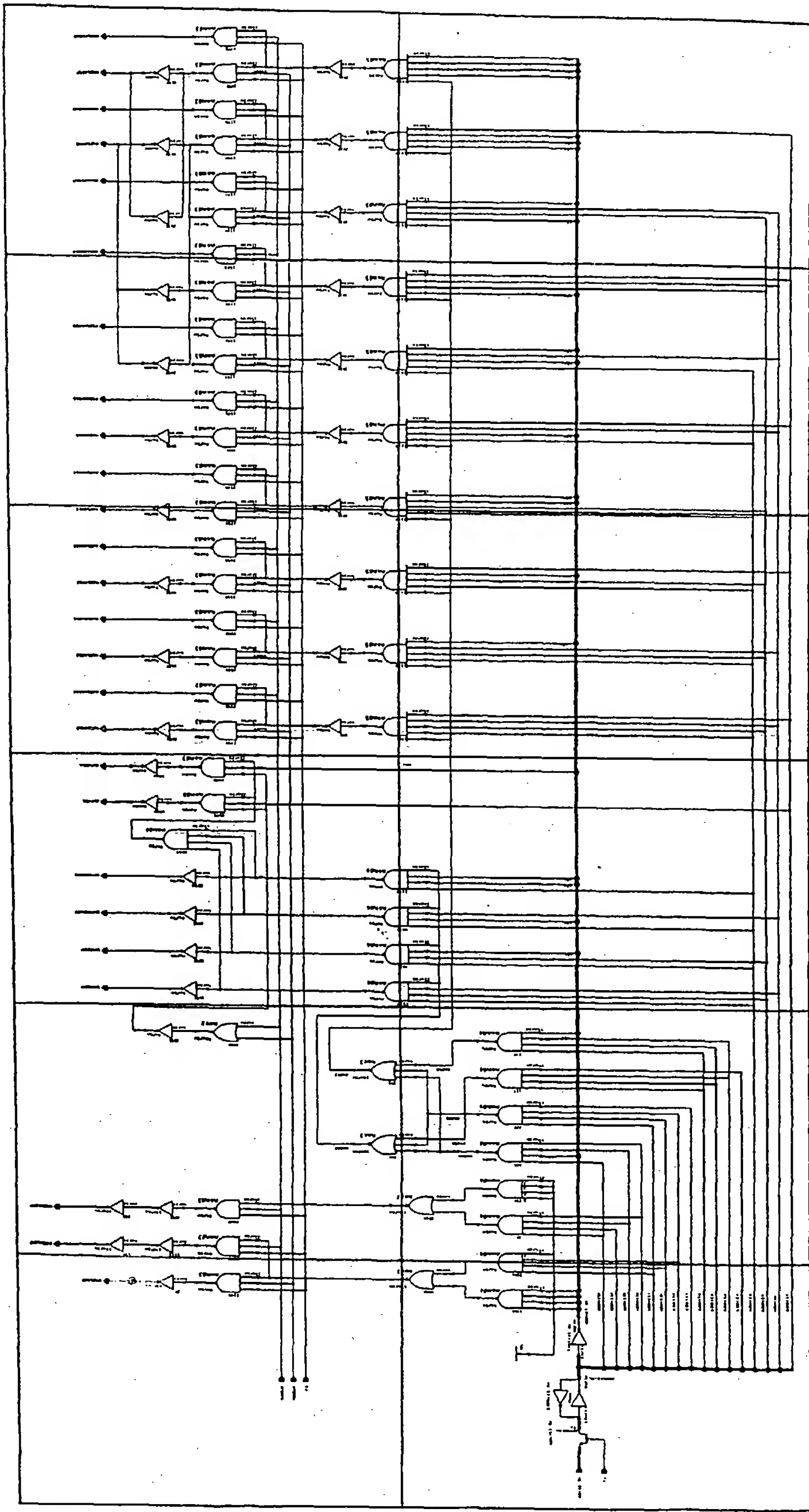


FIG. 7.02

<b>MICRON</b>	
INTEGRATED CIRCUIT DESIGN	ADDRESS: BOSTON, MASS.
CONFIDENTIAL INFORMATION	DATE: 11-11-66

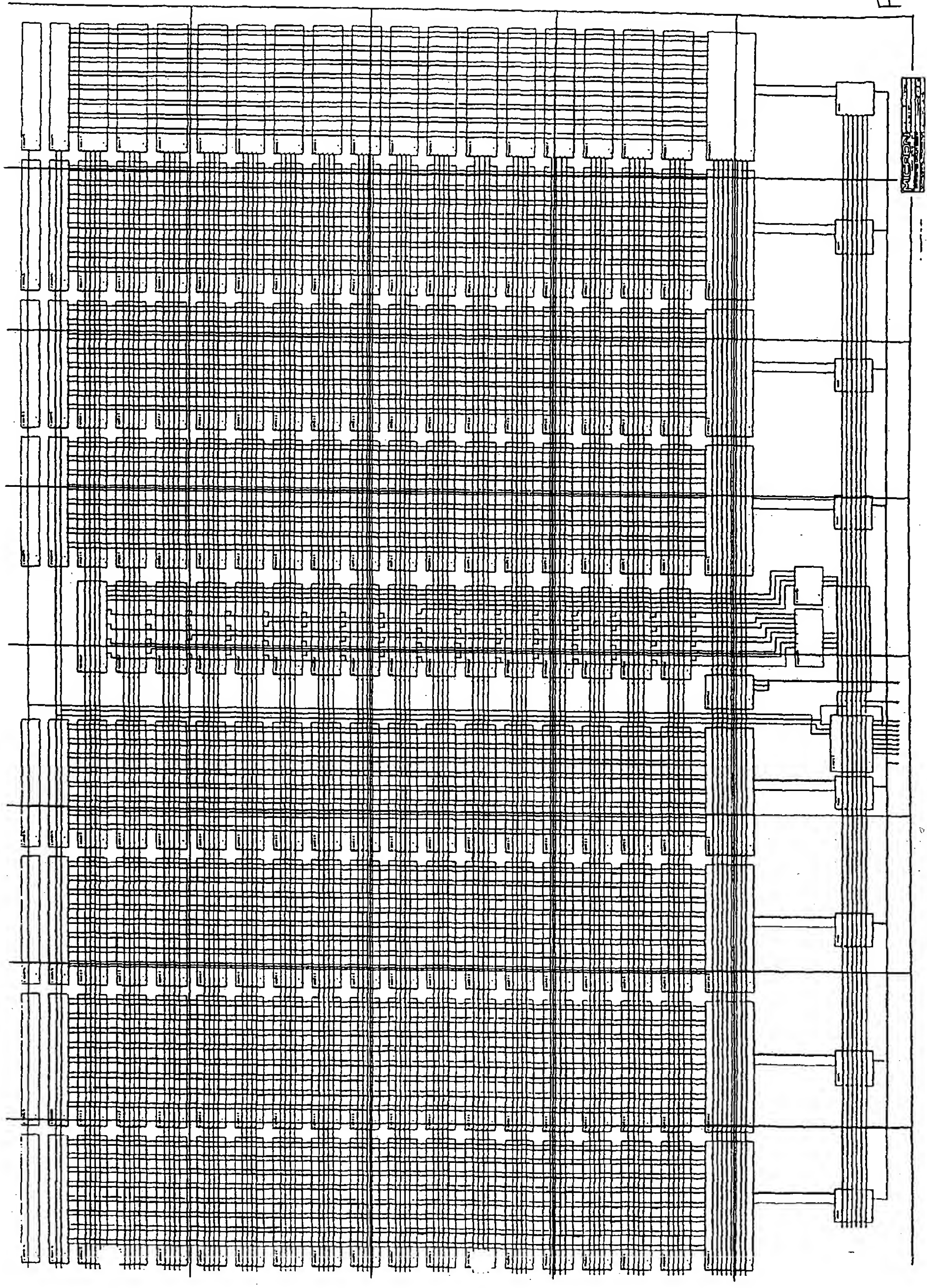
24. Integrated drive at MICRON and MICRON



7.03AA	7.03AB	7.03AC	7.03AD	7.03AE	7.03AF	7.03AG	7.03AH
7.03BA	7.03BB	7.03BC	7.03BD	7.03BE	7.03BF	7.03BG	7.03BH
7.03CA	7.03CB	7.03CC	7.03CD	7.03CE	7.03CF	7.03CG	7.03CH
7.03DA	7.03DB	7.03DC	7.03DD	7.03DE	7.03DF	7.03DG	7.03DH
7.03EA	7.03EB	7.03EC	7.03ED	7.03EE	7.03EF	7.03EG	7.03EH

IL 11 00 00 00 00 00

Fig 7.03



7.0301AA	7.0301AB
7.0301BA	7.0301BB

ITEM 7.0301

RAM CTL

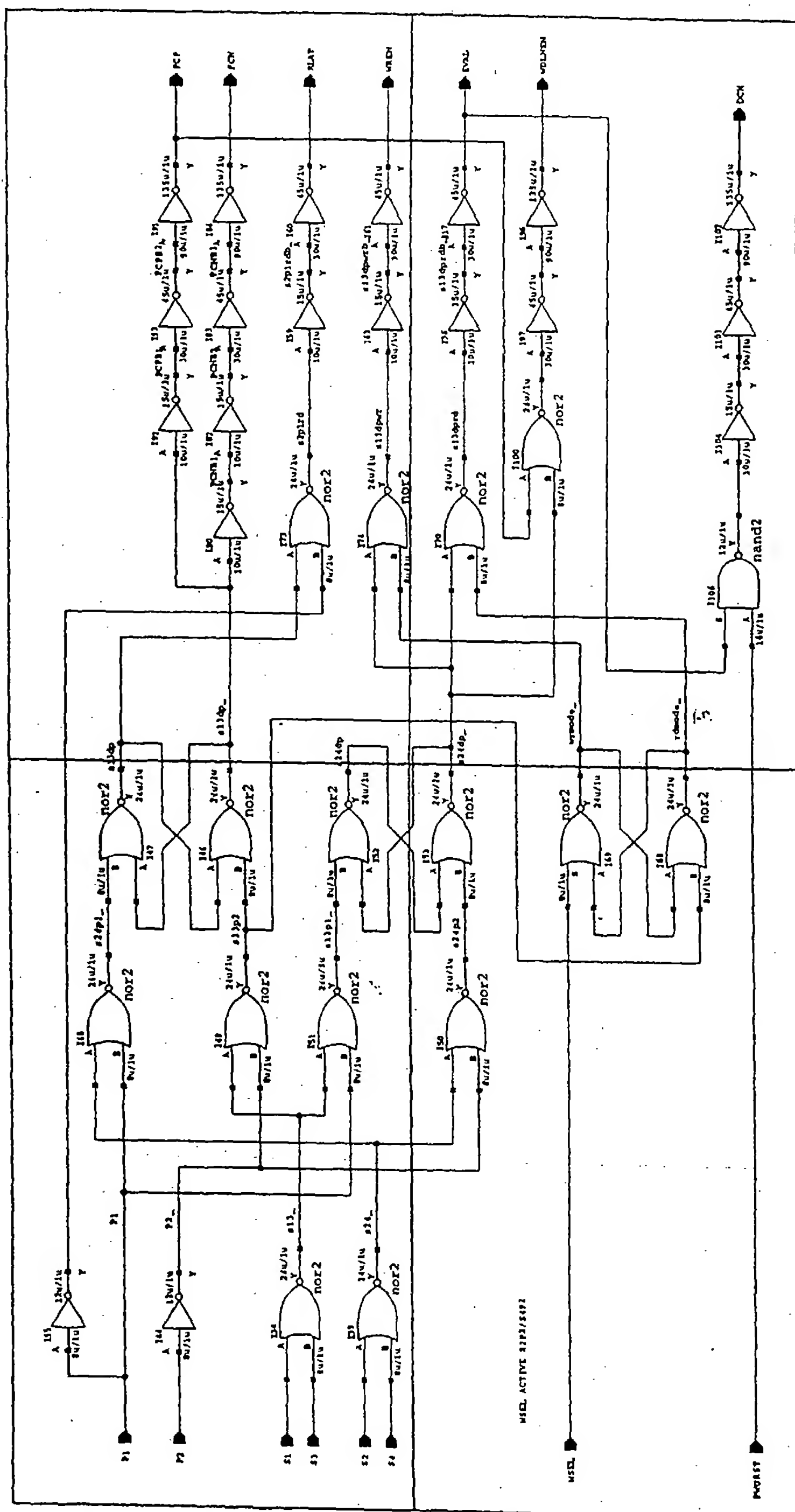


FIG. 7.0301

MICRON		DESIGN L03 Ad3	DESIGN: Rotzoll
COMMUNICATIONS, INC.		RAM CONTROL	
INTEGRATED CIRCUIT DESIGN		REV: 103revs/ramctl	REV: ml
CONFIDENTIAL INFORMATION		DATE: Feb 11 16:47:36 1994	

7.0302AA	7.0302AB	7.0302AC
----------	----------	----------

EX-100-100-100-100

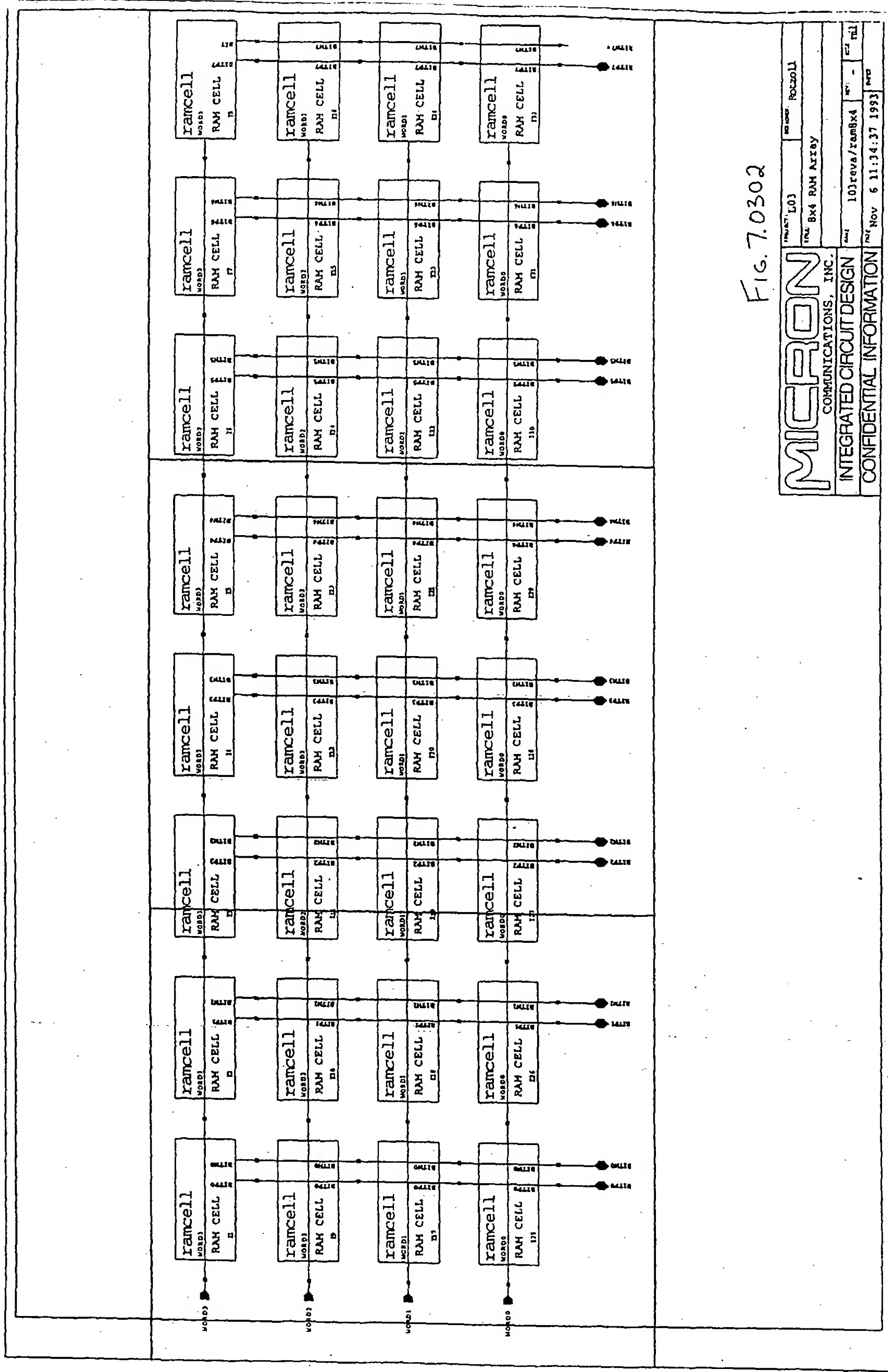


Fig. 7.0302

<b>MICRON</b> COMMUNICATIONS, INC.		PART NO. 70302	REV. 1
		TYPE BX4 RAM ARRAY	DATE 10/19/84
INTEGRATED CIRCUIT DESIGN		101 rev A / ram BX4	101
CONFIDENTIAL INFORMATION		DATE NOV 6 11:34:37 1993	BY

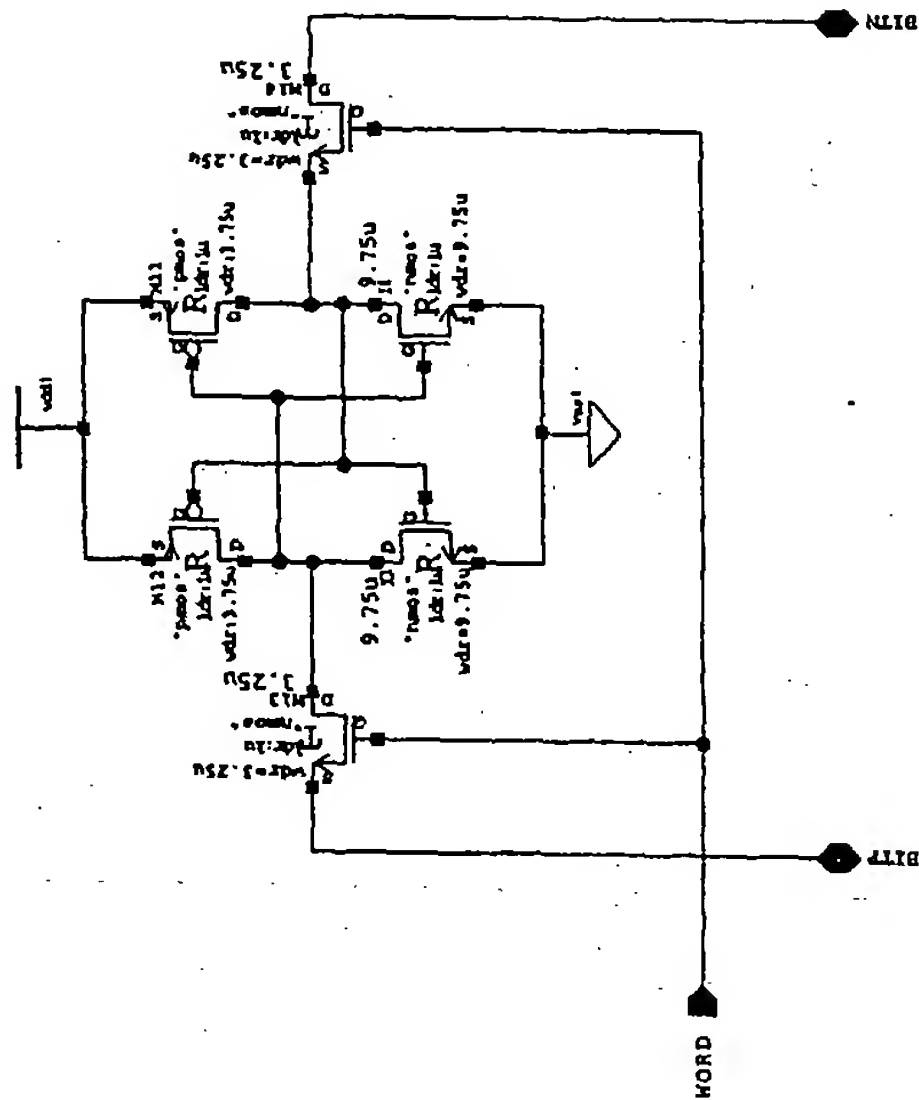


Fig. 7.030201

MICRON		PROJECT: L03	DESIGNER: Rotzoll
COMMUNICATIONS, INC.		TITLE: 6T RAM Cell	
INTEGRATED CIRCUIT DESIGN		NAME: 103reva/rancell	REV: -
CONFIDENTIAL INFORMATION		DATE: Nov 6 11:34:48 1993	SHEET: A

MI40-030

7.0303AA	7.0303AB	7.0303AC	7.0303AD
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MEMPHIS



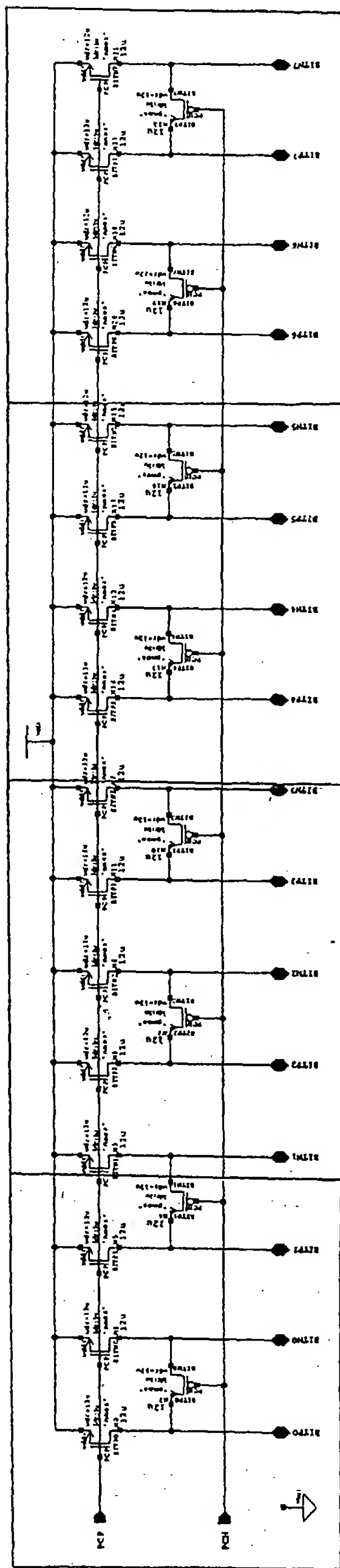


Fig. 7.0303

MICRON		Rev. 1.03	Rev. 1.03
COMMUNICATIONS, INC.		RAM Precharge	RAM Precharge
INTEGRATED CIRCUIT DESIGN		103revA/rampch	103revA/rampch
CONFIDENTIAL INFORMATION		Nov 12 02:58:36 1993	Nov 12 02:58:36 1993

7.0304AA	7.0304AB	7.0304AC	7.0304AD
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FILED JUL 30 1964

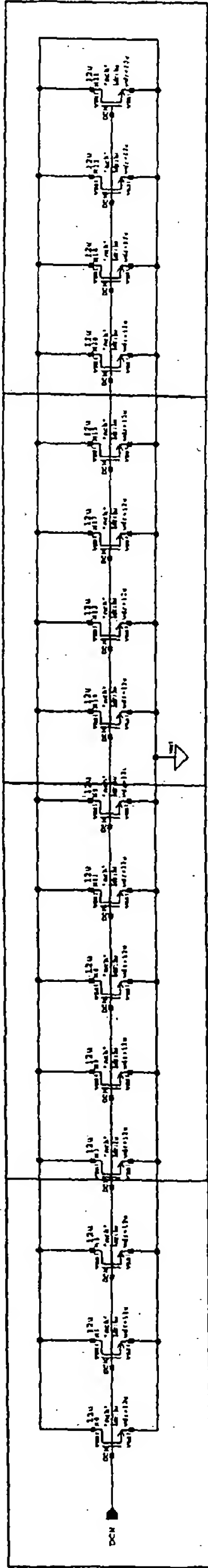
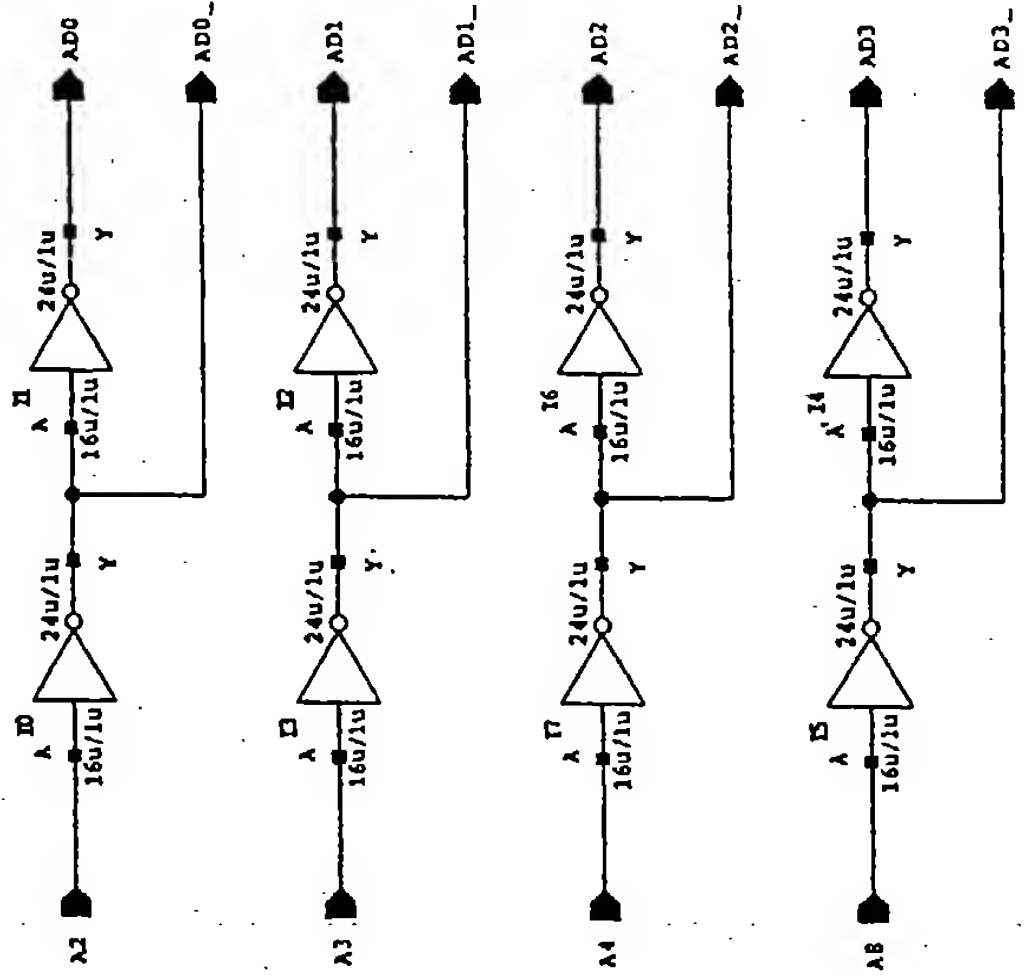


FIG. 7.0304

<b>MICRON</b>	PROJECT: L03	DESIGN: J0000LE
	NAME: RAH Precharge	
COMMUNICATIONS, INC.		
INTEGRATED CIRCUIT DESIGN		
CONFIDENTIAL INFORMATION		
DATE: 10/19/94	REV: 80	REV: 80
DATE: Jan 28 09:51:27 1996	REV: 80	REV: 80

88: disconnected dch devices from bit lines and tied to vss



**MICRON**  
 COMMUNICATIONS, INC.  
 INTEGRATED CIRCUIT DESIGN  
 CONFIDENTIAL INFORMATION

PROJECT: L03	DESIGNER: Rotzoll
TITLE: RAM Address Buffer	
NAME: 103reva/ramadb	REV: -
DATE: Sep 29 16:04:01 1993	SIZE: A
	SHEET: 1

Fig. 7.0305

MI40-030

7.0306AA

7.0306BA

7.0306 7.0306

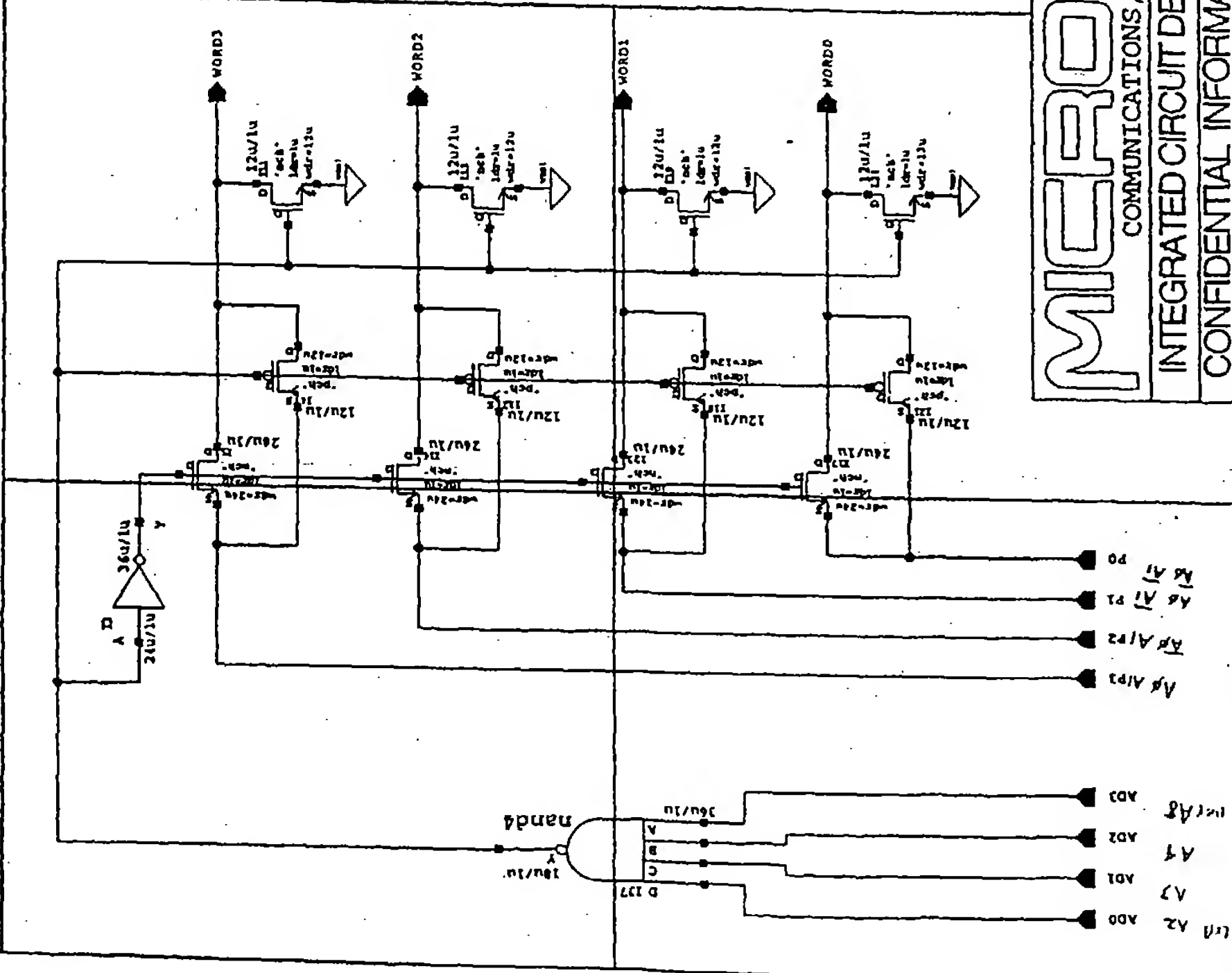


MI40-030

7.0307AA	7.0307AB
7.0307BA	7.0307BB

II 11 11 11 11 11

FIG. 7.0307



MICRON		PROJECT: L03	DESIGNED: Rotzoll
COMMUNICATIONS, INC.		RAM Word Line Decoder	
INTEGRATED CIRCUIT DESIGN		DATE: 103reva/ramwdec	REV: -
CONFIDENTIAL INFORMATION		DATE: Sep 29 15:41:08 1993	PART: A



MI40-030

7.0308AA	7.0308AB
7.0308BA	7.0308BB

7.0308 7.0308

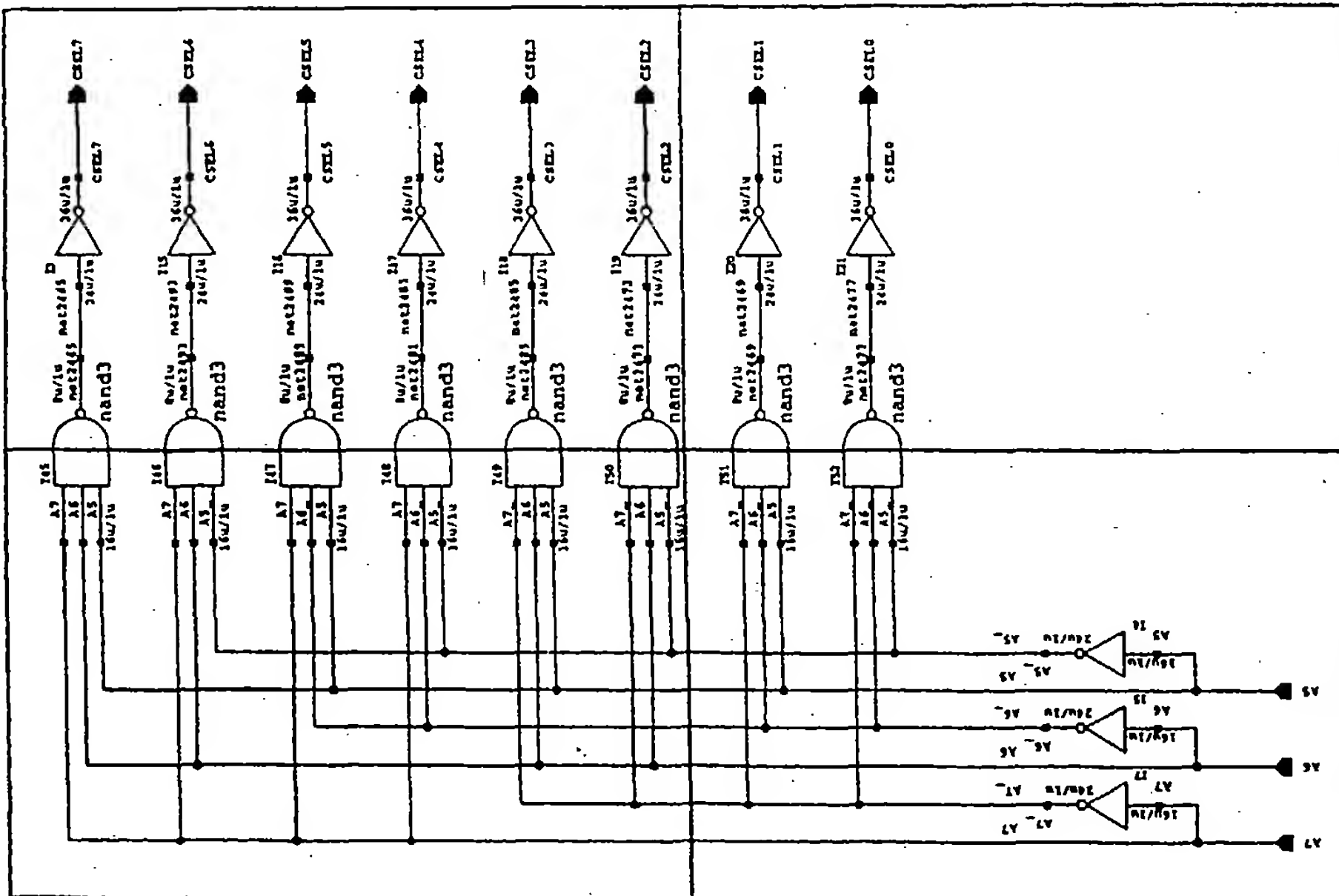


FIG. 7.0308

MICRON		Part No. L01	Rev. 10/20/91
COMMUNICATIONS, INC.		RAM Column Select Decode	
INTEGRATED CIRCUIT DESIGN		3 to 8	
CONFIDENTIAL INFORMATION		Rev. 10/20/91	Rev. 10/20/91
		Nov 5 17:21:07 1993	Rev. 10/20/91

7.0309AA	7.0309AB	7.0309AC	7.0309AD	7.0309AE	7.0309AF	7.0309AG
7.0309BA	7.0309BB	7.0309BC	7.0309BD	7.0309BE	7.0309BF	7.0309BG

SECRET





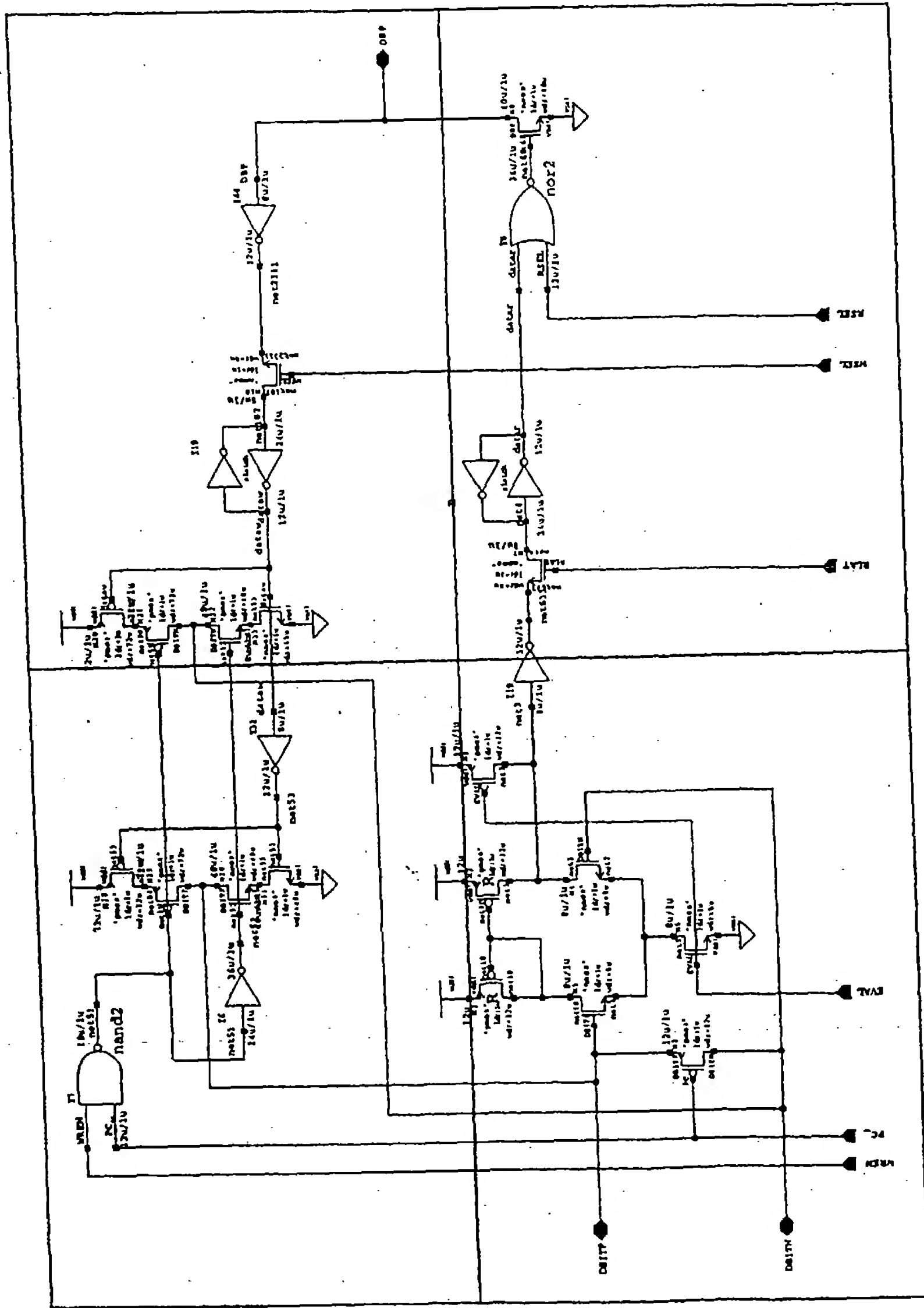


FIG. 7.0310

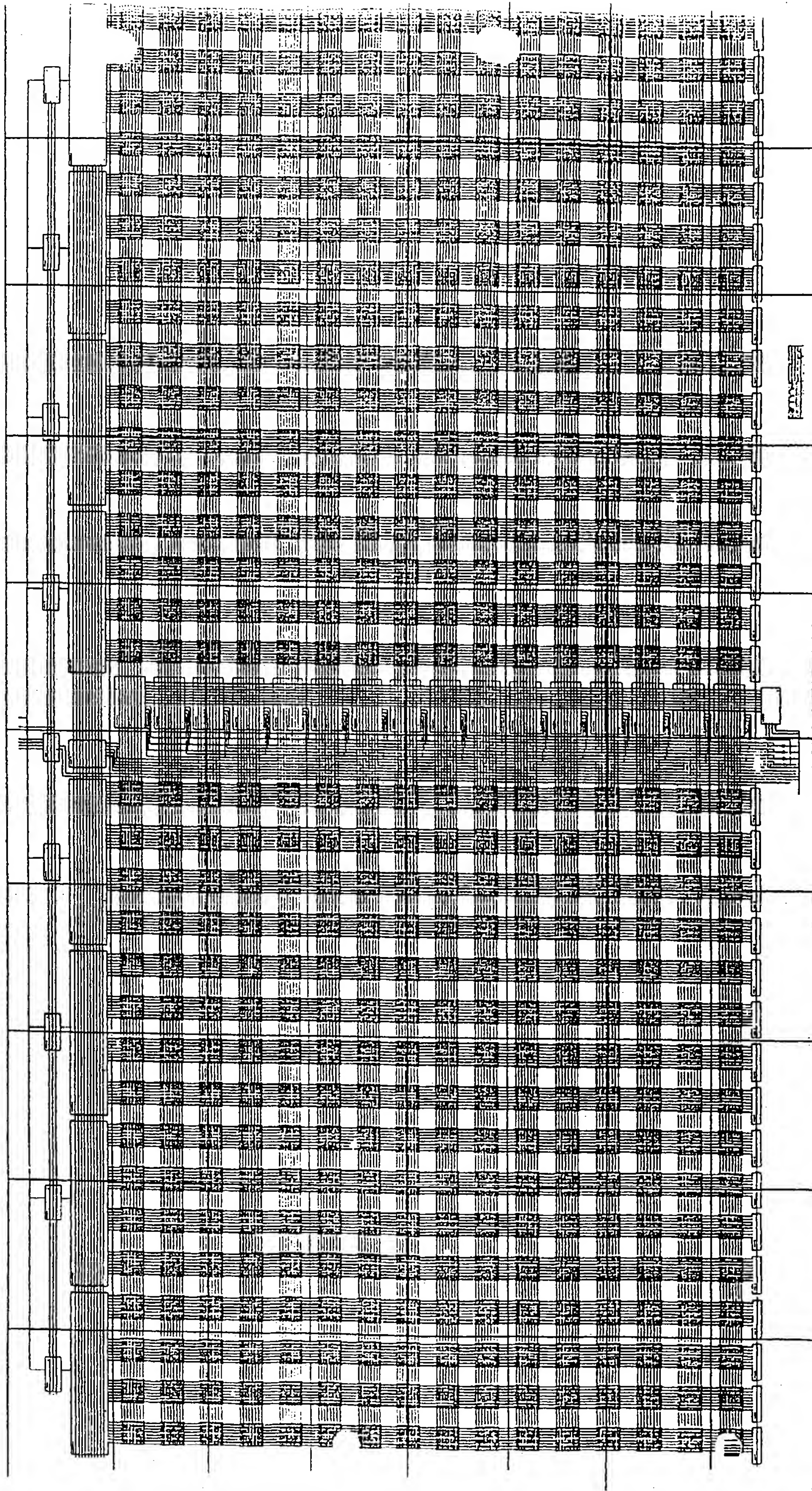
PROJECT: L03		REVISION: Retroll	
TITLE: RAM Databus Interface			
DESIGNER: 103reva/ramdb		DRAWN: -	
DATE: OCT 6 12:08:33 1993		PART: m1	

**MICRON**  
 COMMUNICATIONS, INC.  
 INTEGRATED CIRCUIT DESIGN  
 CONFIDENTIAL INFORMATION





FIG. 7.04





MI40-030

7.0401AB

7.0401AA

II. III. IV. V. VI. VII. VIII. IX. X. XI. XII.

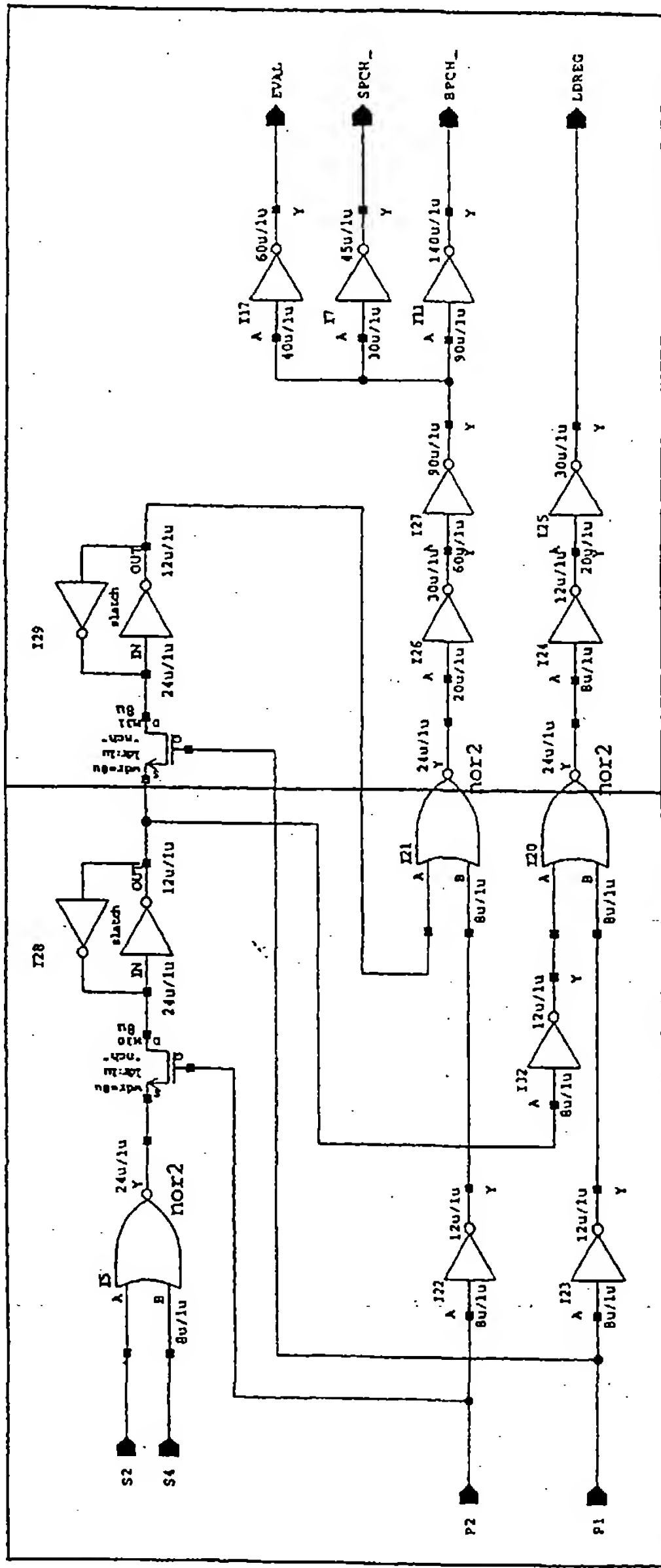
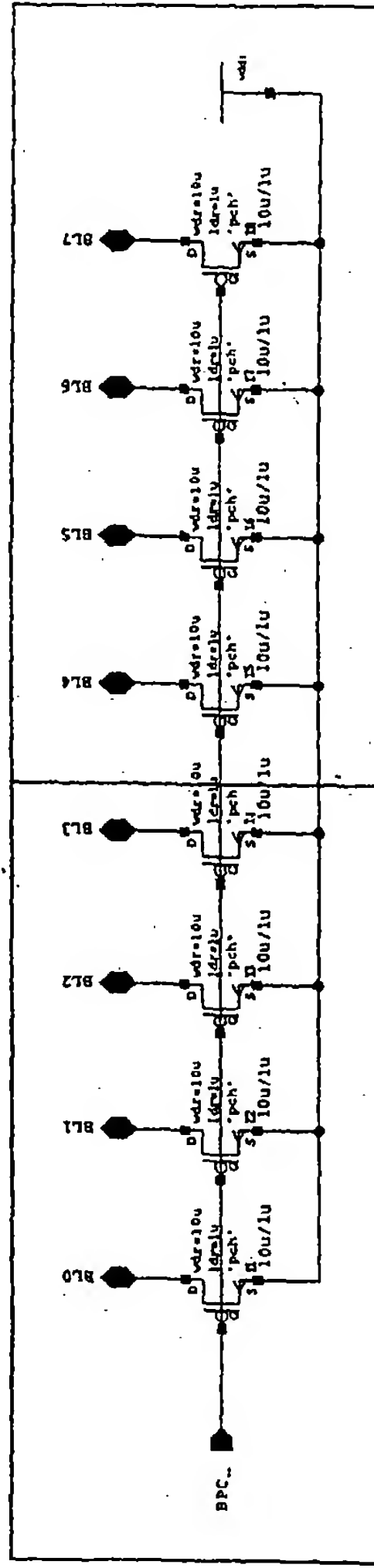


Fig. 7.04C

MICRON		PRODUCT: L03	DESIGNER: Rotzoll
COMMUNICATIONS, INC.		TITLE: ROM Control Logic	
INTEGRATED CIRCUIT DESIGN		NAME: 103reva/romctl	REV: -
CONFIDENTIAL INFORMATION		DATE: Oct 3 13:16:28 1993	SIZE: A

7.0402AA	7.0402AB
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7.0402



**MICRON**  
 COMMUNICATIONS, INC.  
 INTEGRATED CIRCUIT DESIGN  
 CONFIDENTIAL INFORMATION

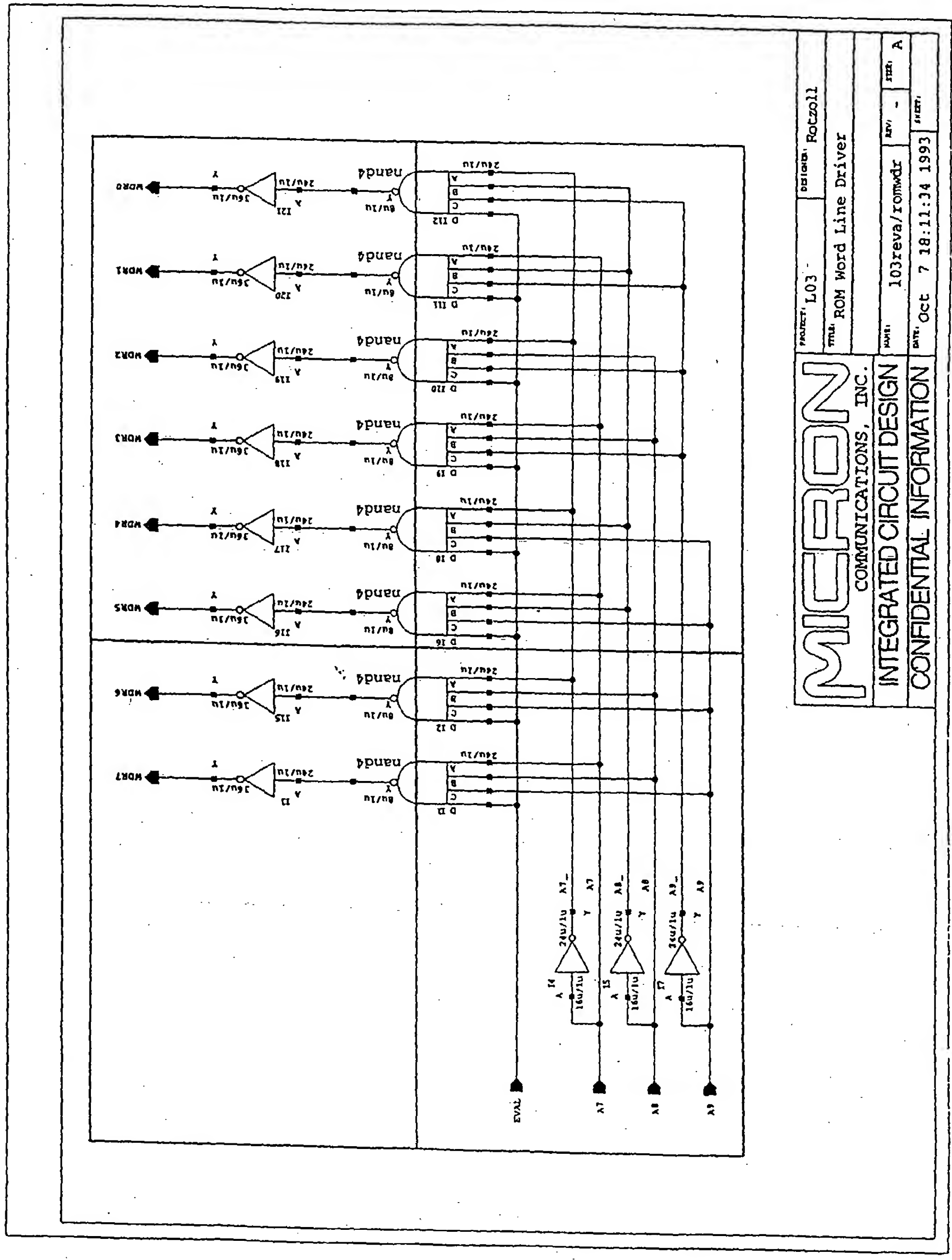
PRODUCT: L03	DESIGNER: Rotzoll
TITLE: ROM Bit Line Precharge	
NAME: 103reva/rompch	REV: -
DATE: Oct 7 18:09:48 1993	SIZE: A
SHEET: 1	

Fig. 7.0902

7.0403AA	7.0403AB
7.0403BA	7.0403BB

IIII 7.0403BB

FIG. 7.0903



PROJECT: L03		DESIGNED: Rotzoll	
TITLE: ROM Word Line Driver			
NAME:	103reva/romwdr	REV:	1
DATE:	Oct 7 18:11:34 1993	SHEET:	A
MICRON COMMUNICATIONS, INC.			
INTEGRATED CIRCUIT DESIGN			
CONFIDENTIAL INFORMATION			

	7.0404AB	7.0404AC
7.0404BA	7.0404BB	7.0404BC
	7.0404CB	7.0404CC
	7.0404DB	7.0404DC

II II II 7.040404

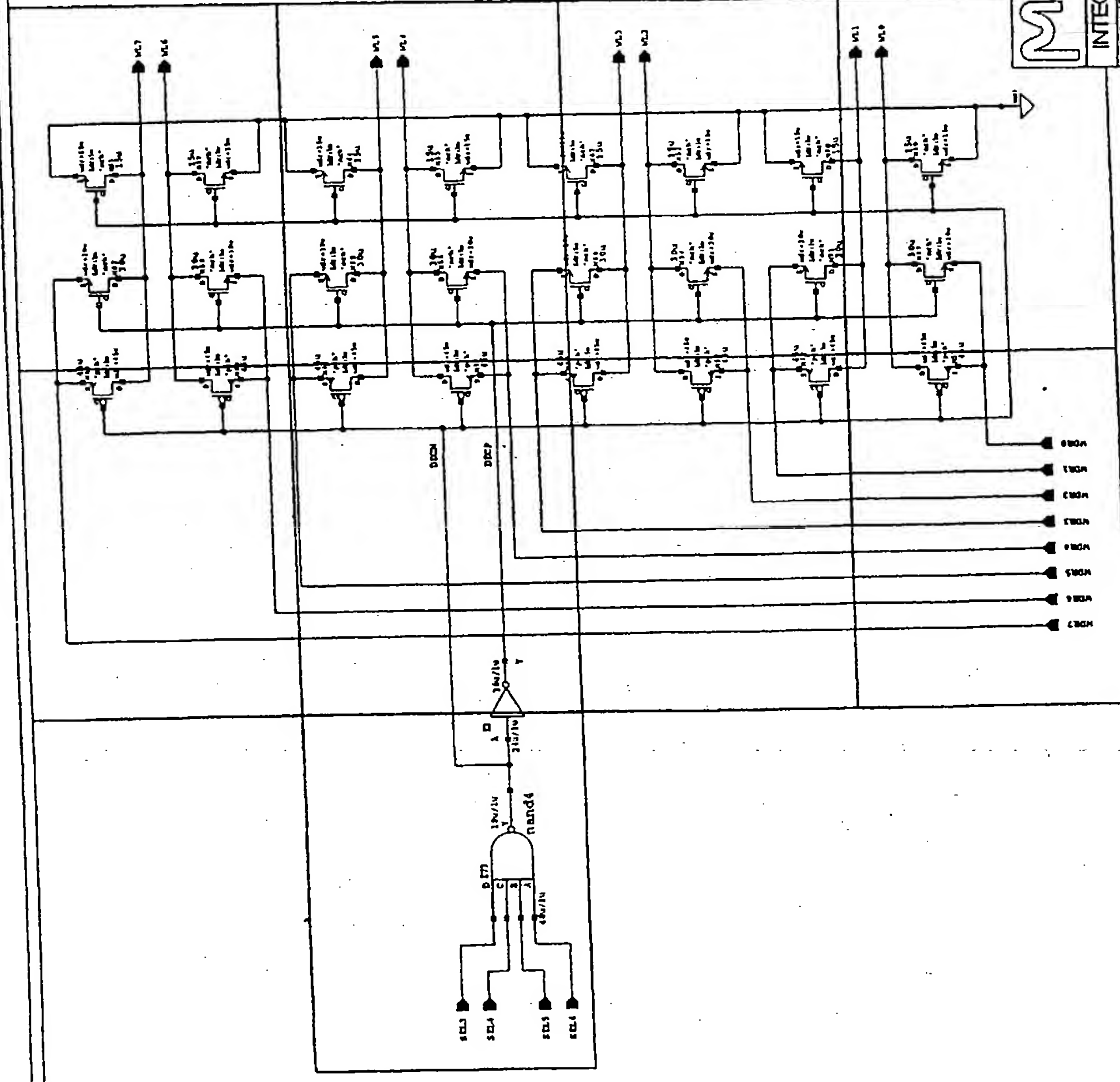


FIG. 7.0404

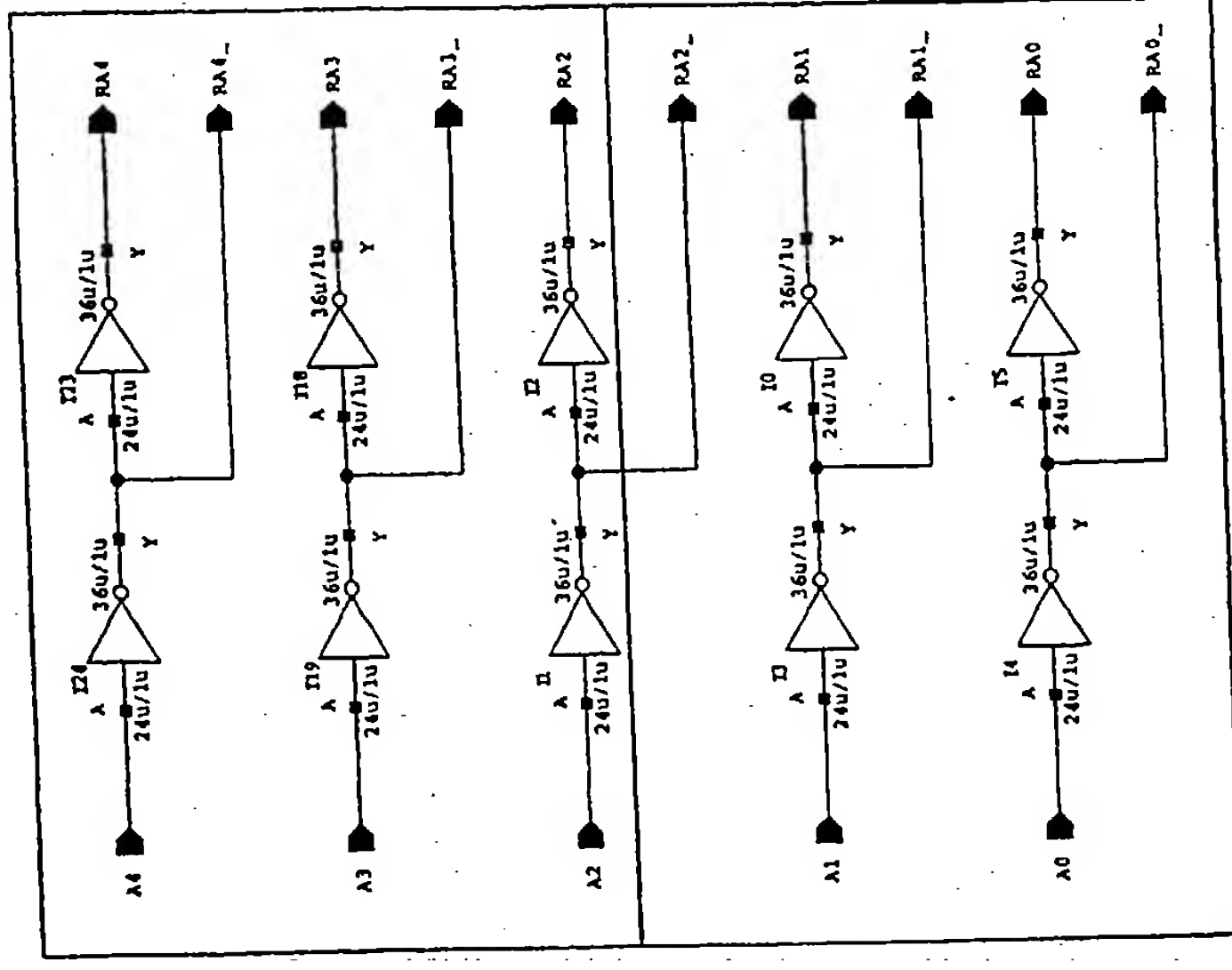
MICRON		PRODUCT L03	REVISION 1022011
COMMUNICATIONS, INC.		Word Block Decoder	
INTEGRATED CIRCUIT DESIGN		DESIGNER J03revA/romwdec_rev	DATE -
CONFIDENTIAL INFORMATION		DATE Nov 5 17:38:09 1993	BY ml



7.0405AA

7.0405BA

II II II 7.0405



MICRON				DESIGNER: Rotzoll	
PROJECT: L03					
TITLE: ROM Bit Line Address Driver					
NAME: 103reva/rombldr				REV: -	SIZE: A
DATE: Oct 7 12:08:42 1993				SHEET:	
COMMUNICATIONS, INC.					
INTEGRATED CIRCUIT DESIGN					
CONFIDENTIAL INFORMATION					

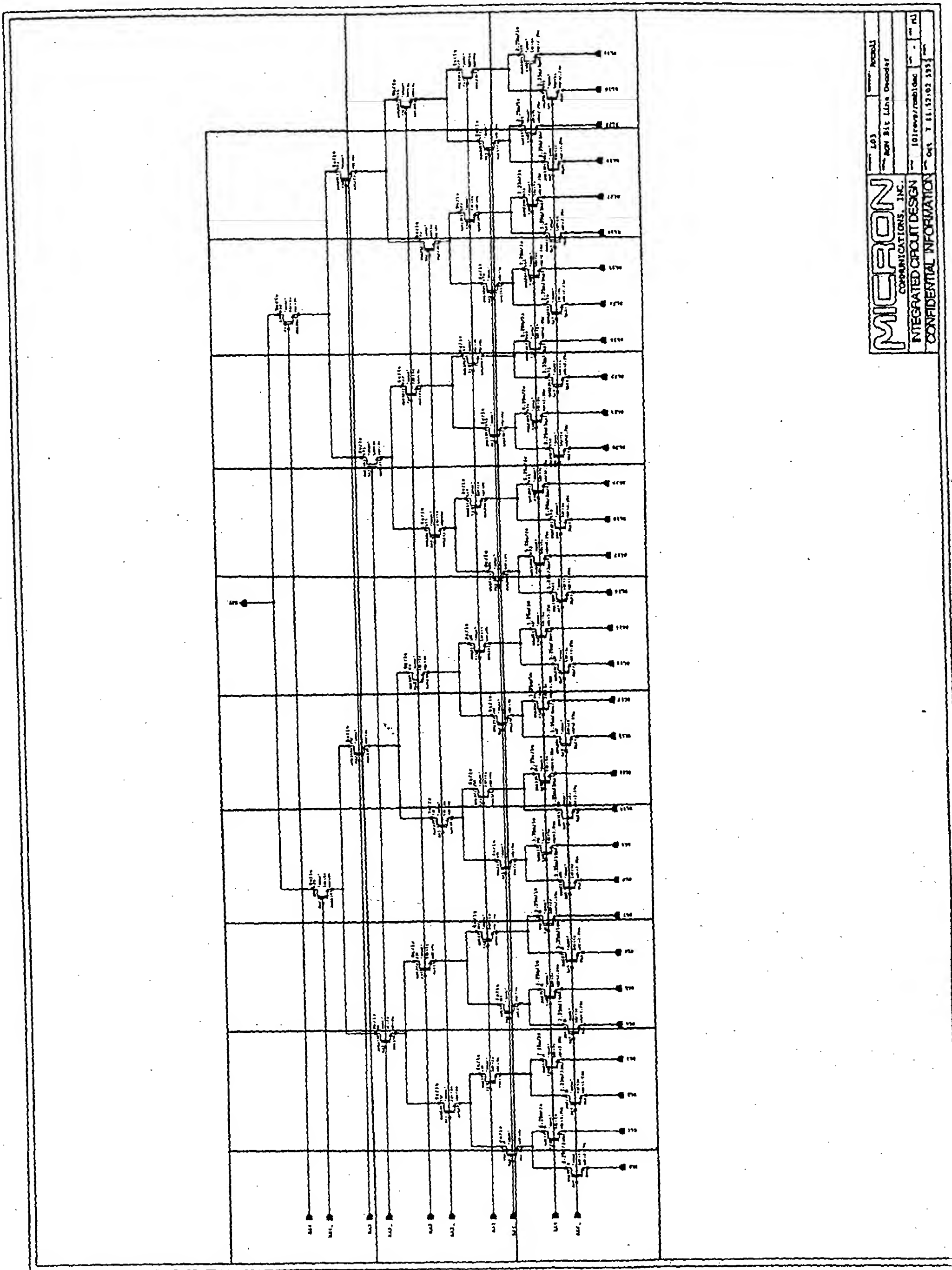
**MICRON**  
 COMMUNICATIONS, INC.  
 INTEGRATED CIRCUIT DESIGN  
 CONFIDENTIAL INFORMATION

FIG. 7.0405

7.0406AA	7.0406AB	7.0406AC	7.0406AD	7.0406AE	7.0406AF	7.0406AG	7.0406AH	7.0406AI	7.0406AJ	
7.0406BA	7.0406BB	7.0406BC	7.0406BD	7.0406BE	7.0406BF	7.0406BG	7.0406BH	7.0406BI	7.0406BJ	7.0406BK
7.0406CA	7.0406CB	7.0406CC	7.0406CD	7.0406CE	7.0406CF	7.0406CG	7.0406CH	7.0406CI	7.0406CJ	7.0406CK

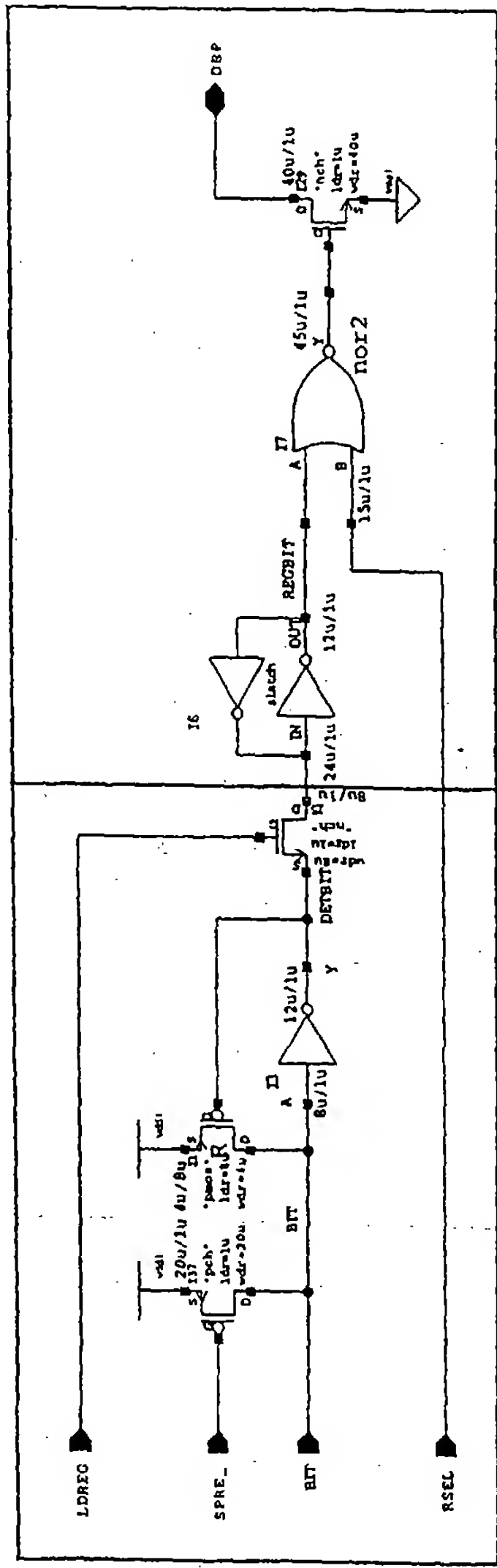
IEEE 7.0406

Fig. 7.0406



7.0407AA	7.0407AB
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7.0407AA 7.0407AB



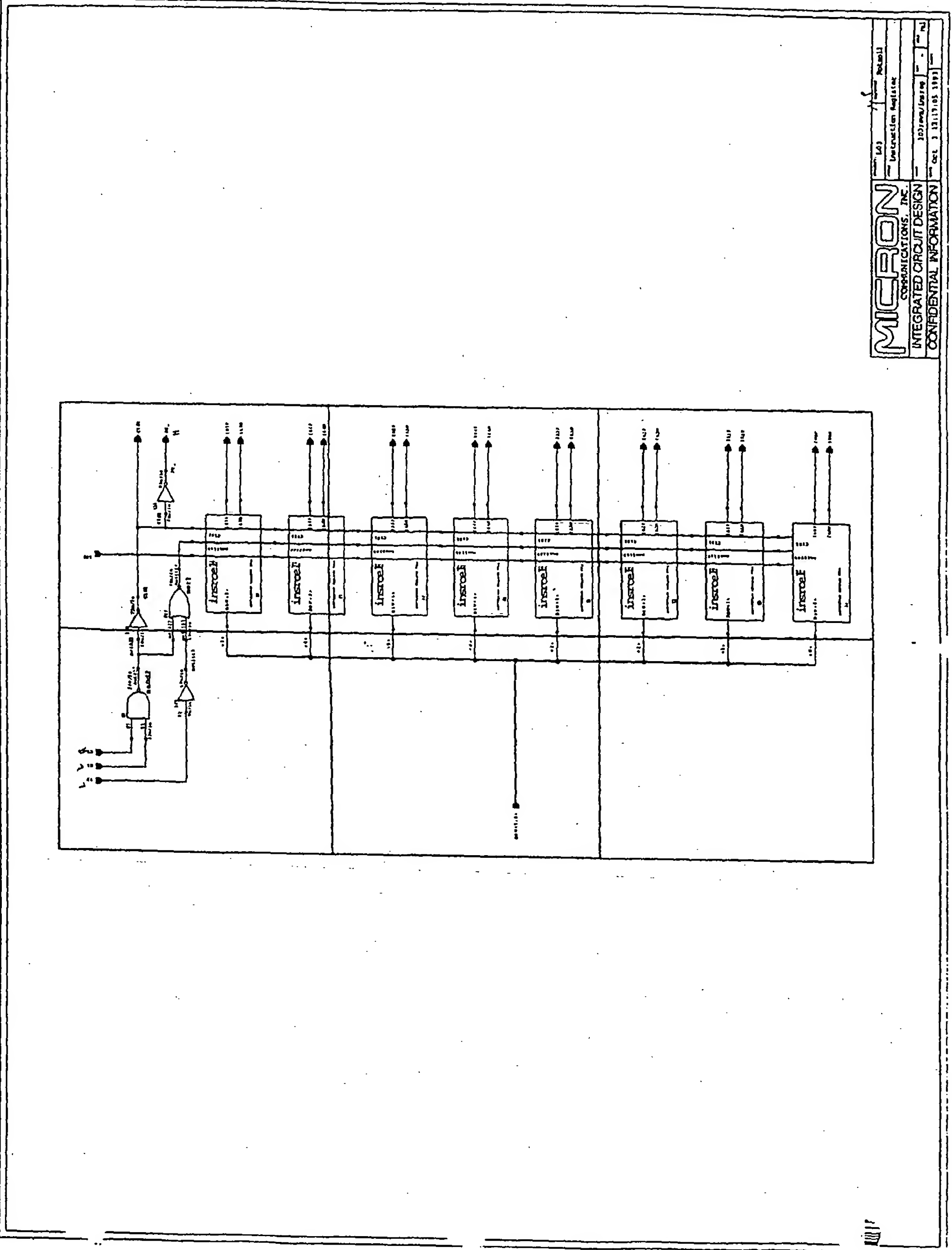
**MICRON**  
 COMMUNICATIONS, INC.  
 INTEGRATED CIRCUIT DESIGN  
 CONFIDENTIAL INFORMATION

PROJECT: L03	DESIGNER: Rotzoll
TITLE: ROM Sense Amplifier	
NAME: 103reva/romsns	REV: -
DATE: Oct 7 18:12:58 1993	SHEET: A

FIG. 7.0407

7.05AA	7.05AB
7.05BA	7.05BB
7.05CA	7.05CB

FIG. 7.05



**MICRON**  
 COMMUNICATIONS, INC.  
 INTEGRATED CIRCUIT DESIGN  
 CONFIDENTIAL INFORMATION

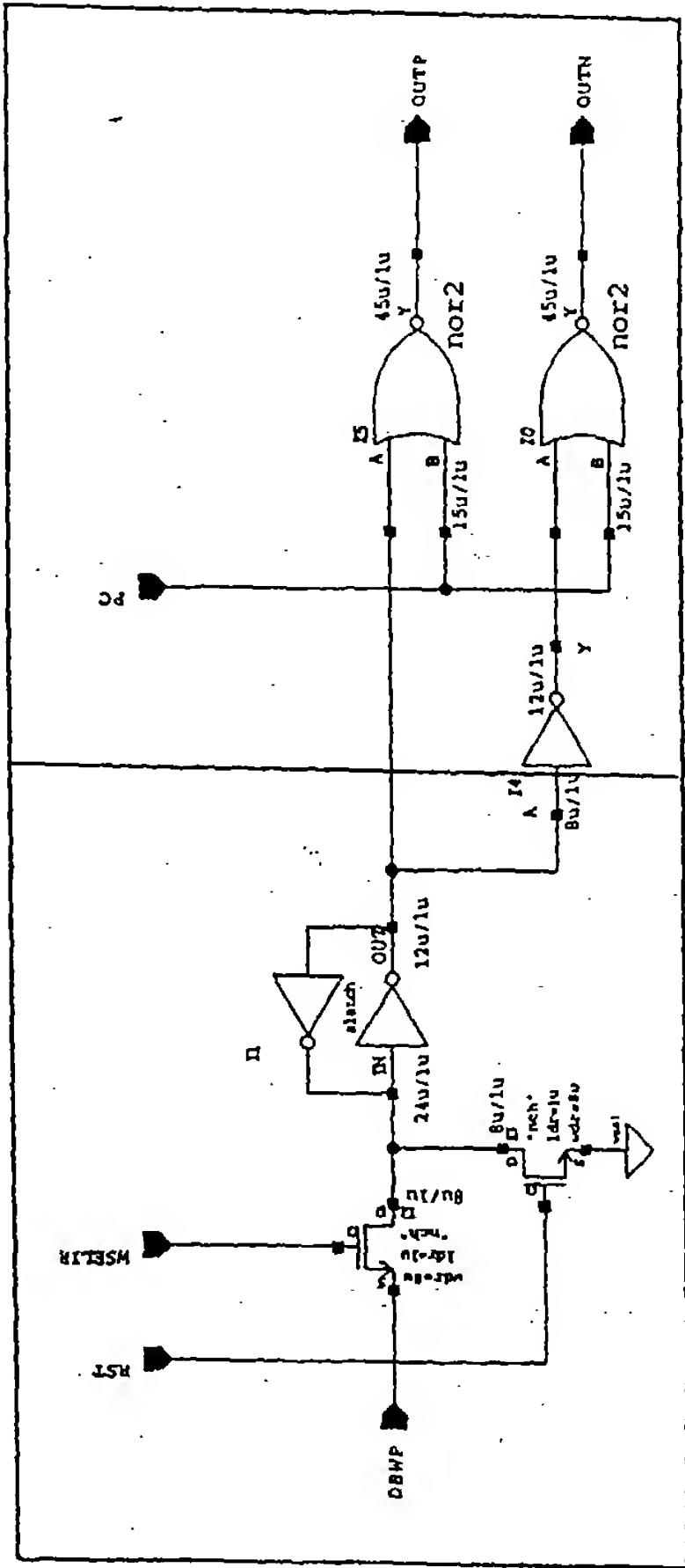
Rev. 1.03  
 Instruction Register  
 10/20/80/10/80  
 Oct. 3 12:17:05 1980



7.0501AA	7.0501AB
----------	----------

EX-10501

Fig. 7.0501



MICRON		PROJECT: L03	DESIGNER: Rotzoll
COMMUNICATIONS, INC.		TITLE: Instruction Register Cell	
INTEGRATED CIRCUIT DESIGN		MADE: 103reva/insrcel	REV: -
CONFIDENTIAL INFORMATION		DATE: Oct 5 20:12:49 1993	SHEET: A



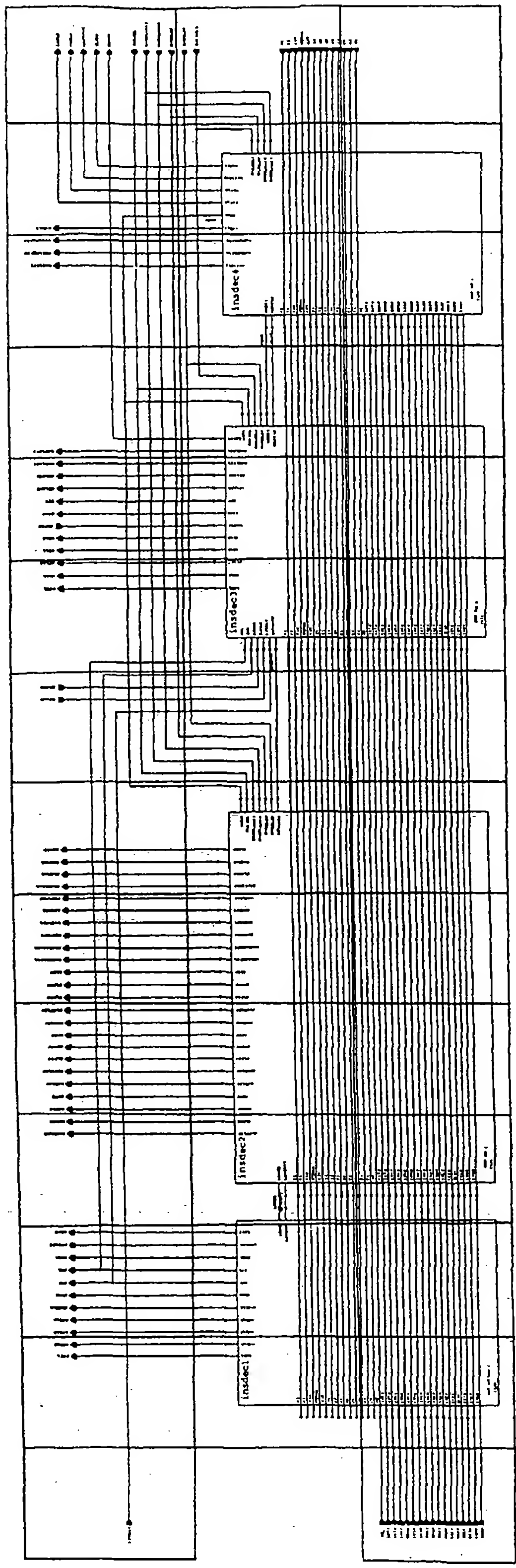


Fig. 7.06

7.0601AA	7.0601AB	7.0601AC	7.0601AD	7.0601AE	7.0601AF	7.0601AG	7.0601AH	7.0601AI
7.0601BA	7.0601BB	7.0601BC	7.0601BD	7.0601BE	7.0601BF	7.0601BG	7.0601BH	7.0601BI
7.0601CA	7.0601CB	7.0601CC	7.0601CD	7.0601CE	7.0601CF	7.0601CG	7.0601CH	7.0601CI
7.0601DA	7.0601DB	7.0601DC	7.0601DD	7.0601DE	7.0601DF	7.0601DG	7.0601DH	7.0601DI
7.0601EA	7.0601EB	7.0601EC	7.0601ED	7.0601EE	7.0601EF	7.0601EG	7.0601EH	7.0601EI
7.0601FA	7.0601FB	7.0601FC	7.0601FD	7.0601FE	7.0601FF	7.0601FG	7.0601FH	7.0601FI
7.0601GA	7.0601GB	7.0601GC	7.0601GD	7.0601GE	7.0601GF	7.0601GG	7.0601GH	7.0601GI
7.0601HA	7.0601HB	7.0601HC	7.0601HD	7.0601HE	7.0601HF	7.0601HG	7.0601HH	7.0601HI

И.И.С. 7.0601

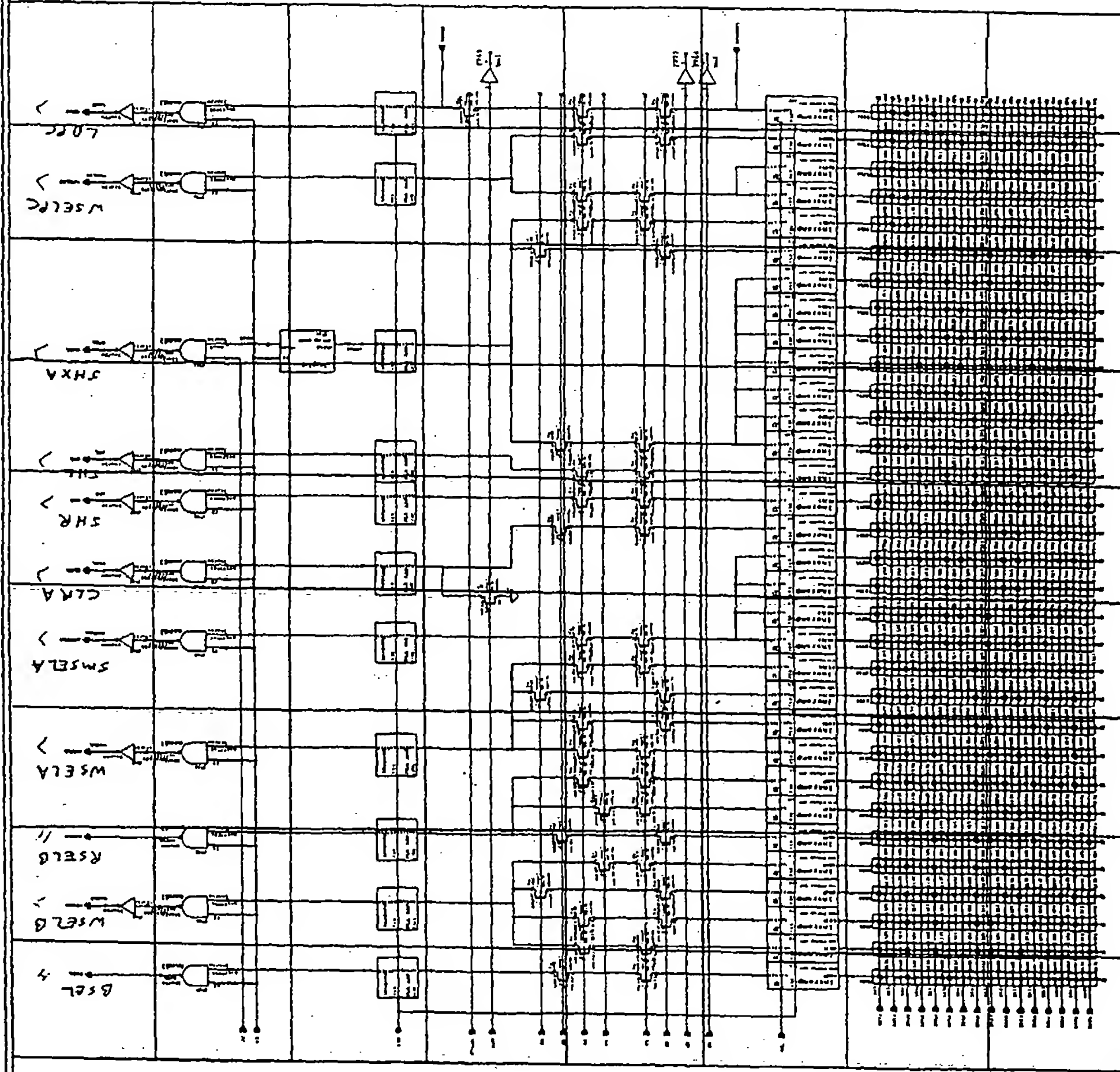
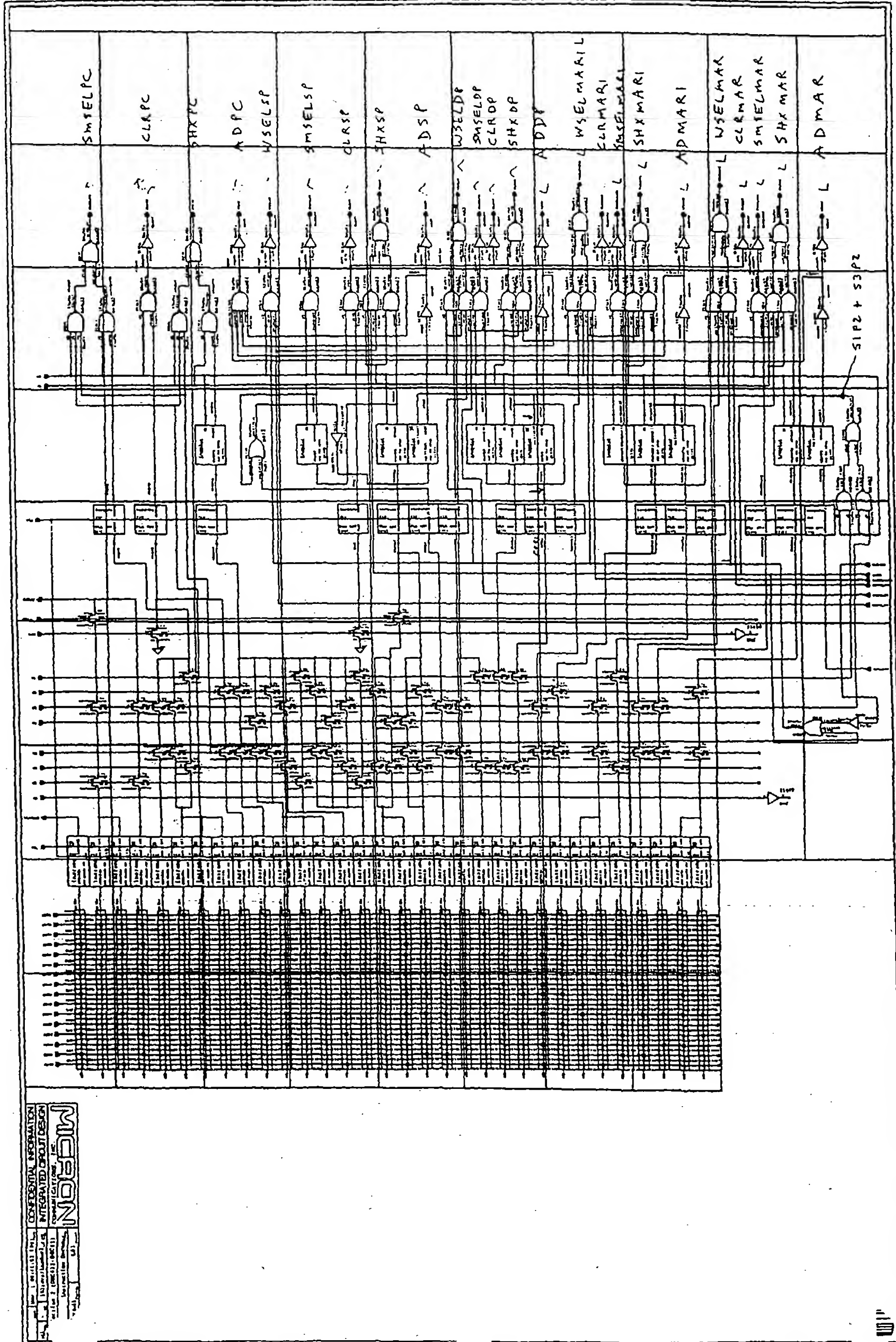


Fig. 7.0601

7.0602AA	7.0602AB	7.0602AC	7.0602AD	7.0602AE	7.0602AF	7.0602AG	7.0602AH
7.0602BA	7.0602BB	7.0602BC	7.0602BD	7.0602BE	7.0602BF	7.0602BG	7.0602BH
7.0602CA	7.0602CB	7.0602CC	7.0602CD	7.0602CE	7.0602CF	7.0602CG	7.0602CH
7.0602DA	7.0602DB	7.0602DC	7.0602DD	7.0602DE	7.0602DF	7.0602DG	7.0602DH
7.0602EA	7.0602EB	7.0602EC	7.0602ED	7.0602EE	7.0602EF	7.0602EG	7.0602EH
7.0602FA	7.0602FB	7.0602FC	7.0602FD	7.0602FE	7.0602FF	7.0602FG	7.0602FH
7.0602GA	7.0602GB	7.0602GC	7.0602GD	7.0602GE	7.0602GF	7.0602GG	7.0602GH
7.0602HA	7.0602HB	7.0602HC	7.0602HD	7.0602HE	7.0602HF	7.0602HG	7.0602HH
		7.0602IC	7.0602ID	7.0602IE	7.0602IF	7.0602IG	7.0602IH
		7.0602JC	7.0602JD	7.0602JE	7.0602JF	7.0602JG	7.0602JH



-ADPC is bus  
bus of WSELSP, ADPC, ADMAR  
ADPC, ADDP, ADMAR  
ADPC

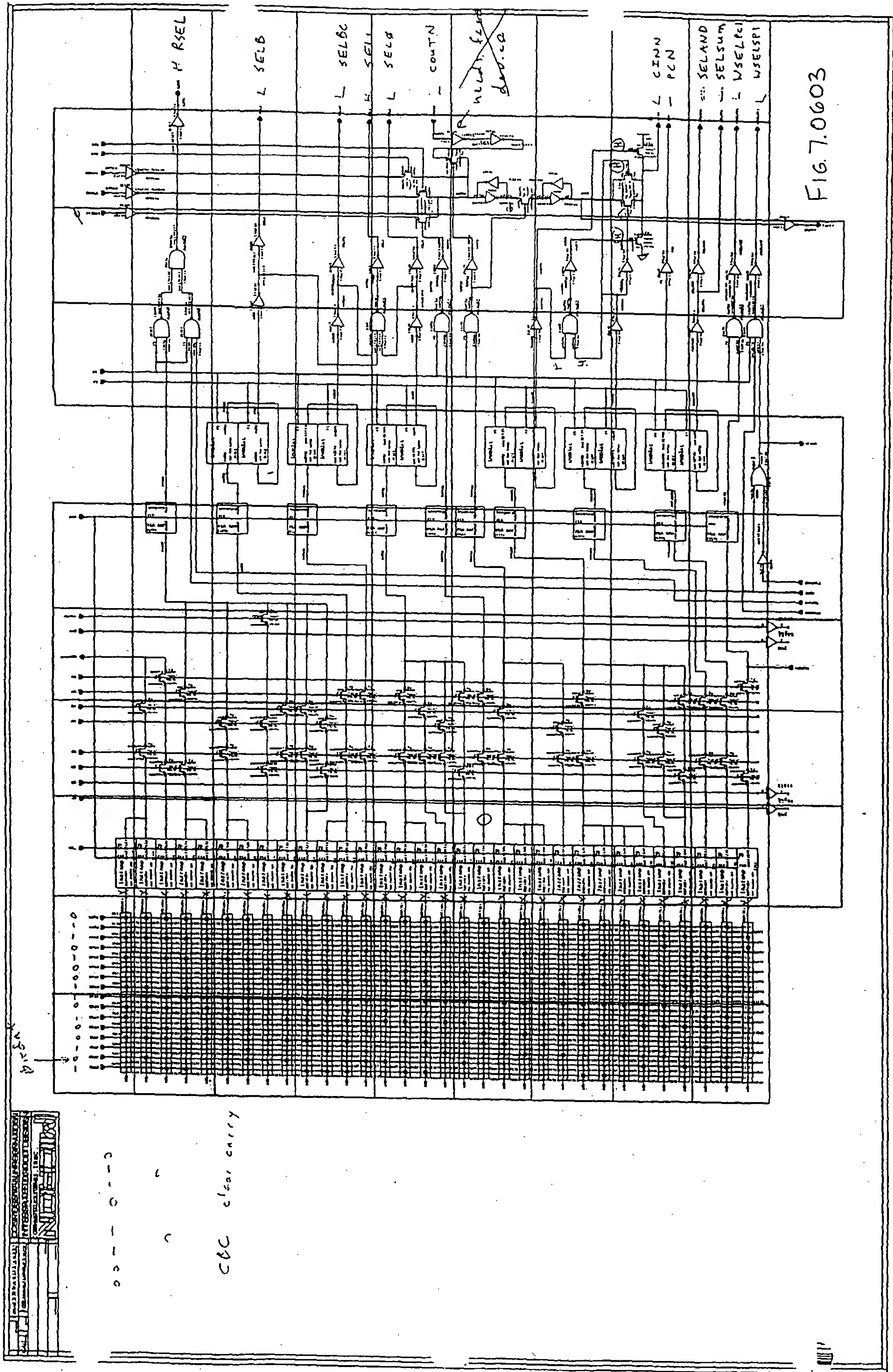
FIG. 7.0602

CONFIDENTIAL INFORMATION  
INTEGRATED CIRCUIT DESIGN  
NORBITAL  
NORBITAL CORPORATION, INC.  
NORBITAL CORPORATION, INC.  
NORBITAL CORPORATION, INC.



7.0603AA	7.0603AB	7.0603AC	7.0603AD	7.0603AE	7.0603AF	7.0603AH	7.0603AI	7.0603AJ
7.0603BA	7.0603BB	7.0603BC	7.0603BD	7.0603BE	7.0603BF	7.0603BG	7.0603BI	7.0603BJ
7.0603CA	7.0603CB	7.0603CC	7.0603CD	7.0603CE	7.0603CF	7.0603CG	7.0603CI	7.0603CJ
7.0603DA	7.0603DB	7.0603DC	7.0603DD	7.0603DE	7.0603DF	7.0603DG	7.0603DI	7.0603DJ
7.0603EA	7.0603EB	7.0603EC	7.0603ED	7.0603EE	7.0603EF	7.0603EG	7.0603EI	7.0603EJ
7.0603FA	7.0603FB	7.0603FC	7.0603FD	7.0603FE	7.0603FF	7.0603FG	7.0603FI	7.0603FJ
7.0603GA	7.0603GB	7.0603GC	7.0603GD	7.0603GE	7.0603GF	7.0603GG	7.0603GI	7.0603GJ
7.0603HA	7.0603HB	7.0603HC	7.0603HD	7.0603HE	7.0603HF	7.0603HG	7.0603HI	7.0603HJ
7.0603IA	7.0603IB	7.0603IC	7.0603ID	7.0603IE	7.0603IF	7.0603IG	7.0603IH	7.0603IJ
		7.0603JC	7.0603JD	7.0603JE	7.0603JF	7.0603JG	7.0603JI	
								7.0603BK

7.0603





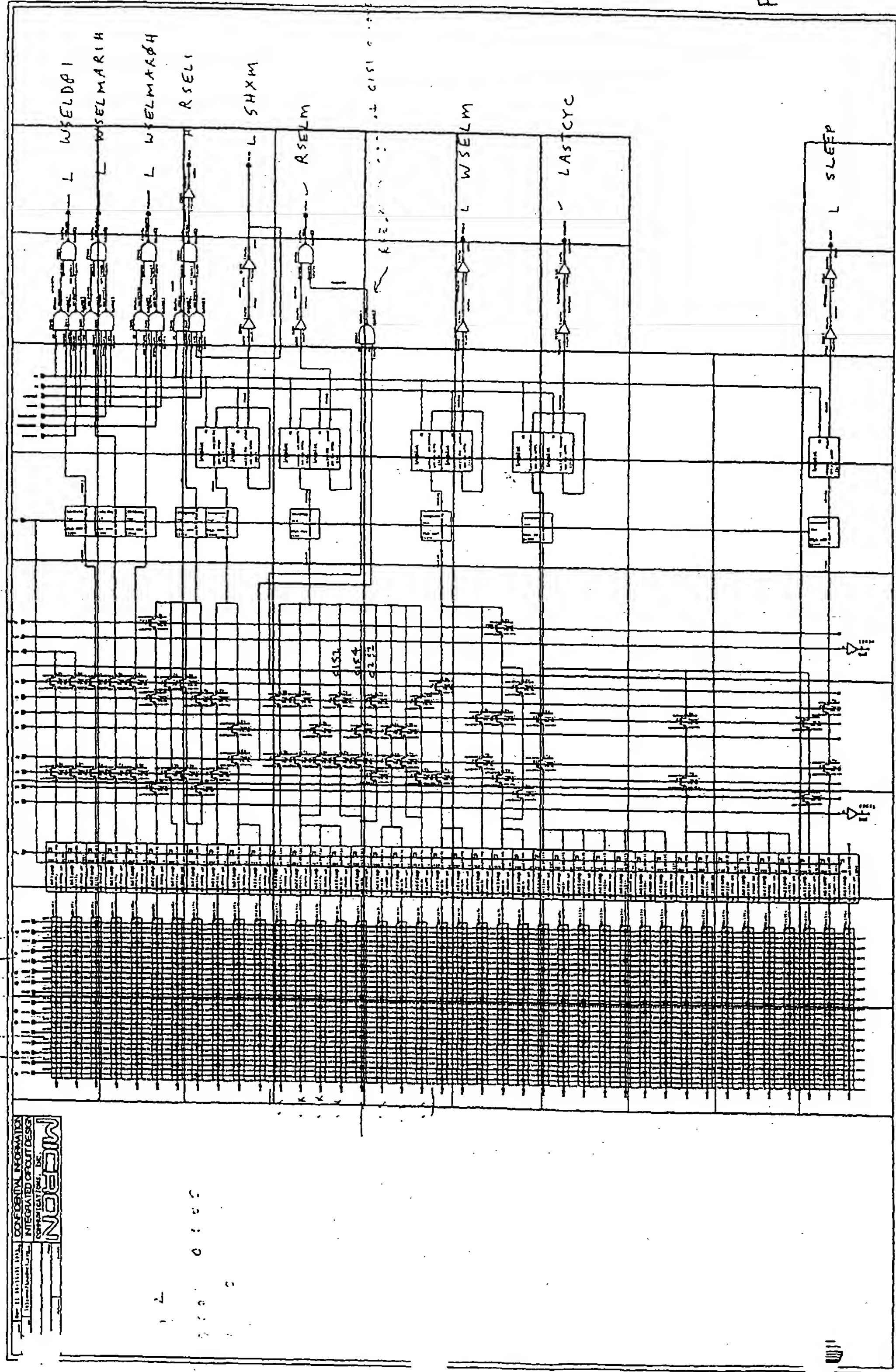


FIG. 7.06

INFORMATION  
 INTEGRATED CIRCUITS  
 CORPORATION  
 2800 ZEEB RD.  
 FOLSOM, CA 95630  
 (916) 438-5000  
 FAX (916) 438-5001  
 TELEX 153200  
 CABLE 153200  
 MAILING LIST  
 NO. 1000





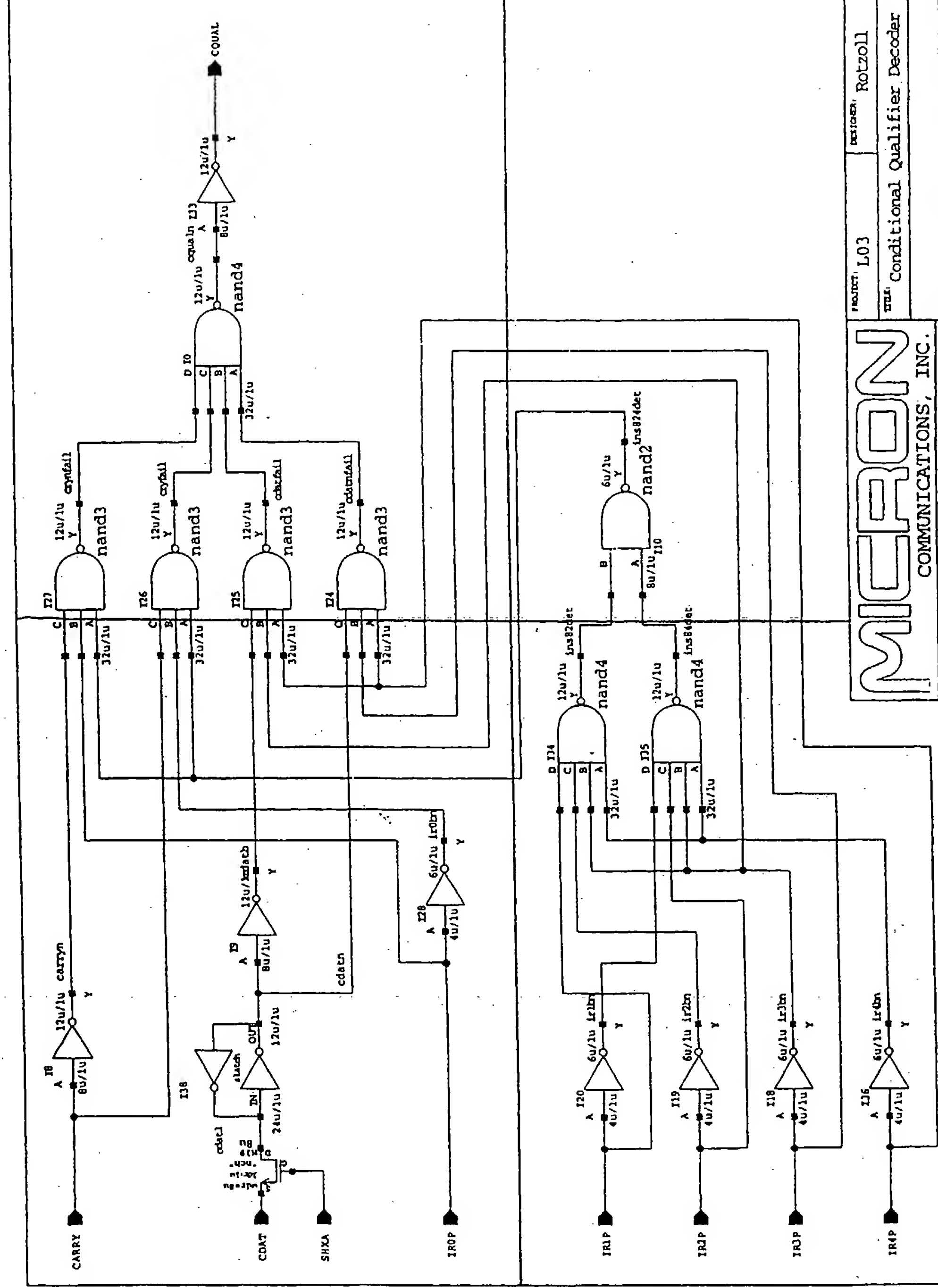


7.07AA	7.07AB
7.07BA	7.07BB

II II III III



Fig. 7.07



**MICRON**  
COMMUNICATIONS, INC.

PROJECT: L03     DESIGNER: Rotzoll

TITLE: Conditional Qualifier Decoder

NAME: 103reva/cqualdec     REV: -     DES: A

DATE: Nov 17 20:09:12 1993     DESK: 1

INTEGRATED CIRCUIT DESIGN

CONFIDENTIAL INFORMATION

7.08AA

7.08BA

7.08CA

IF II 07 7.08B

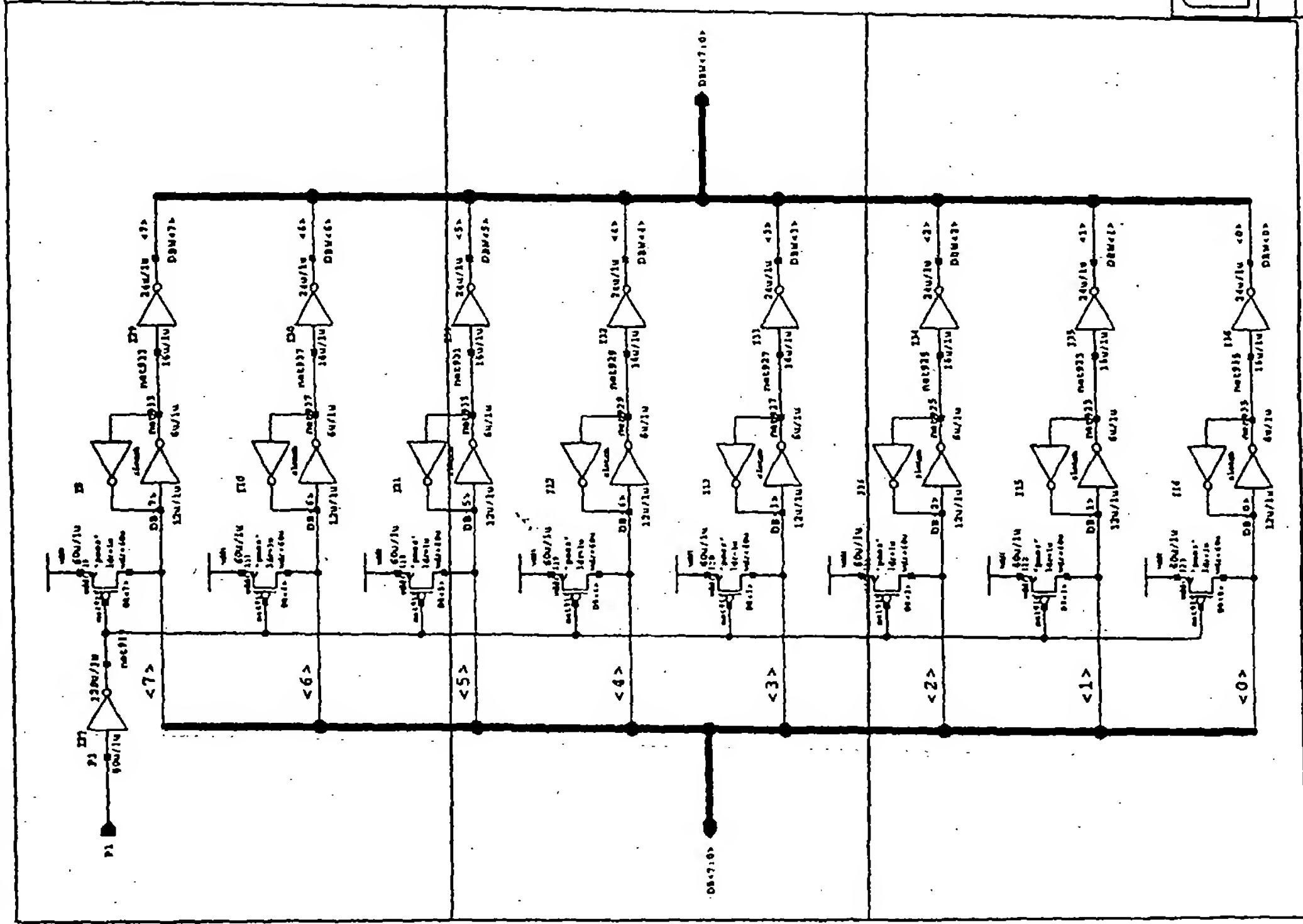


FIG. 7.08

MICRON		PRODUCT: L03	DESIGNED: Rotzoll
COMMUNICATIONS, INC.		NAME: Databus Latch/Precharge	
INTEGRATED CIRCUIT DESIGN		DATE: 103 reva/dblatch	REV: - r11
CONFIDENTIAL INFORMATION		DATE: Oct 1 14:51:49 1993	DESIGNED BY: r11

7.09AA	7.09AB	7.09AC	7.09AD	7.09AE	7.09AF
7.09BA	7.09BB	7.09BC	7.09BD	7.09BE	7.09BF

7.09

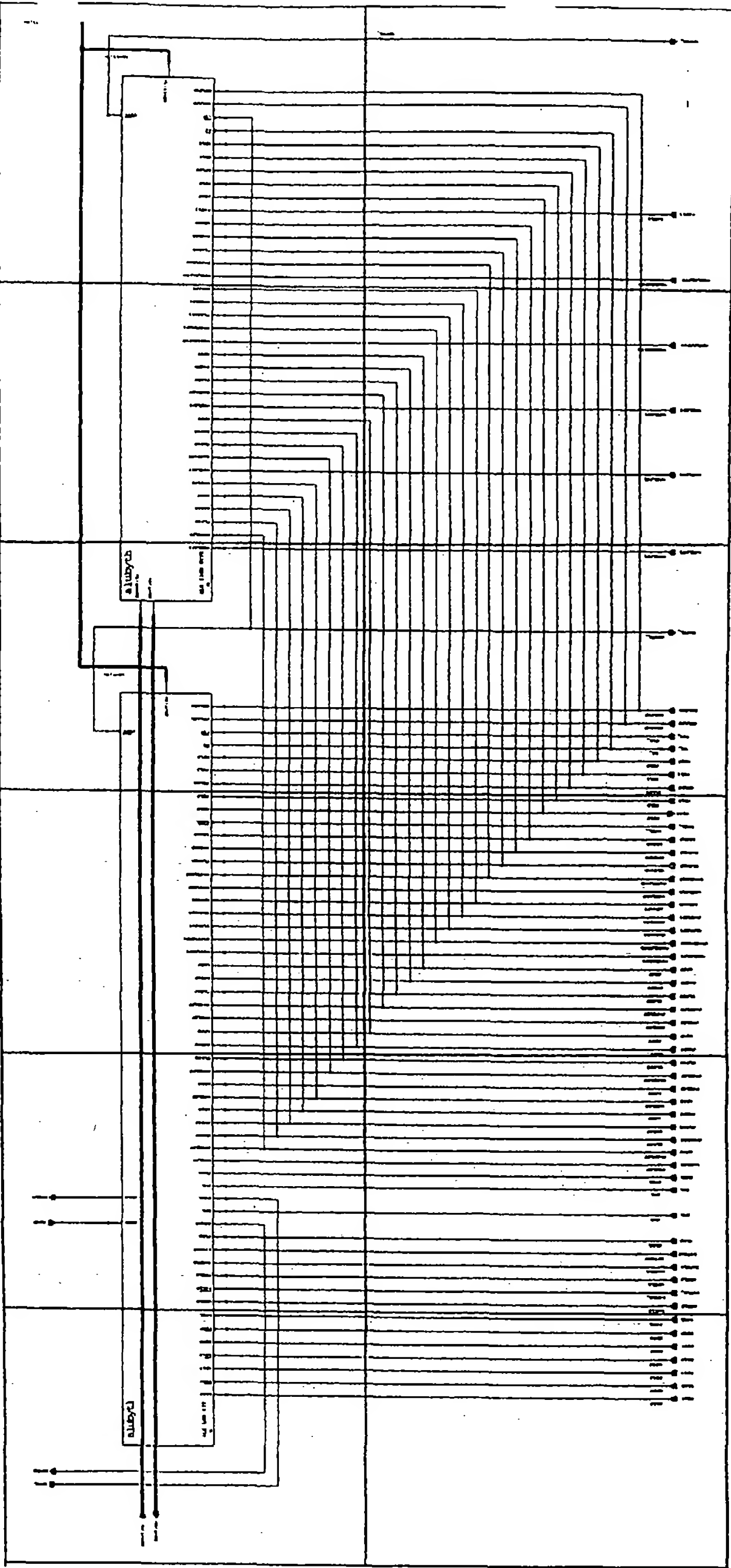


FIG. 7.09



FIG. 7.0901

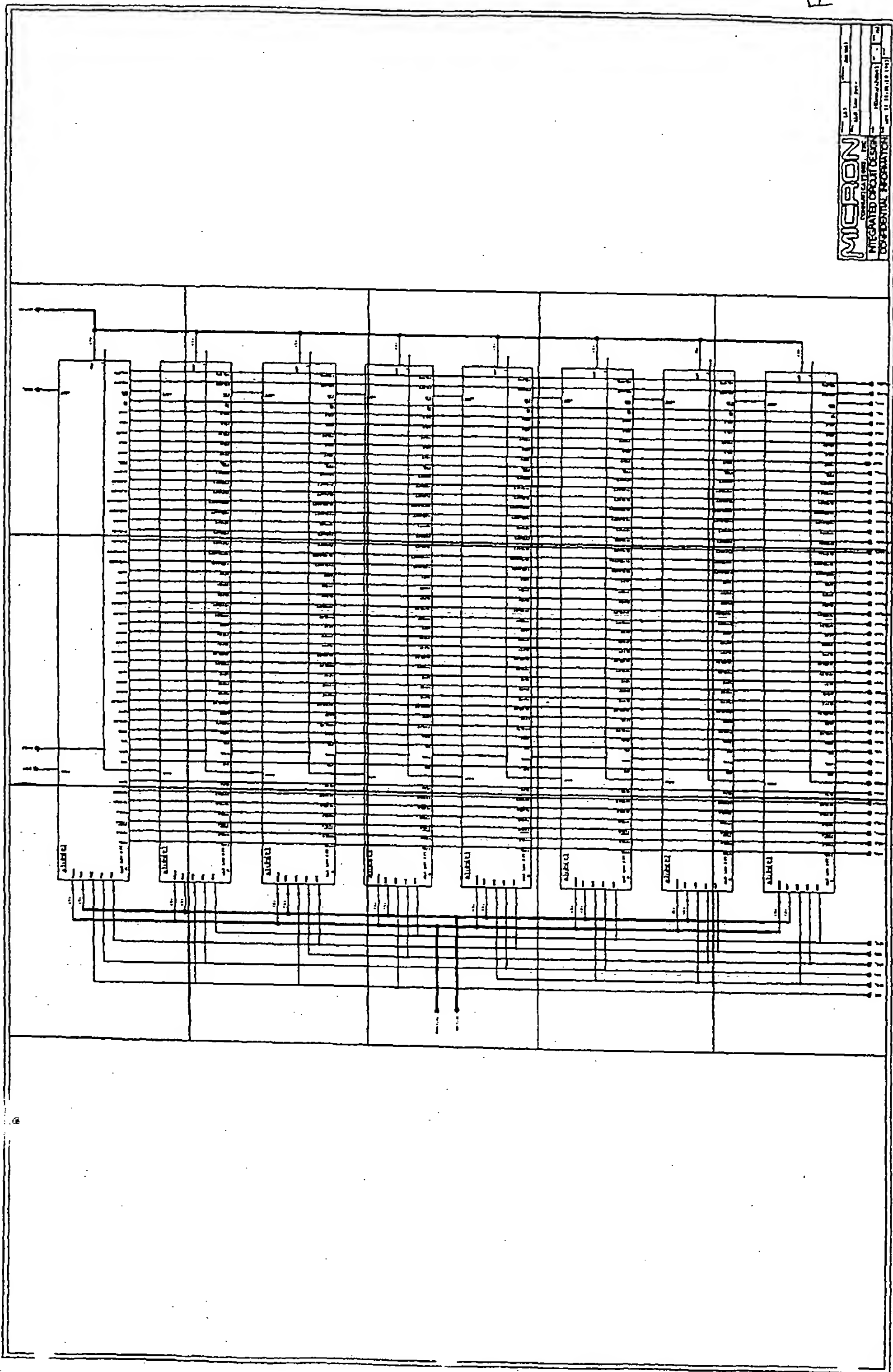
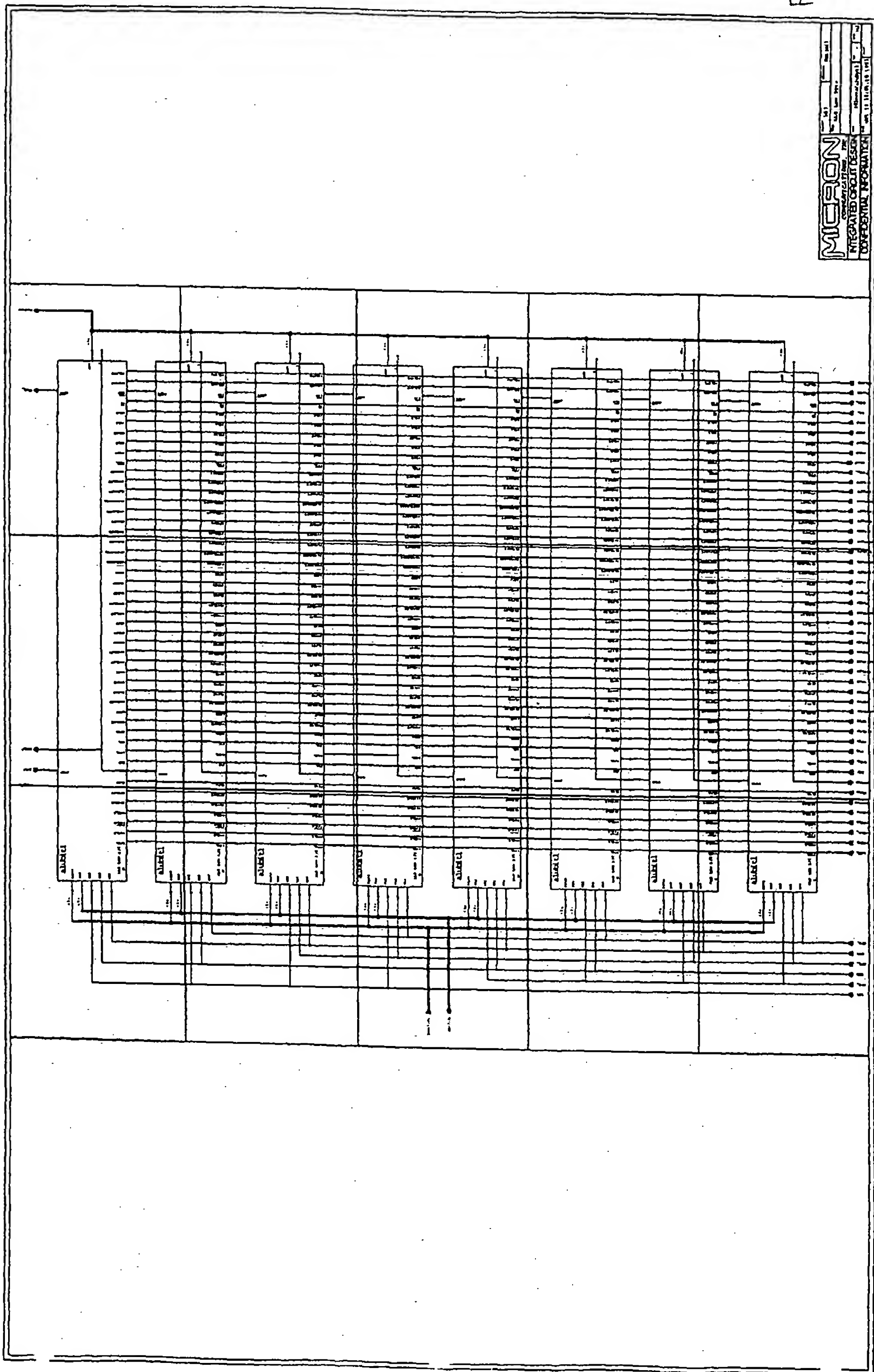


FIG. 7.0901

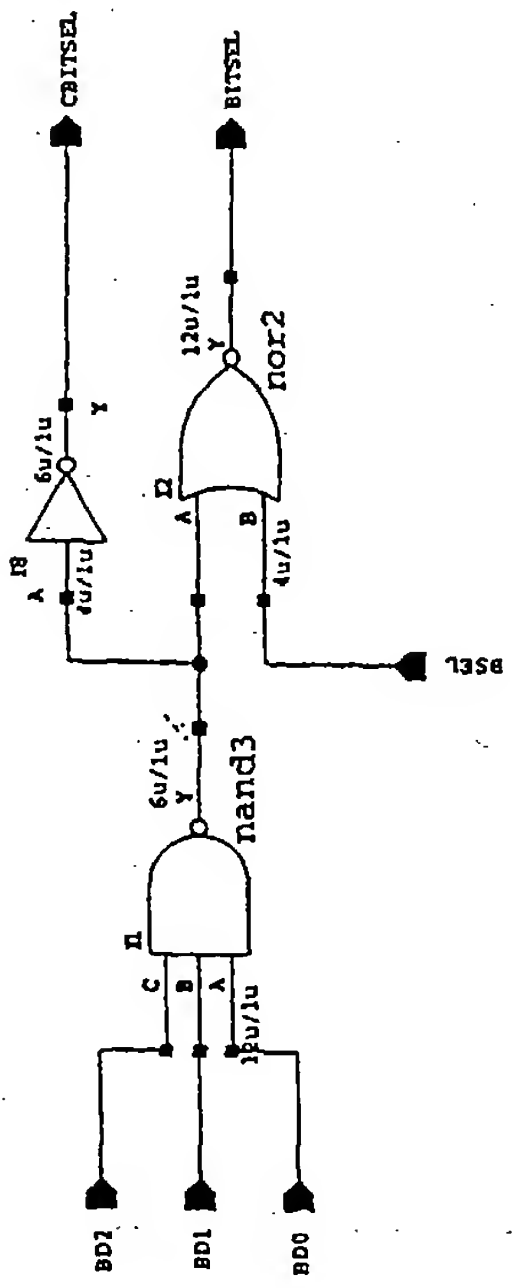




7.090101AA	7.090101AB	7.090101AC	7.090101AD
------------	------------	------------	------------

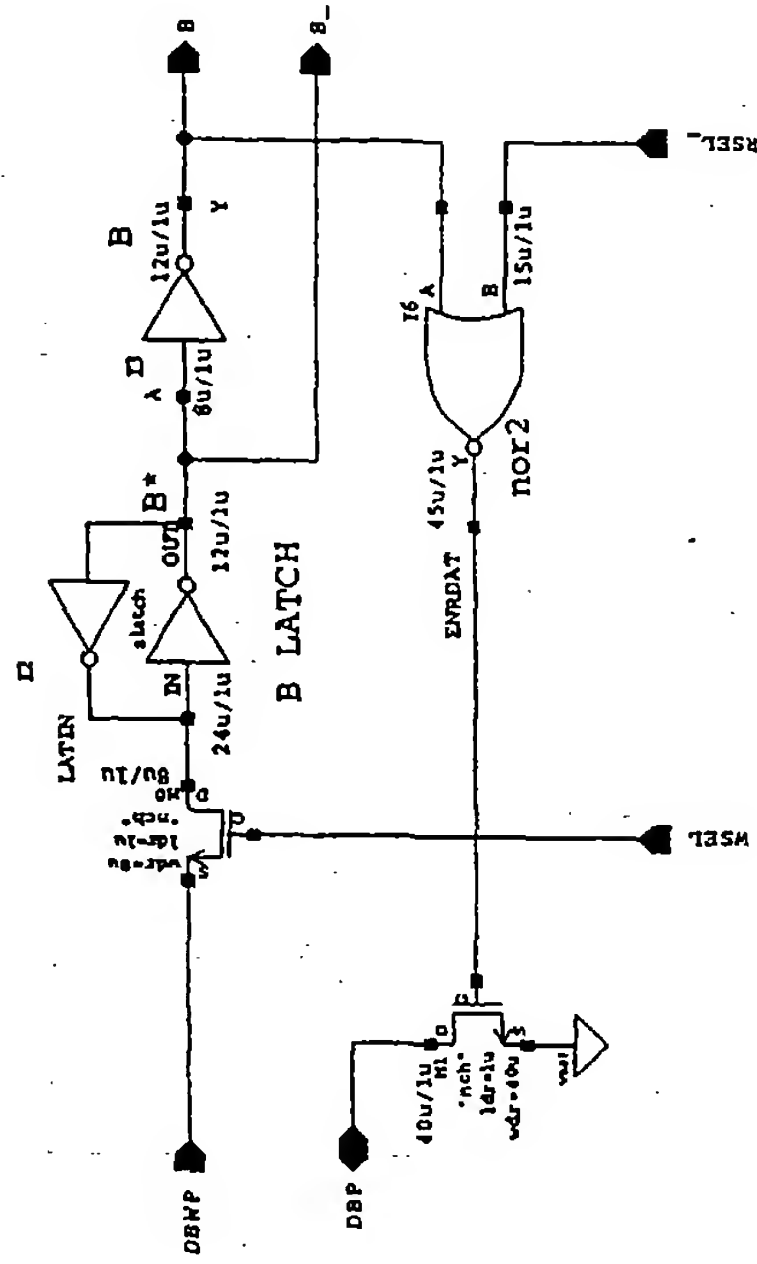
IL 11 03 11.09.01 11 11





<b>MICRON</b>		PROJECT: L03	DESIGNER: Rotzoll
COMMUNICATIONS, INC.		TITLE: ALU Bit Decoder Cell	
INTEGRATED CIRCUIT DESIGN		NOV: 103reva/alubdec	REV: -
CONFIDENTIAL INFORMATION		DATE: Sep 29 16:07:43 1993	SHEET: A

Fig. 7.09010101



PROJECT: L03		DESIGNER: Rotzoll	
TITLE: ALU B Register Cell			
NAME: 103reva/alubcell		REV: -	SIZE: A
DATE: Oct 1 15:32:35 1993		PAGE: 1	

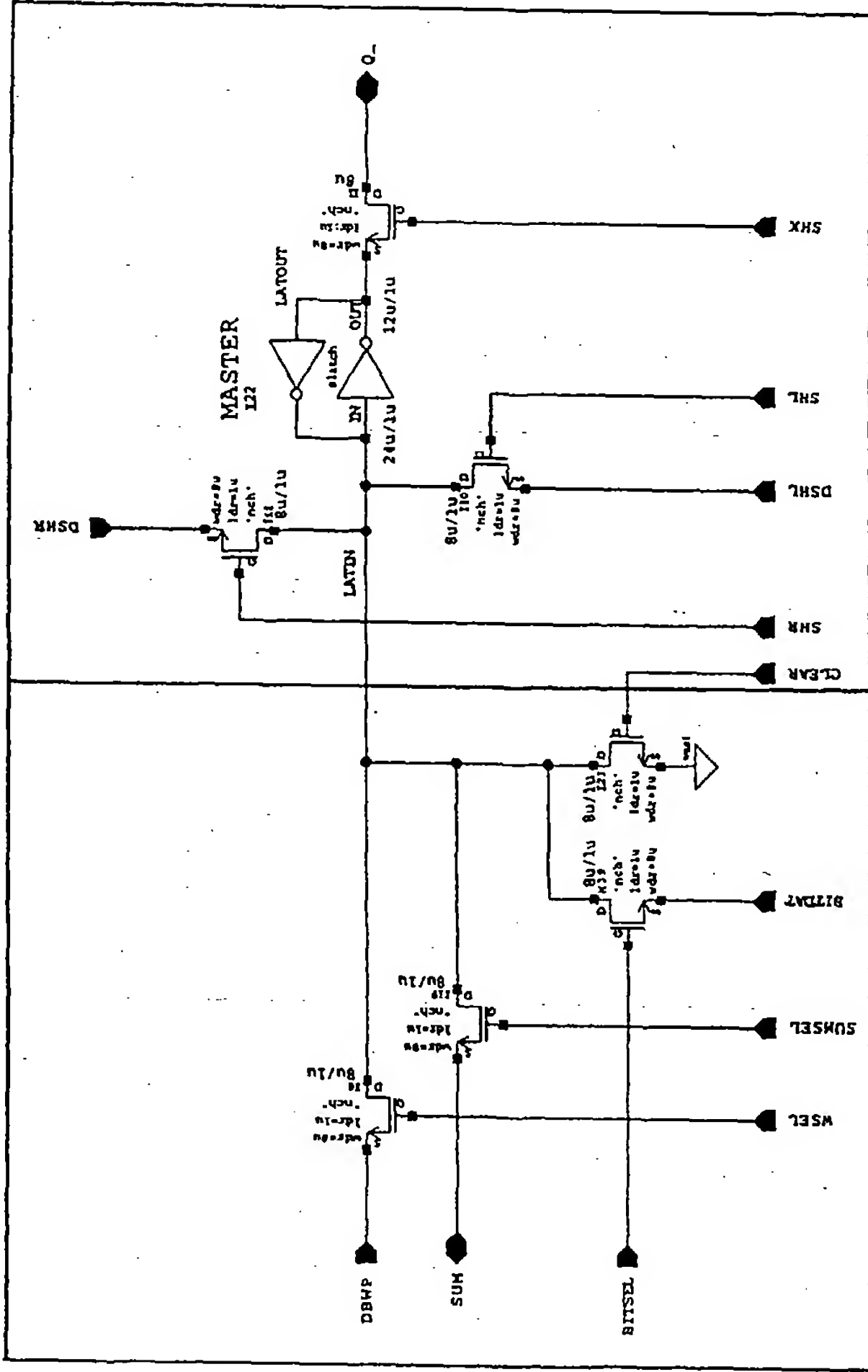
**MICRON**  
 COMMUNICATIONS, INC.  
 INTEGRATED CIRCUIT DESIGN  
 CONFIDENTIAL INFORMATION

Fig. 7.09010102

7.09010103AB

7.09010103AA

7.09010103



MICRON				COMMUNICATIONS, INC.	
INTEGRATED CIRCUIT DESIGN					
CONFIDENTIAL INFORMATION					
PROJECT: L03		DESIGNER: Rotzoll			
TITLE: ALU A Register Cell					
NAME: 103reva/aluacell		REV: -	ITER: A		
DATE: Oct 1 15:41:37 1993			PAGE: 1		

**MICRON**  
 COMMUNICATIONS, INC.  
 INTEGRATED CIRCUIT DESIGN  
 CONFIDENTIAL INFORMATION

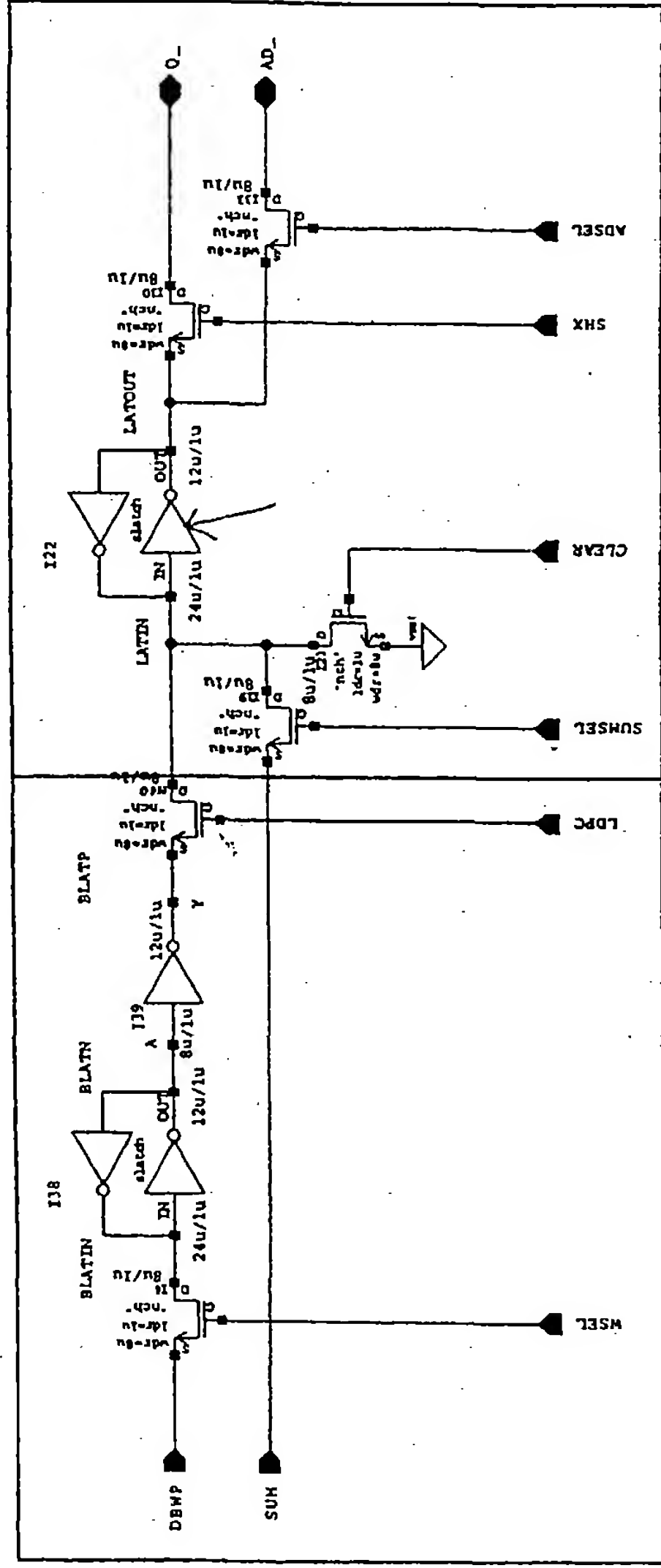
FIG. 7.09010103

7.09010104AB

7.09010104AA

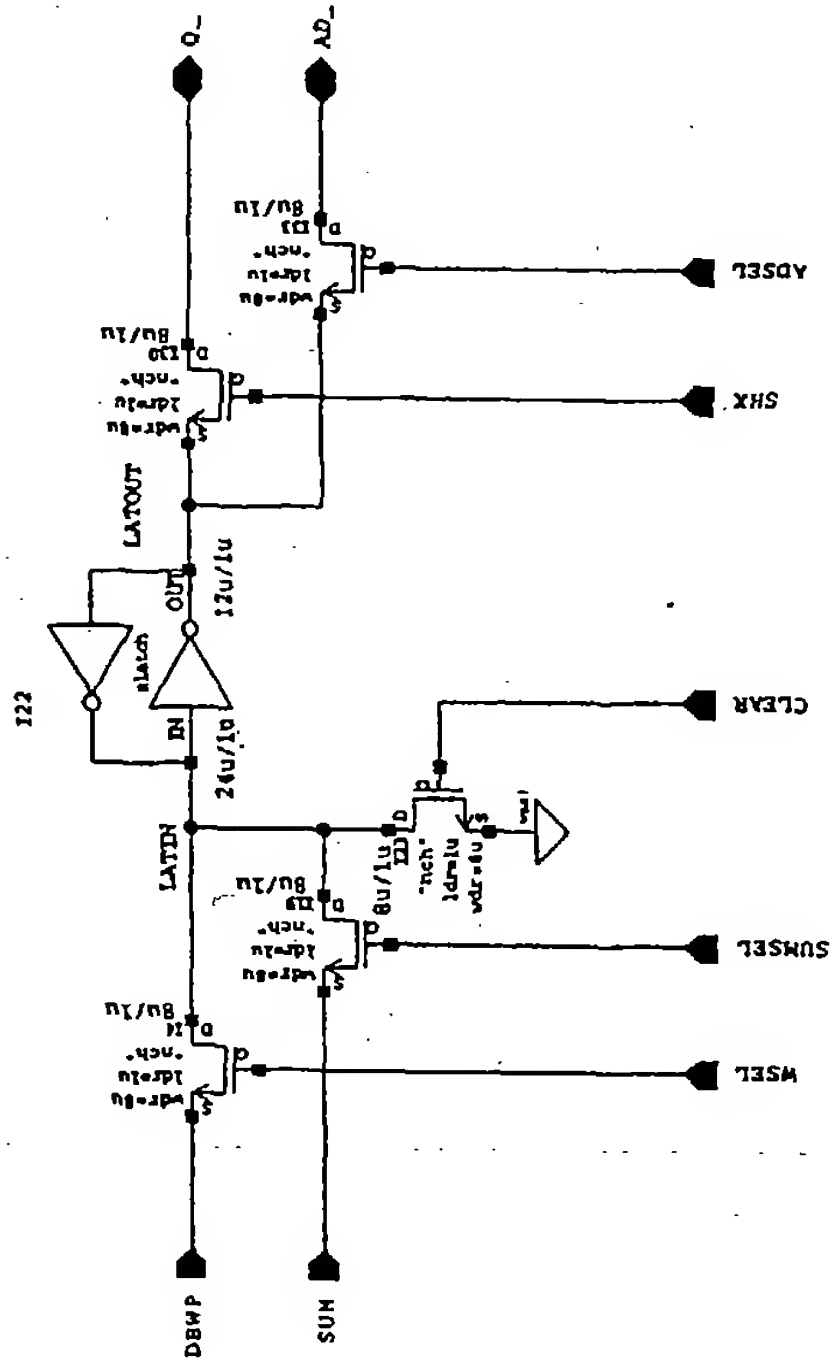
John Wiley & Sons

Fig. 7.0901010104



MICRON				PROJECT: L03		DESIGNER: Rotzoll			
COMMUNICATIONS, INC.				TITLE: ALU Register Cell					
NAME:				103reva/alupc		REV: -		SIZE: A	
DATE:				Oct 1 15:45:48 1993		SHEET:			
INTEGRATED CIRCUIT DESIGN									
CONFIDENTIAL INFORMATION									



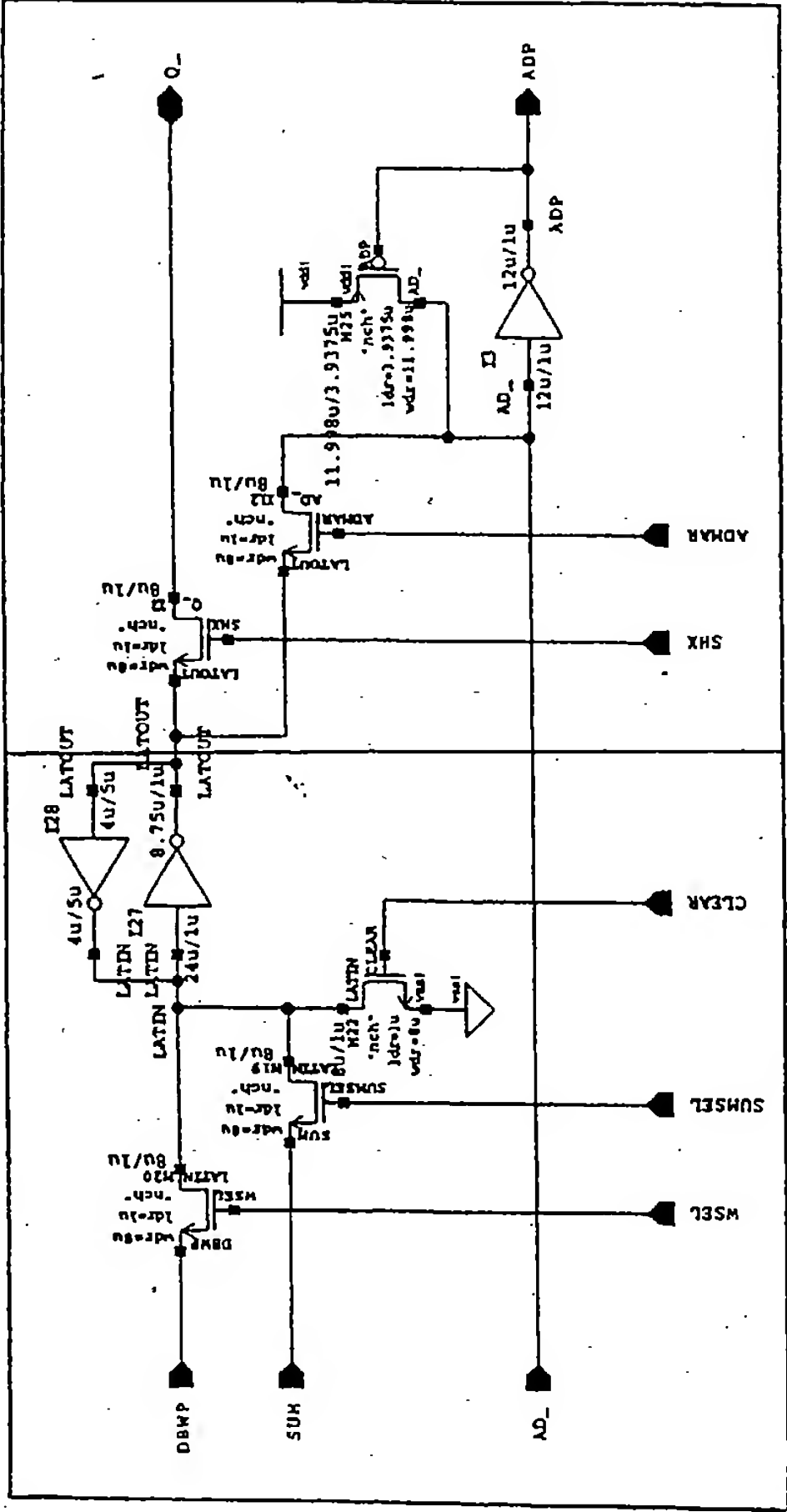


<b>MICRON</b>		PROJECT: L03	DESIGNER: Rotzoll
COMMUNICATIONS, INC.		TITLE: ALU Register Cell	
INTEGRATED CIRCUIT DESIGN		NAME: 103reva/alurcell	REV: -
CONFIDENTIAL INFORMATION		DATE: Oct 1 15:51:03 1993	SHEET: A

Fig. 7.09010105

7.09010106AA	7.09010106AB
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7.09010106



**MICRON**  
COMMUNICATIONS, INC.

INTEGRATED CIRCUIT DESIGN  
CONFIDENTIAL INFORMATION

PROJECT: L03

DESIGNER: JOTOOLE

TITLE: ALU Memory Address Register

NOV: 103reva/alumar

REV: B8

DATE: Jan 4 10:27:28 1996

SIZE: A

B8: added pch feedback device

FIG. 7.09010106



7.09010108AA	7.09010108AB	7.09010108AC
7.09010108BA	7.09010108BB	7.09010108BC

7.09010108BB

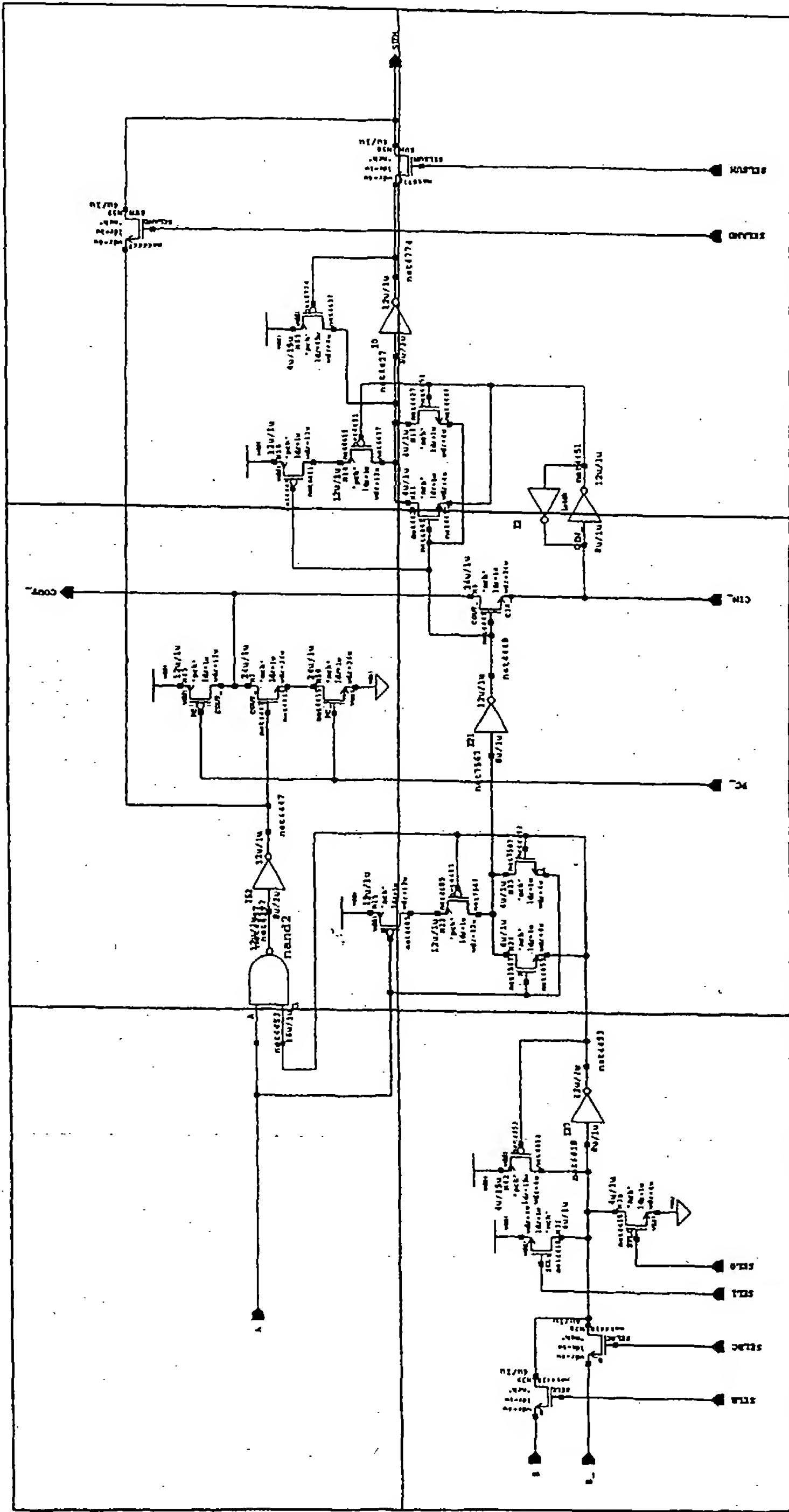


Fig. 7.09010108

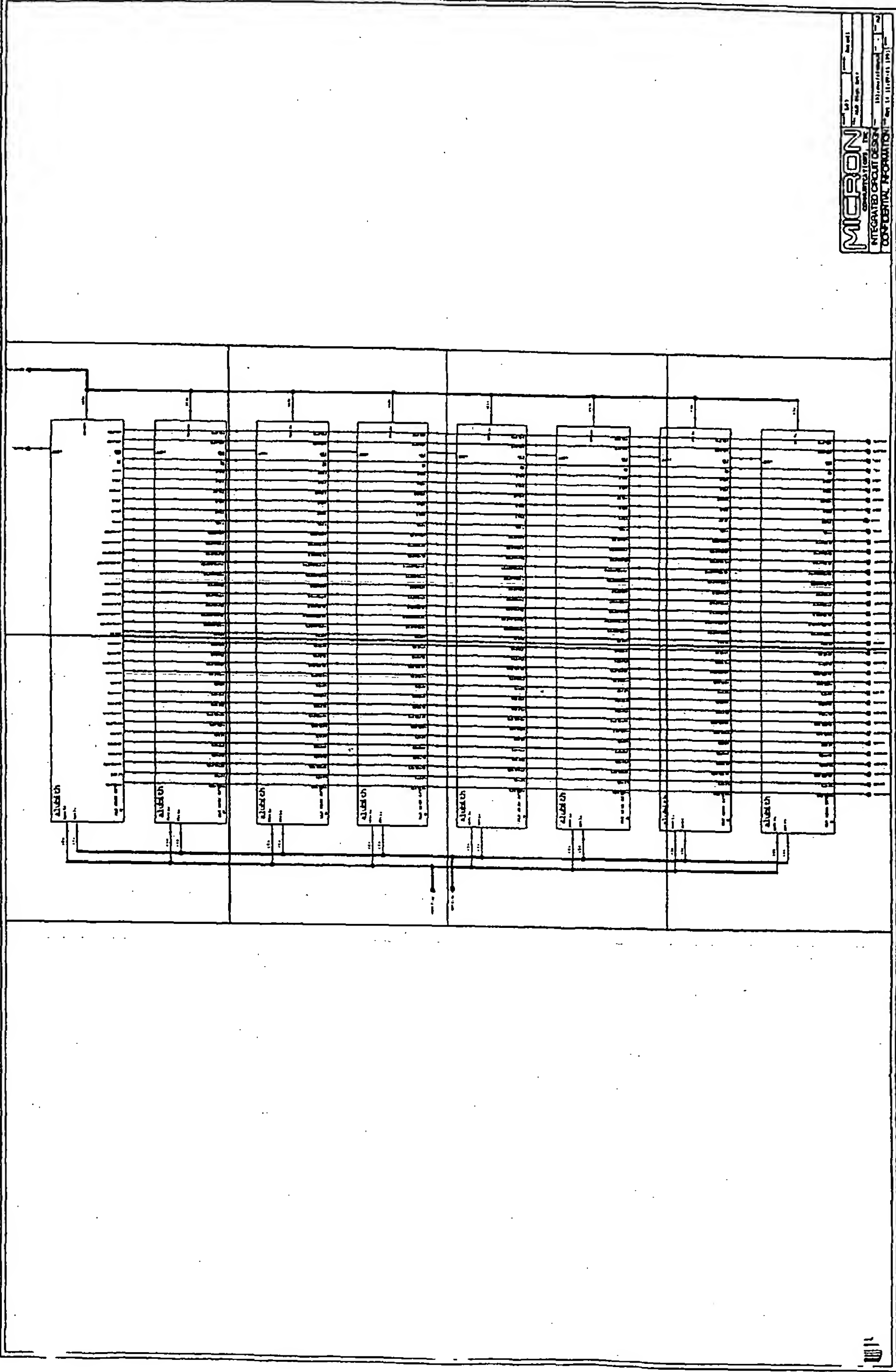
B5: move feedback device from I21 to I27

MICRON		PROJECT: L03	REVISION: J0700LE
COMMUNICATIONS, INC.		THE ALU Adder	
INTEGRATED CIRCUIT DESIGN		PART: 103revs/aluadd	REV: B5
CONFIDENTIAL INFORMATION		DATE: Sep 16 15:48:21 1995	

7.0902AA	7.0902AB	7.0902AC	7.0902AD
7.0902BA	7.0902BB	7.0902BC	7.0902BD

ENCLOSURE

Fig. 7.0902



**MICRON**  
INTEGRATED CIRCUIT DESIGN  
CORPORATION  
13110 NE 15TH AVE.  
SHANE, OR 97132  
TEL: (503) 261-1000  
FAX: (503) 261-1001



7.090201AA	7.090201AB	7.090201AC
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EX 7.090201

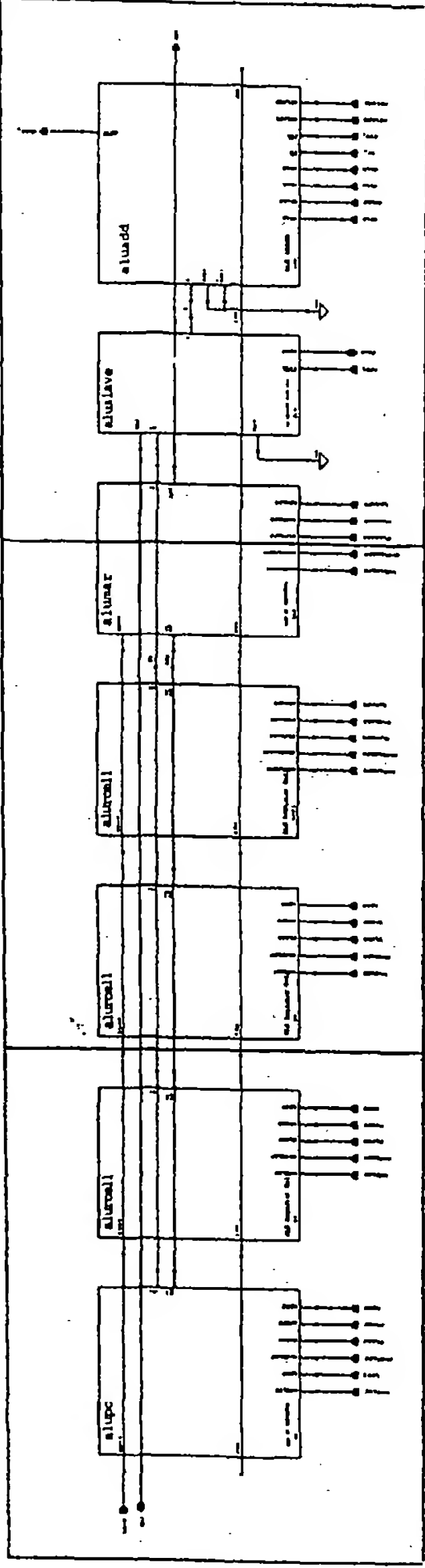
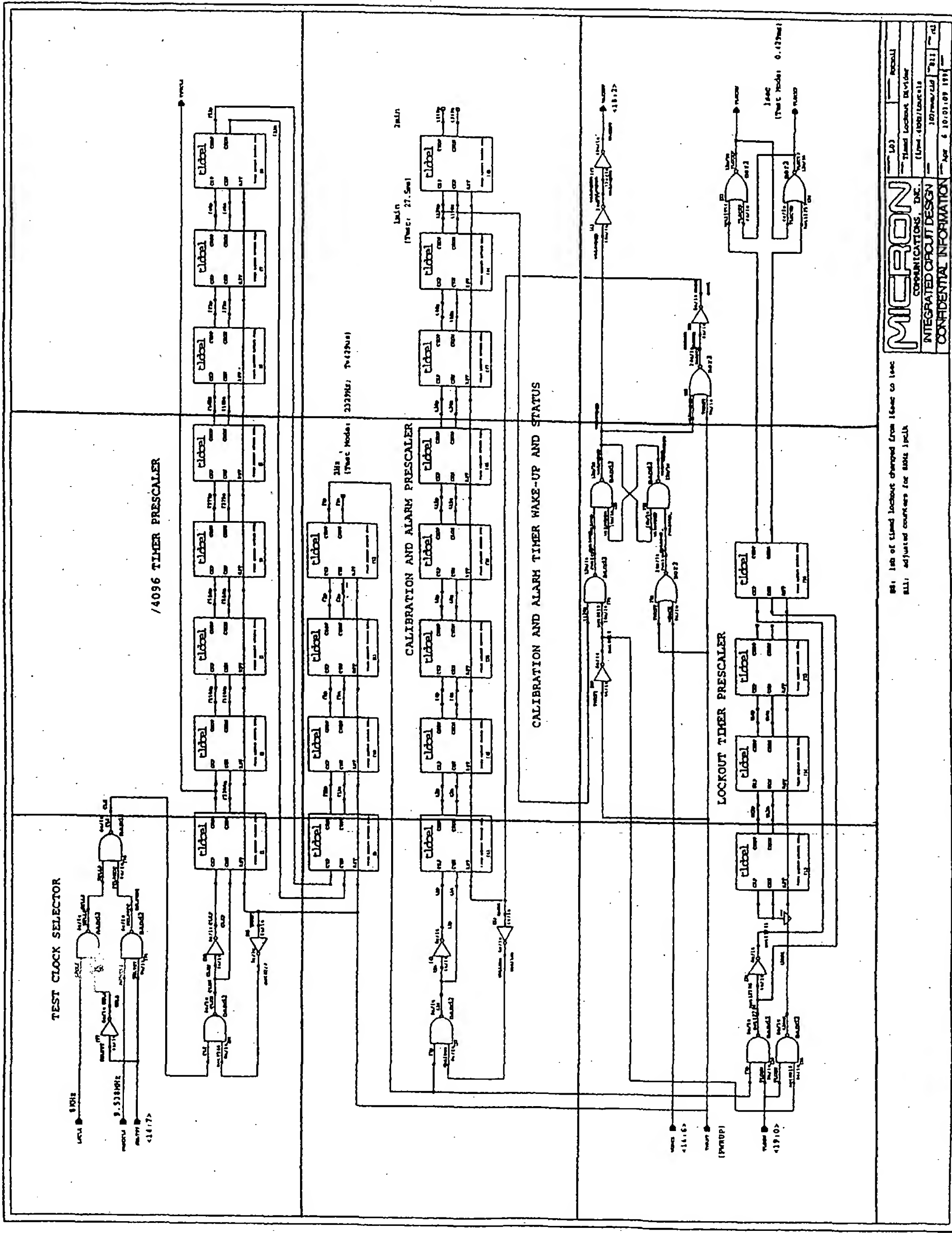
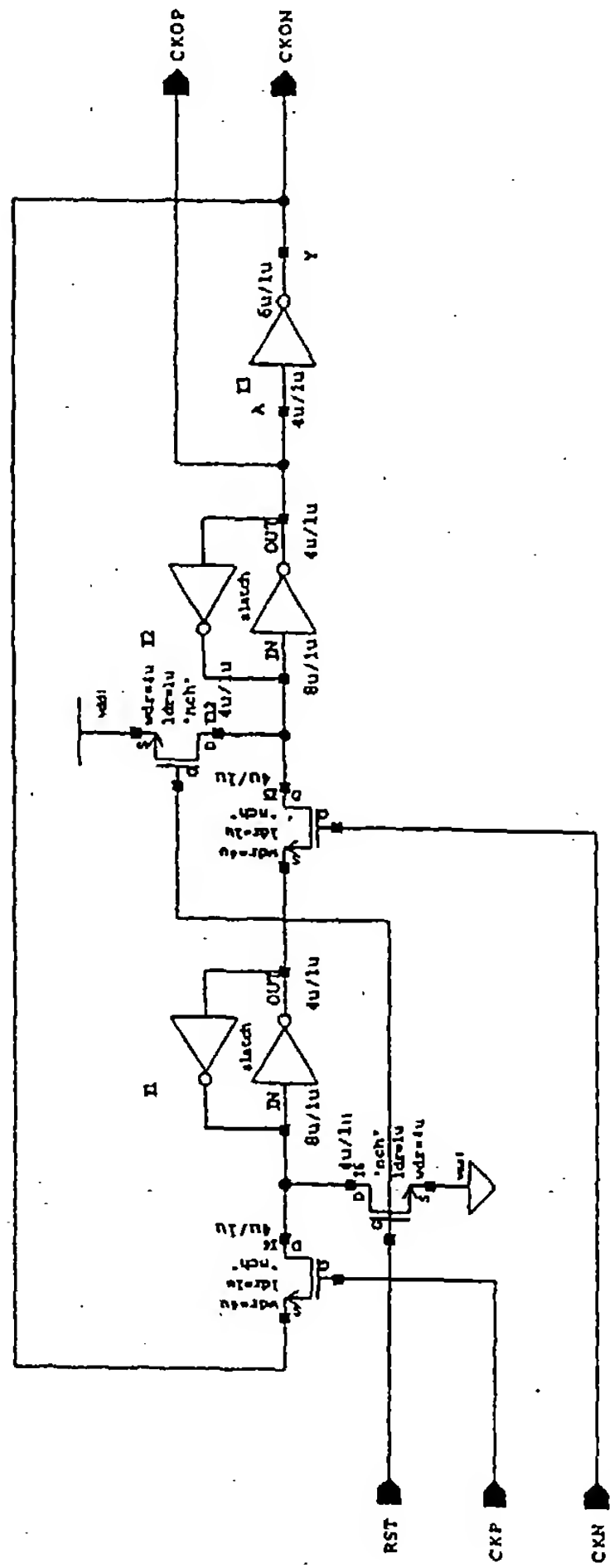


FIG. 7.090201



Fig. 7.10





12/29/92

PROJECT: L03		DESIGNER: Rotzoll	
TITLE: Timed Lockout Divider Cell			
NAME: 103reva/tl4cel		REV: A	
DATE: Sep 22 15:26:56 1994		SHEET: A	

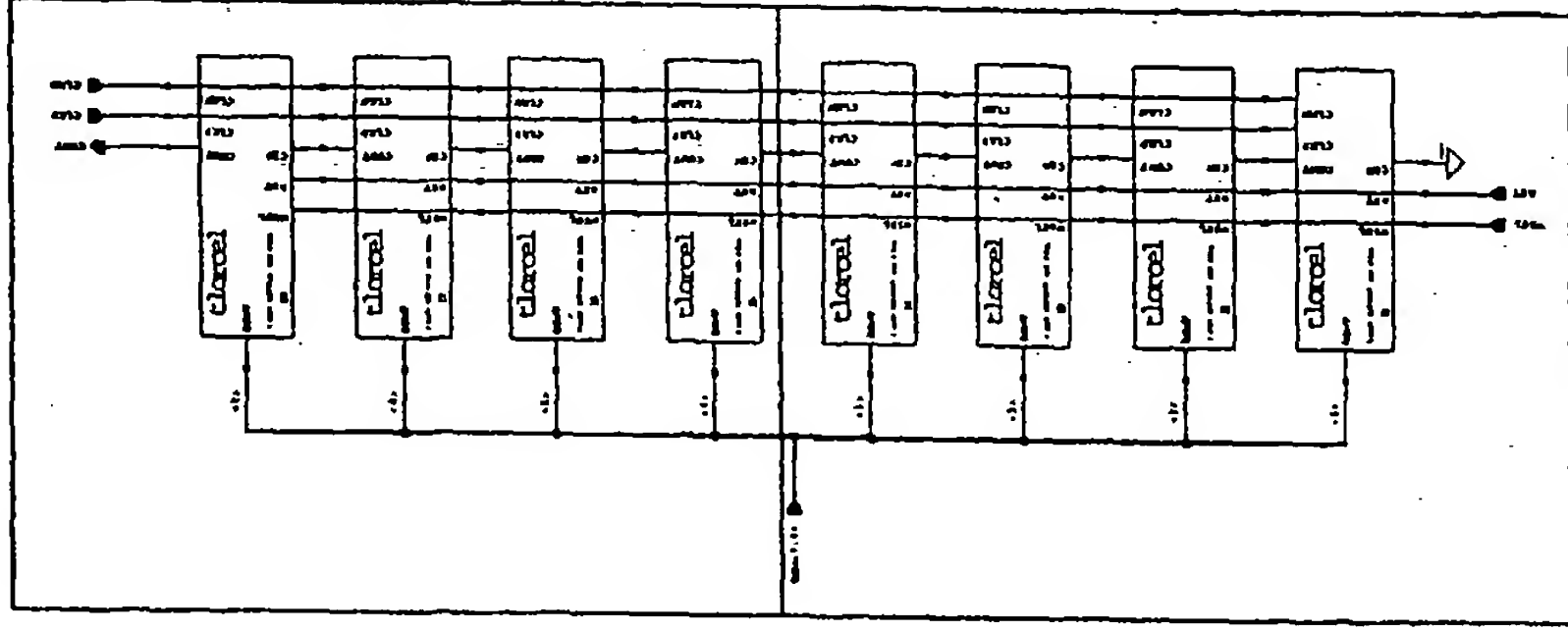
**MICRON**  
 COMMUNICATIONS, INC.  
 INTEGRATED CIRCUIT DESIGN  
 CONFIDENTIAL INFORMATION

Fig. 7.1001

<p>7.11AA</p>	<p>7.11AB</p>
---------------	---------------

II II II II

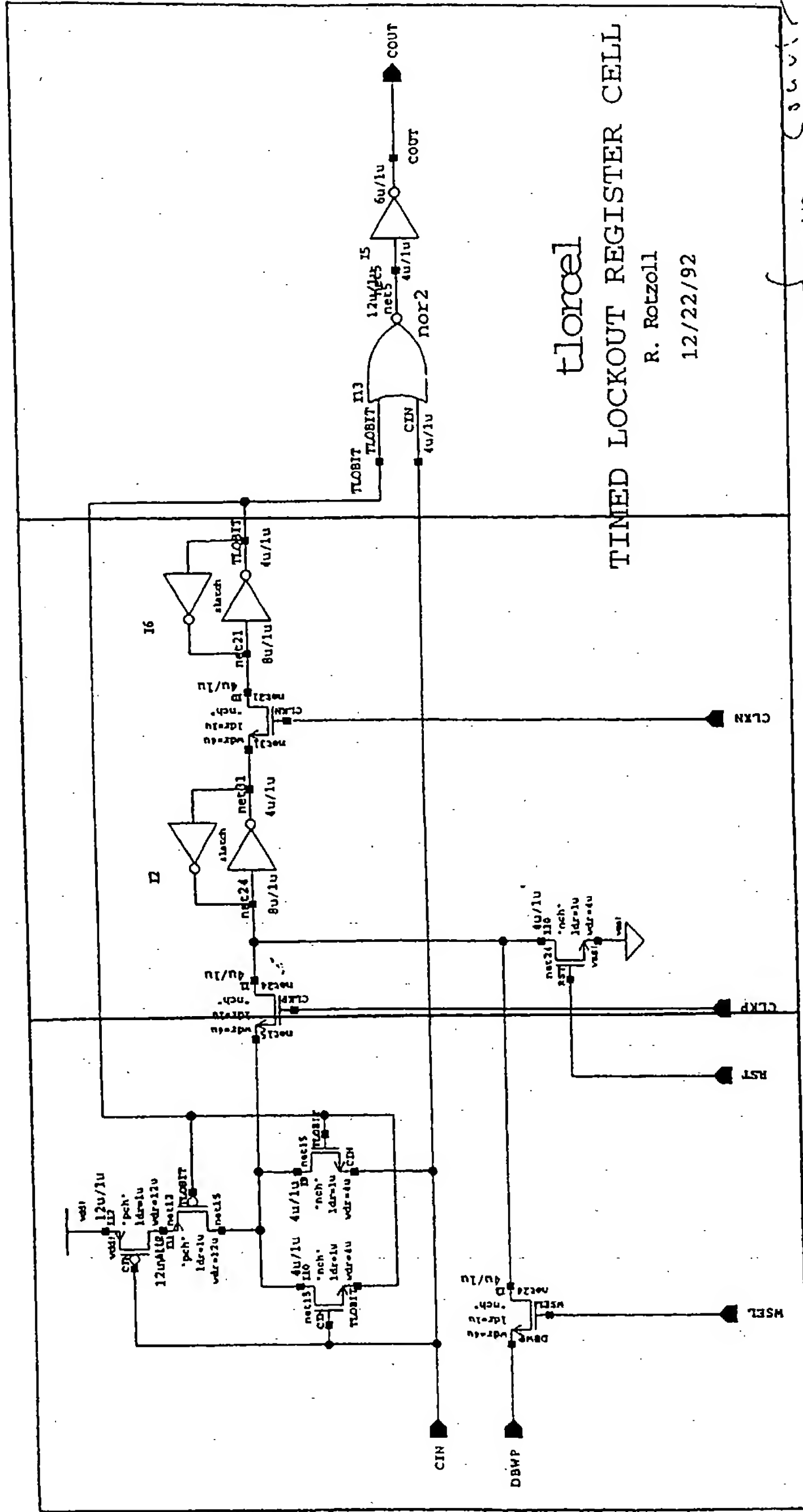
FIG. 7.11



7.1101AA	7.1101AB	7.1101AC
----------	----------	----------

II II 007 7.1101AB 7.1101AC





down counter

FIG. 7.1101

7.12AA	7.12AB	7.12AC
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EX-112

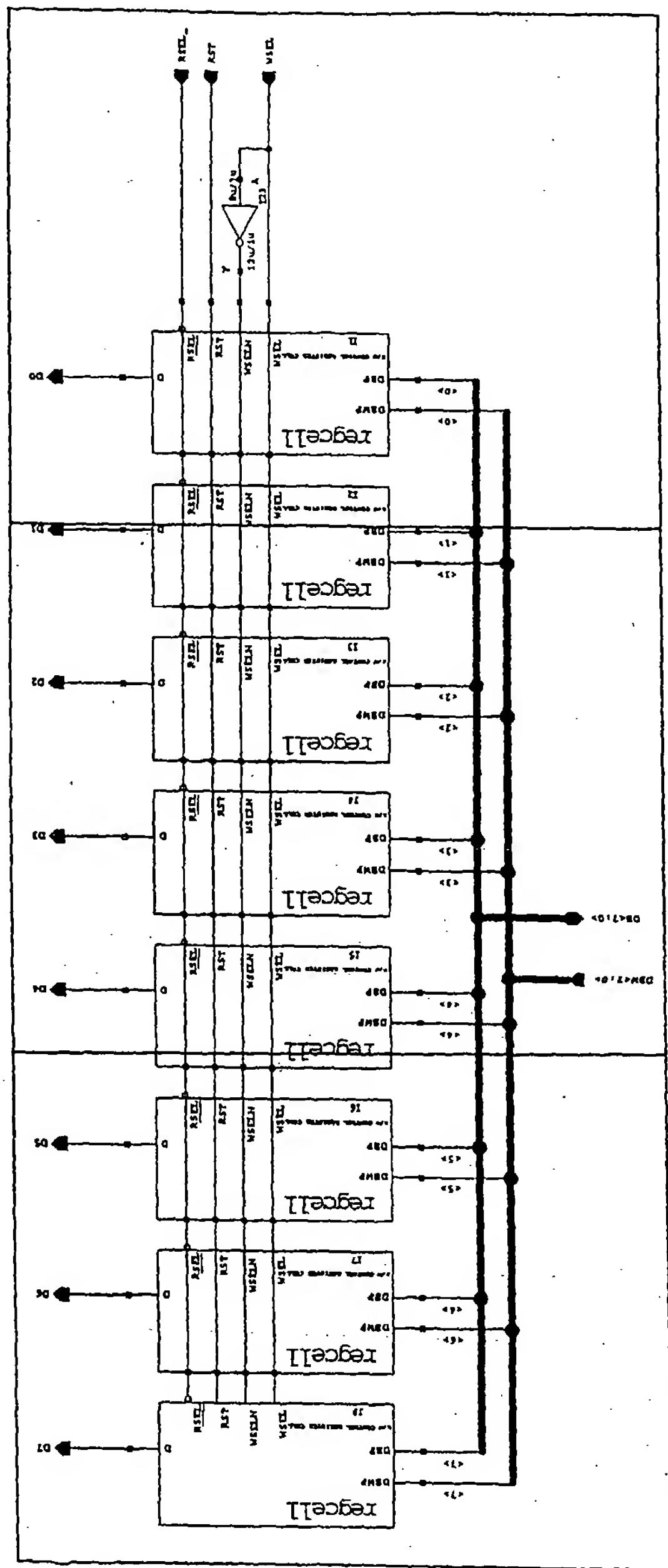
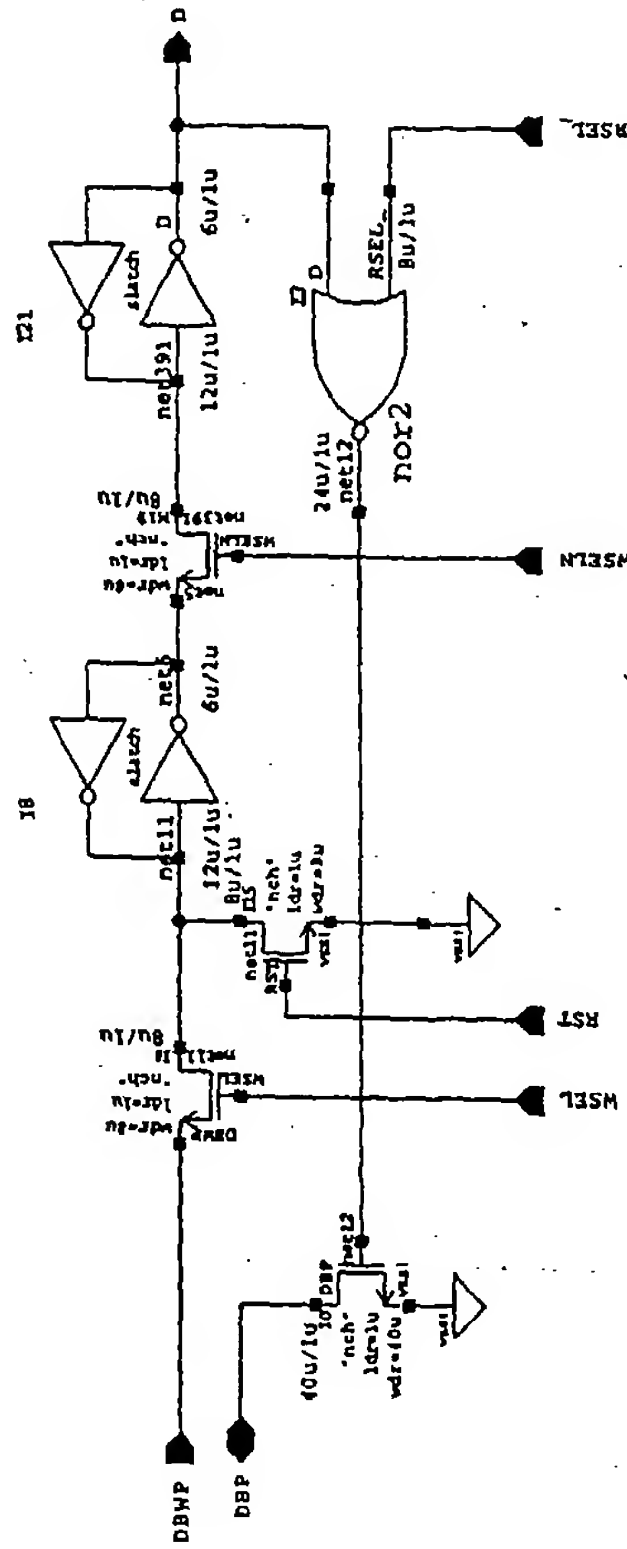


Fig. 7.12

MICRON	PRODUCT: L03	DESIGN: Rotzoll
	TYPE: R/W Control Register	
	DATE: 103xeva/oreg	REV: 1
	CONFIDENTIAL INFORMATION	

Nov 12 09:44:40 1993

Fig. 7.1201



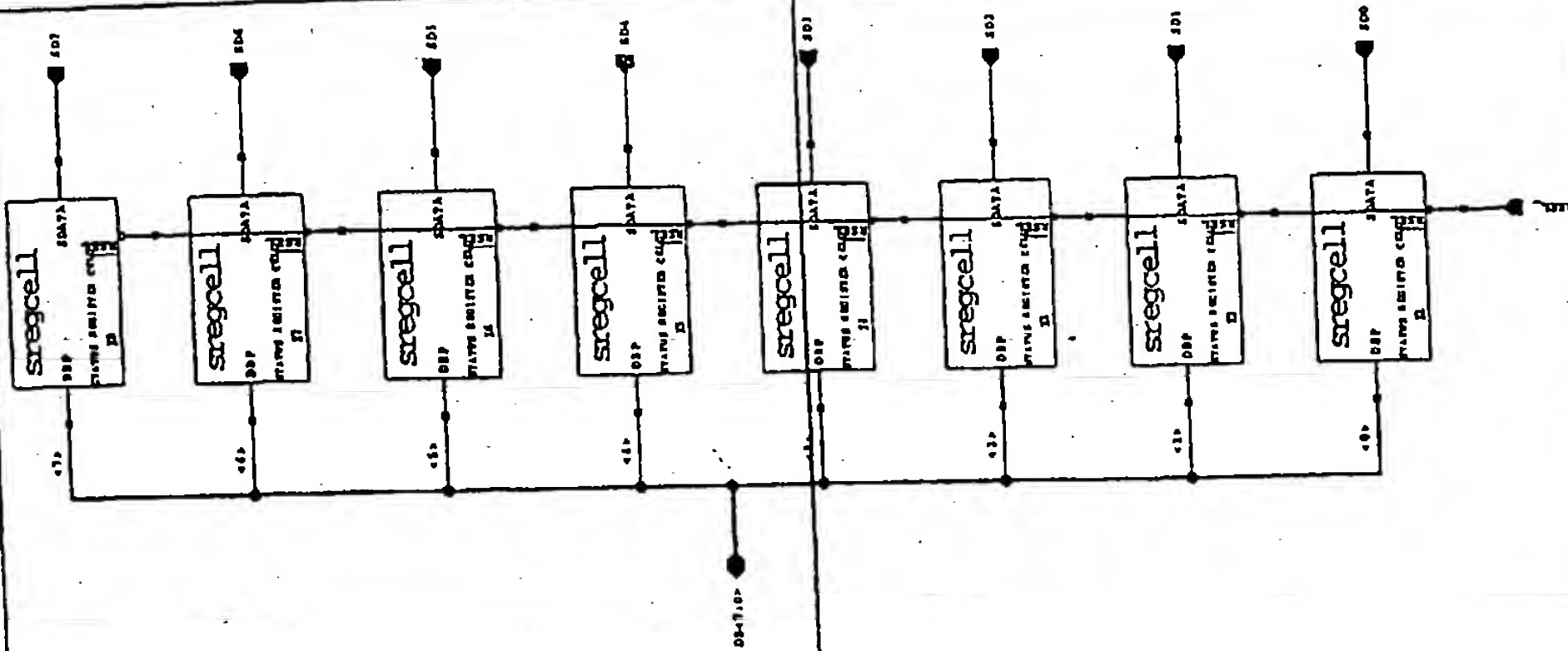
PROJECT: L03		DESIGNER: Rotzoll	
TITLE: R/W Control Register Cell			
NAME: 103reva/regcell		REV: ~	SIZE: A
DATE: Nov 12 09:41:36 1993		SHEET: 1	

**MICRON**  
COMMUNICATIONS, INC.  
INTEGRATED CIRCUIT DESIGN  
CONFIDENTIAL INFORMATION

7.13AA

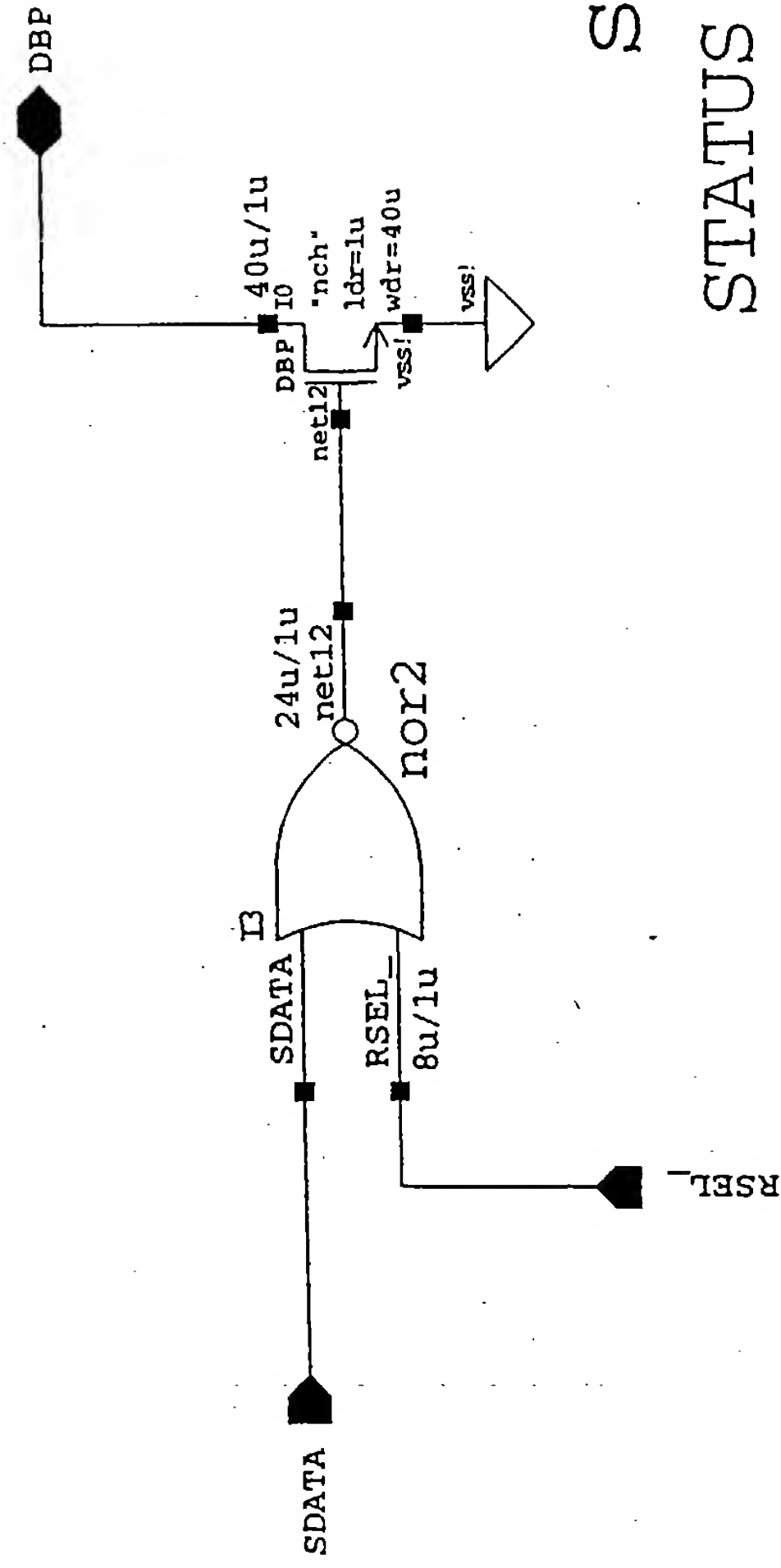
7.13BA

7.13



<b>MICRON</b>		REV. 1.03	DESIGN: Rockwell
COMMUNICATIONS, INC.		TITLE: Status Register	
INTEGRATED CIRCUIT DESIGN		DATE: 10/revs/step	REV: 1
CONFIDENTIAL INFORMATION		DATE: Oct 1 14:49:00 1993	USER:

FIG. 7.13



# sregcell

## STATUS REGISTER CELL

R. Rotzoll

12/8/92

FIG. 7.1301

7.14AA	7.14AB
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II II II 7.14



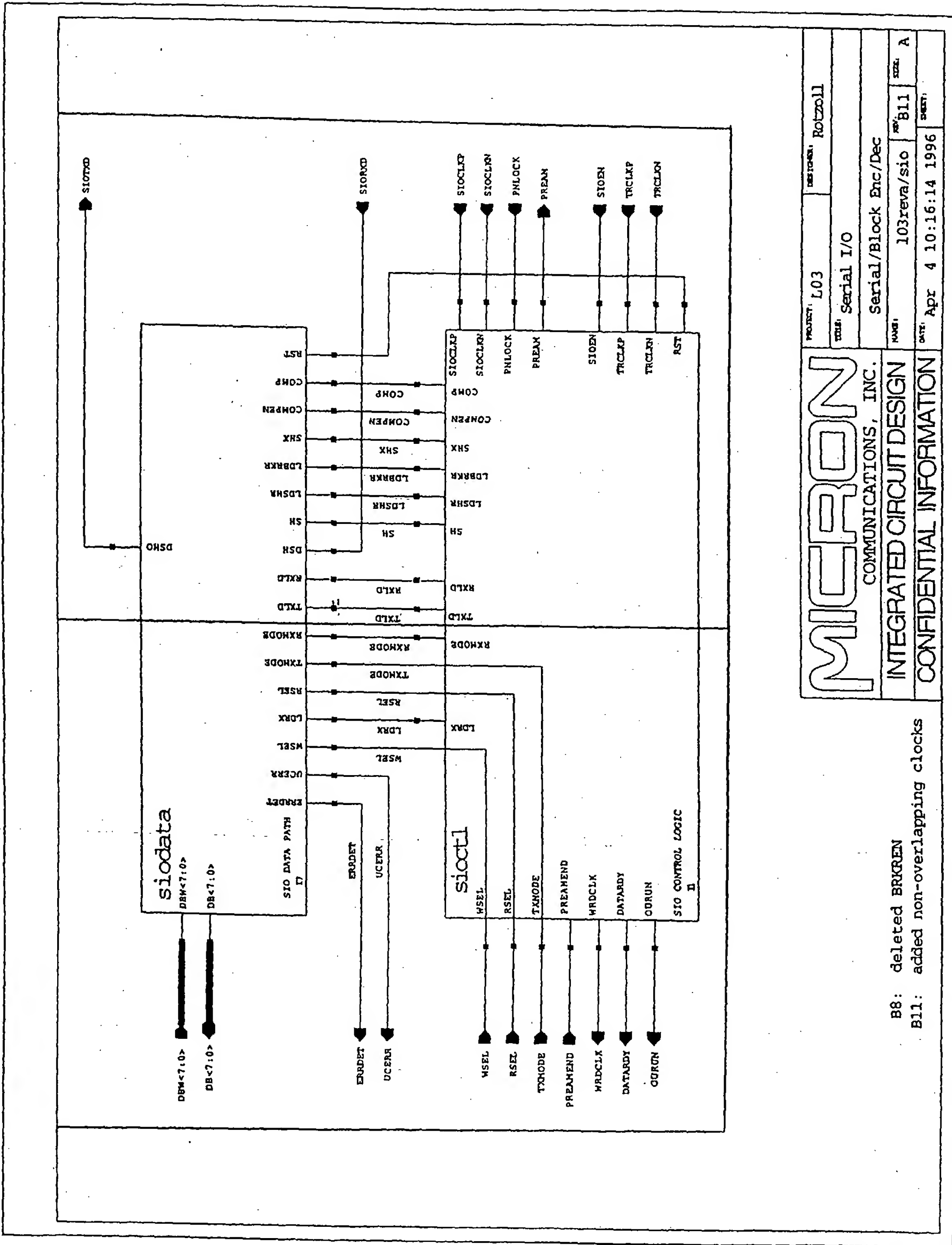


Fig. 7.14

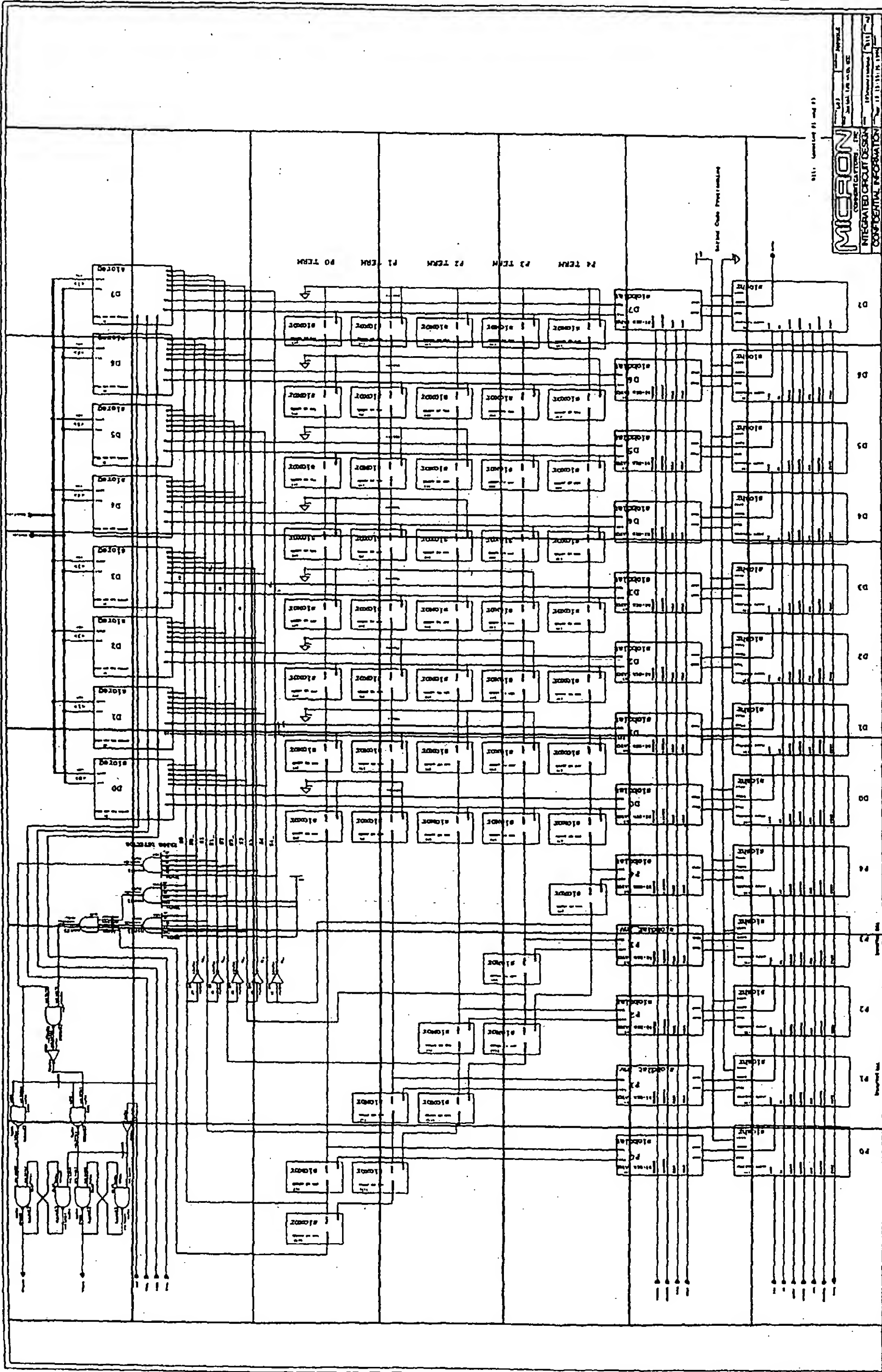
PROJECT: L03		DESIGNER: Rotzoll	
TITLE: Serial I/O		Serial/Block Enc/Dec	
NAME:	103reva/sio	REV: B11	SIZE: A
DATE:	Apr 4 10:16:14 1996	SHEET:	

**MICRON**  
 COMMUNICATIONS, INC.  
 INTEGRATED CIRCUIT DESIGN  
 CONFIDENTIAL INFORMATION

7.1401AA	7.1401AB	7.1401AC	7.1401AD	7.1401AE	7.1401AF
7.1401BA	7.1401BB	7.1401BC	7.1401BD	7.1401BE	7.1401BF
7.1401CA	7.1401CB	7.1401CC	7.1401CD	7.1401CE	7.1401CF
7.1401DA	7.1401DB	7.1401DC	7.1401DD	7.1401DE	7.1401DF
7.1401EA	7.1401EB	7.1401EC	7.1401ED	7.1401EE	7.1401EF
7.1401FA	7.1401FB	7.1401FC	7.1401FD	7.1401FE	7.1401FF
7.1401GA	7.1401GB	7.1401GC	7.1401GD	7.1401GE	7.1401GF

II II III IV V VI VII VIII

Fig. 71401



7.140101AB	7.140101AA
------------	------------

II II II II II II



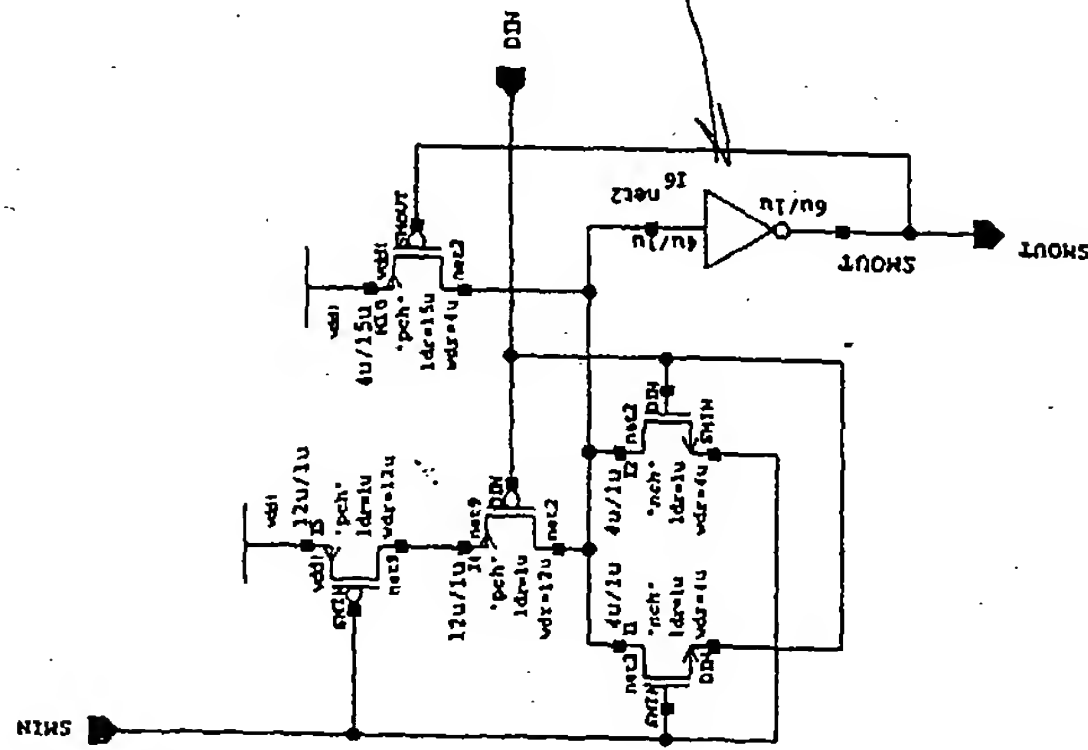


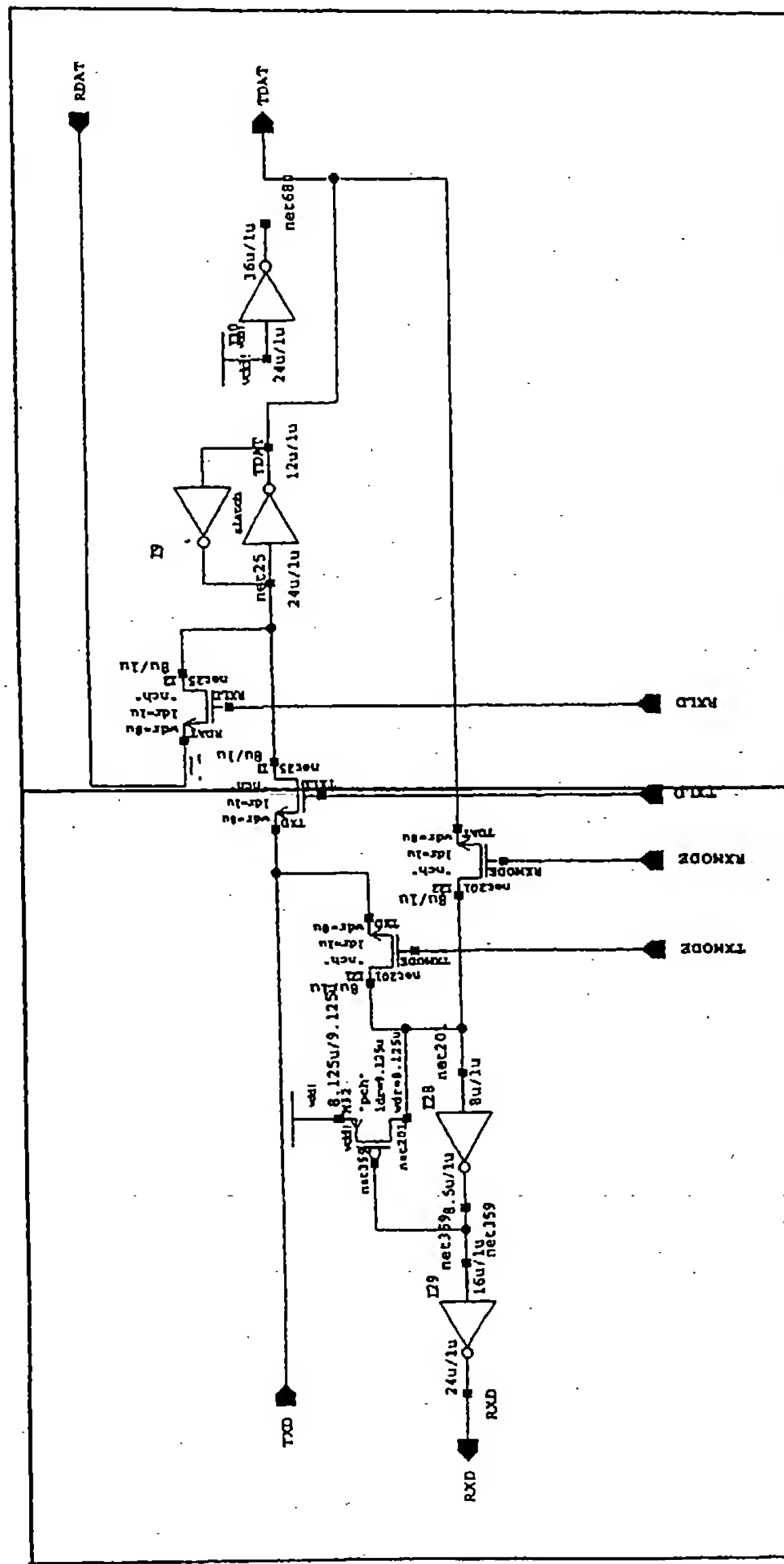
Fig. 7.140102

PROJECT: L03		DESIGNER: JOTOOLE	
TITLE: SIO XOR			
NAME: 103reva/sioxor		REV: B1	FILE: A
DATE: Sep 1 18:07:22 1994		SHEET:	

**MICRON**  
COMMUNICATIONS, INC.  
INTEGRATED CIRCUIT DESIGN  
CONFIDENTIAL INFORMATION

7.140103AA	7.140103AB
------------	------------

7.140103AA 7.140103AB



B11: inverted bit

# NIFFON COMMUNICATIONS, INC.

COMMUNICATIONS, INC.

# INTEGRATED CIRCUIT DESIGN

CONFIDENTIAL INFORMATION

PROJECT: 1.03	DESIGN: JOTOOLE
---------------	-----------------

**DESIGN, JOTOOLE**

STO Bidirectional Latch

NAME	103reva/siobdlat_inv	REV	B11	SIZE	A
------	----------------------	-----	-----	------	---

11	ALL A
----	-------

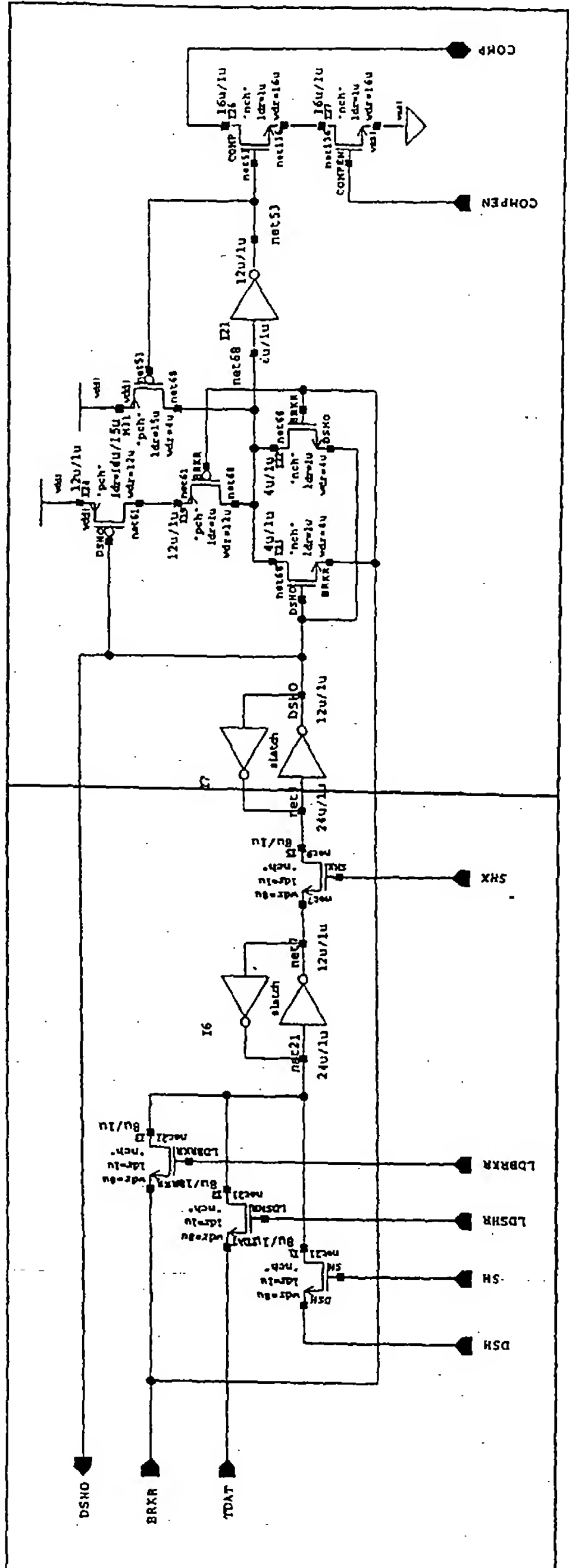
**A**

DATE:	APR 10 15:13:59 1996	9-03-97:
-------	----------------------	----------

**EST:**







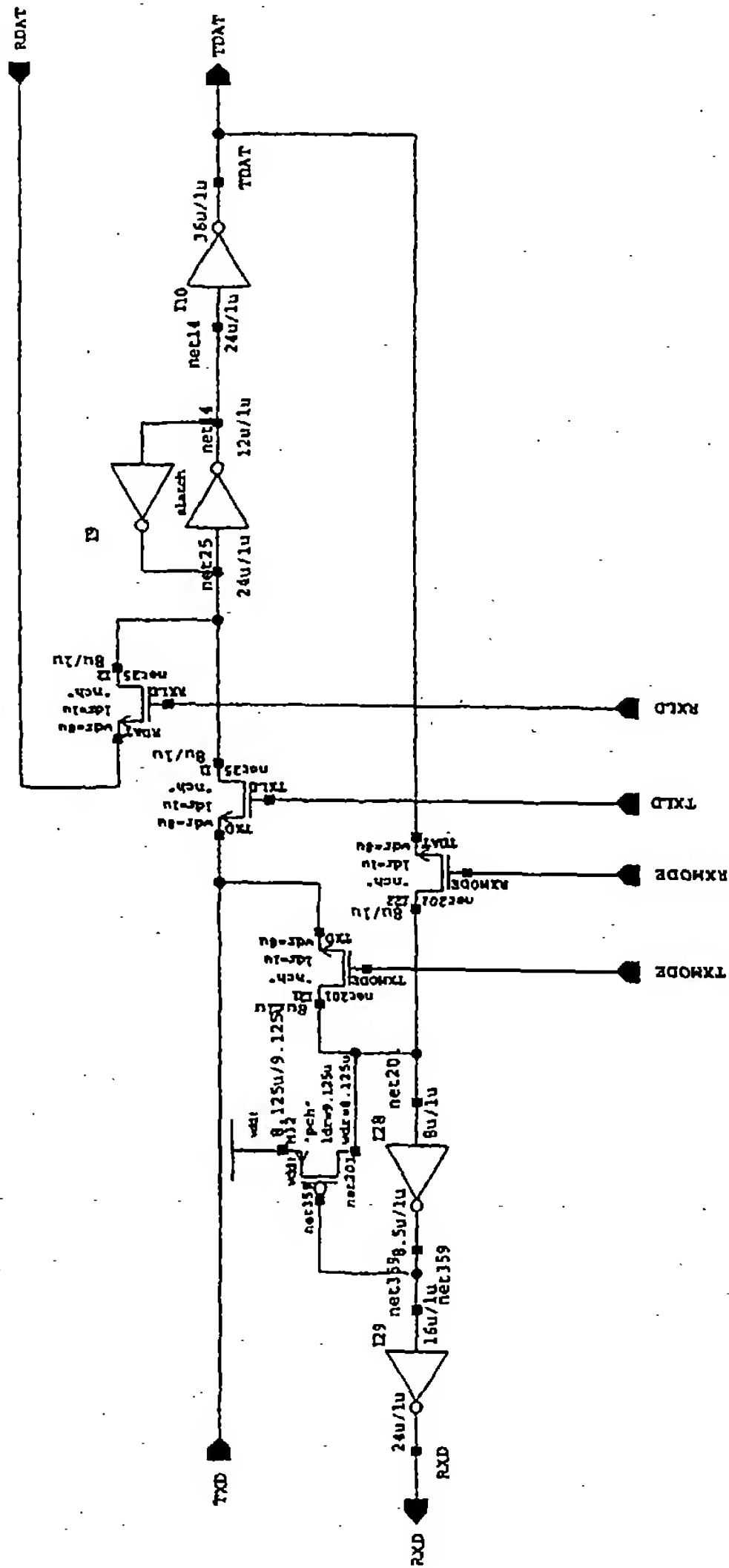
7.1e0104  
FIG. 7.140004

PROJECT: L03		SECTION: JOTOOLE	
TITLE: SIO Shift Register			
NAME: 103reva/sioshr		REV: B1	SHEET: A
DATE: Sep 2 08:06:26 1994		SHEET: 1	

**MICRON**  
COMMUNICATIONS, INC.  
INTEGRATED CIRCUIT DESIGN  
CONFIDENTIAL INFORMATION

7.140105AA	7.140105AB
------------	------------

SECRET



**MICRON**  
COMMUNICATIONS, INC.  
INTEGRATED CIRCUIT DESIGN  
CONFIDENTIAL INFORMATION

PROJECT: L03	DESIGNER: JOTOOLE
TITLE: SIO Bidirectional Latch	
NAME: 103reva/slobdlat	REV: B8
DATE: Jan 8 11:04:57 1996	SHEET: A

B8: added feedback device

Fig. 7.140105

	7.1402AC	7.1402AD	7.1402AE	7.1402AF	7.1402AG	7.1402AH	7.1402AI
7.1402BA	7.1402BB	7.1402BC	7.1402BD	7.1402BE	7.1402BF	7.1402BH	7.1402BI
7.1402CA	7.1402CB	7.1402CC	7.1402CD	7.1402CE	7.1402CF	7.1402CH	7.1402CI
7.1402DA	7.1402DB	7.1402DC	7.1402DD	7.1402DE	7.1402DF	7.1402DH	7.1402DI
7.1402EA	7.1402EB	7.1402EC	7.1402ED	7.1402EE	7.1402EF	7.1402EH	7.1402EI

II II II II II II II II

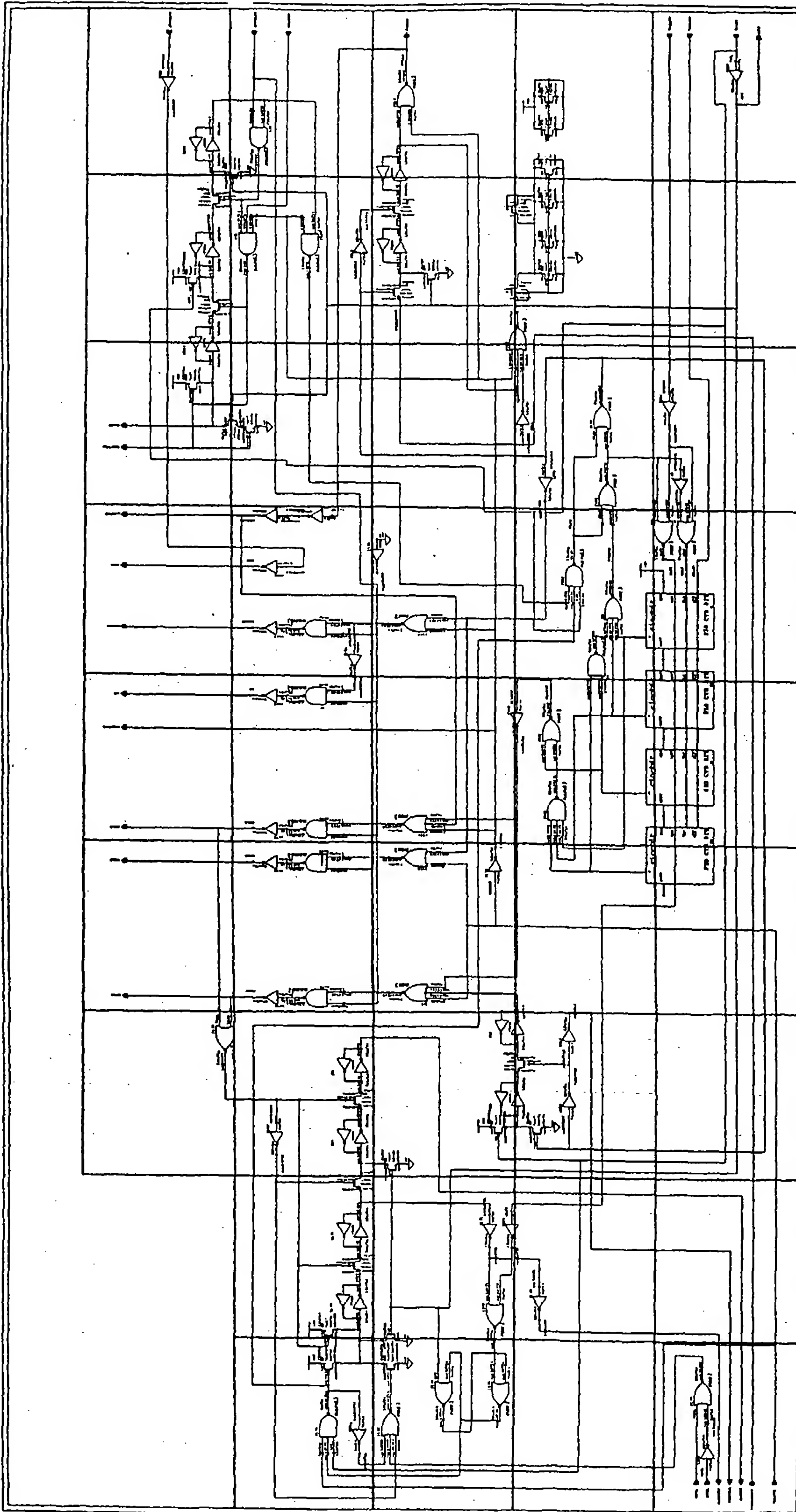


Fig. 7.1A02

NOT: added input to pin 10  
 added input to pin 11  
 added input to pin 12  
 added input to pin 13  
 added input to pin 14  
 added input to pin 15  
 added input to pin 16  
 added input to pin 17  
 added input to pin 18  
 added input to pin 19  
 added input to pin 20  
 added input to pin 21  
 added input to pin 22  
 added input to pin 23  
 added input to pin 24  
 added input to pin 25  
 added input to pin 26  
 added input to pin 27  
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 added input to pin 29  
 added input to pin 30  
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 added input to pin 82  
 added input to pin 83  
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 added input to pin 85  
 added input to pin 86  
 added input to pin 87  
 added input to pin 88  
 added input to pin 89  
 added input to pin 90  
 added input to pin 91  
 added input to pin 92  
 added input to pin 93  
 added input to pin 94  
 added input to pin 95  
 added input to pin 96  
 added input to pin 97  
 added input to pin 98  
 added input to pin 99  
 added input to pin 100

7.140201AB

7.140201AA

ИЗДАТЕЛЬСТВО

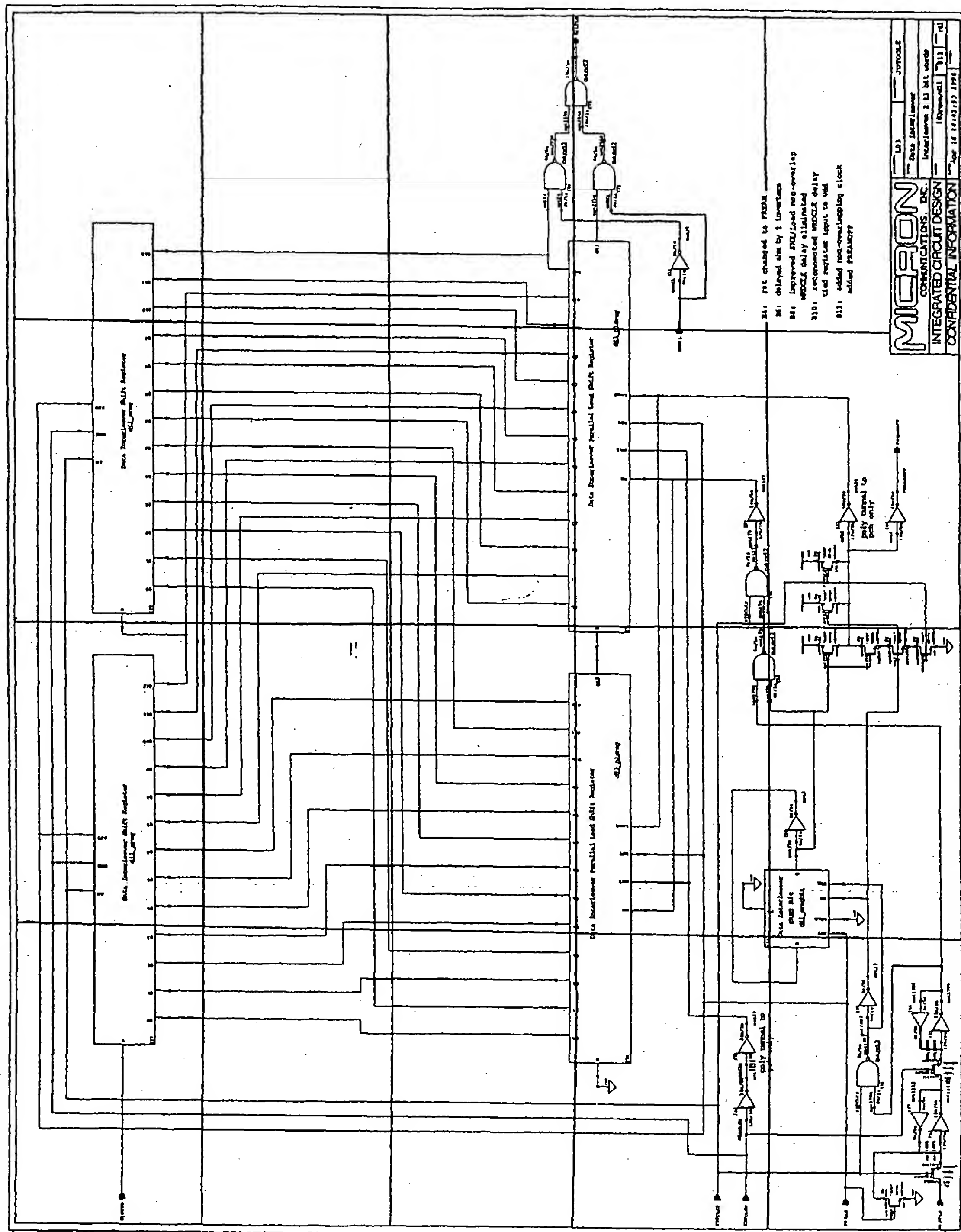


FIG. 7.190 ~~102~~





Fig. 7.15



- 21: 1st changed to P100
- 22: Improved 2nd/3rd non-overlap
- 23: 2nd/3rd delay eliminated
- 210: reconnected 2nd/3rd delay
- 211: added non-overlapping clock
- 212: added P10000

**MICRON**  
COMMUNICATIONS, INC.  
INTEGRATED CIRCUIT DESIGN  
CONFIDENTIAL INFORMATION

LOGIC  
Data Instruction  
Instruction 2 11 bit words  
Instruction 1 11 bit words  
Instruction 2 11 bit words  
Instruction 1 11 bit words  
Instruction 2 11 bit words  
Instruction 1 11 bit words

7.1501AA

7.1501BA

7.1501CA

Fig 7.1501

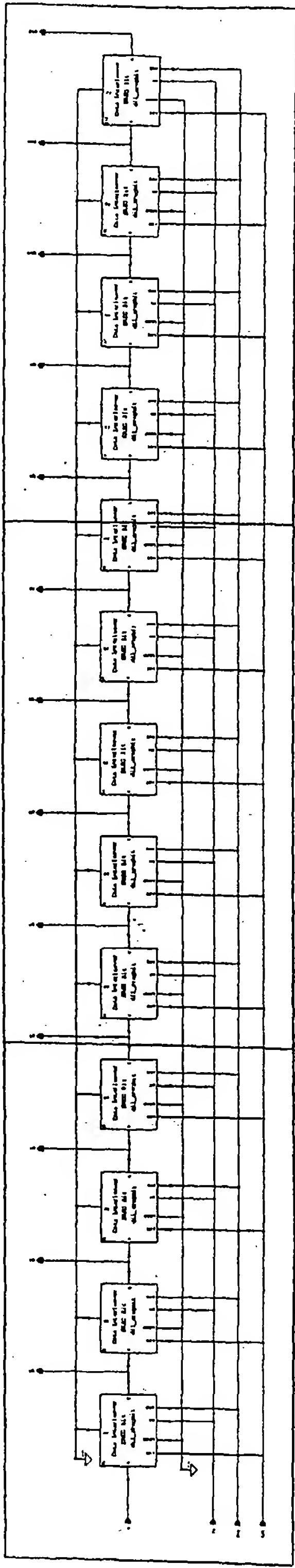


Fig. 7.1501

7.1502AA

7.1502BA

7.1502CA

ISS 7.1502

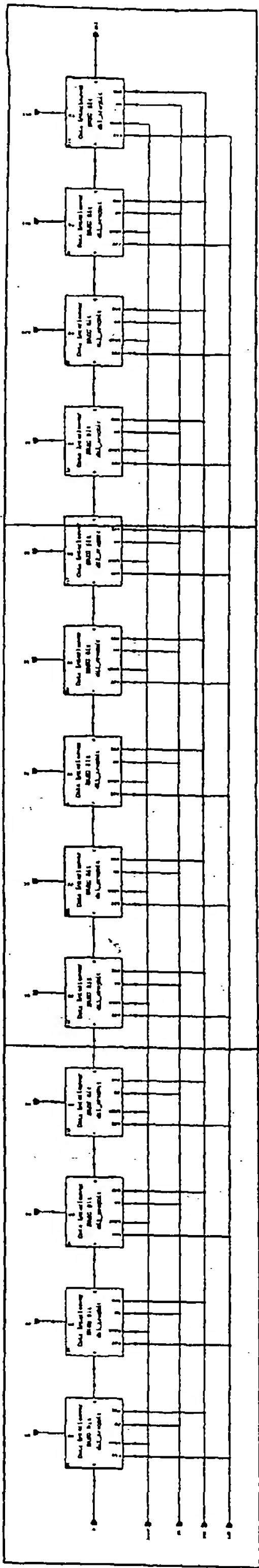
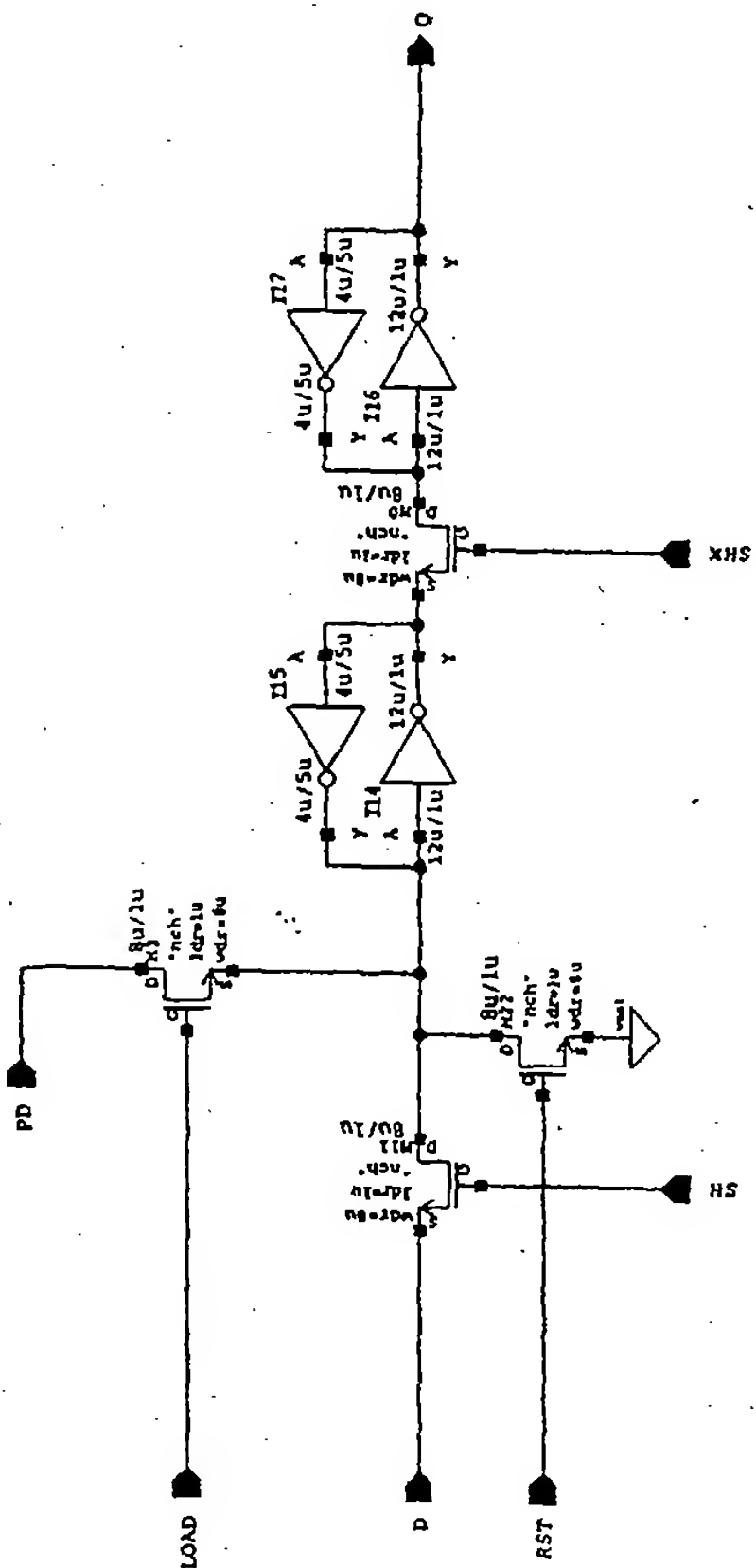


Fig. 7.1502



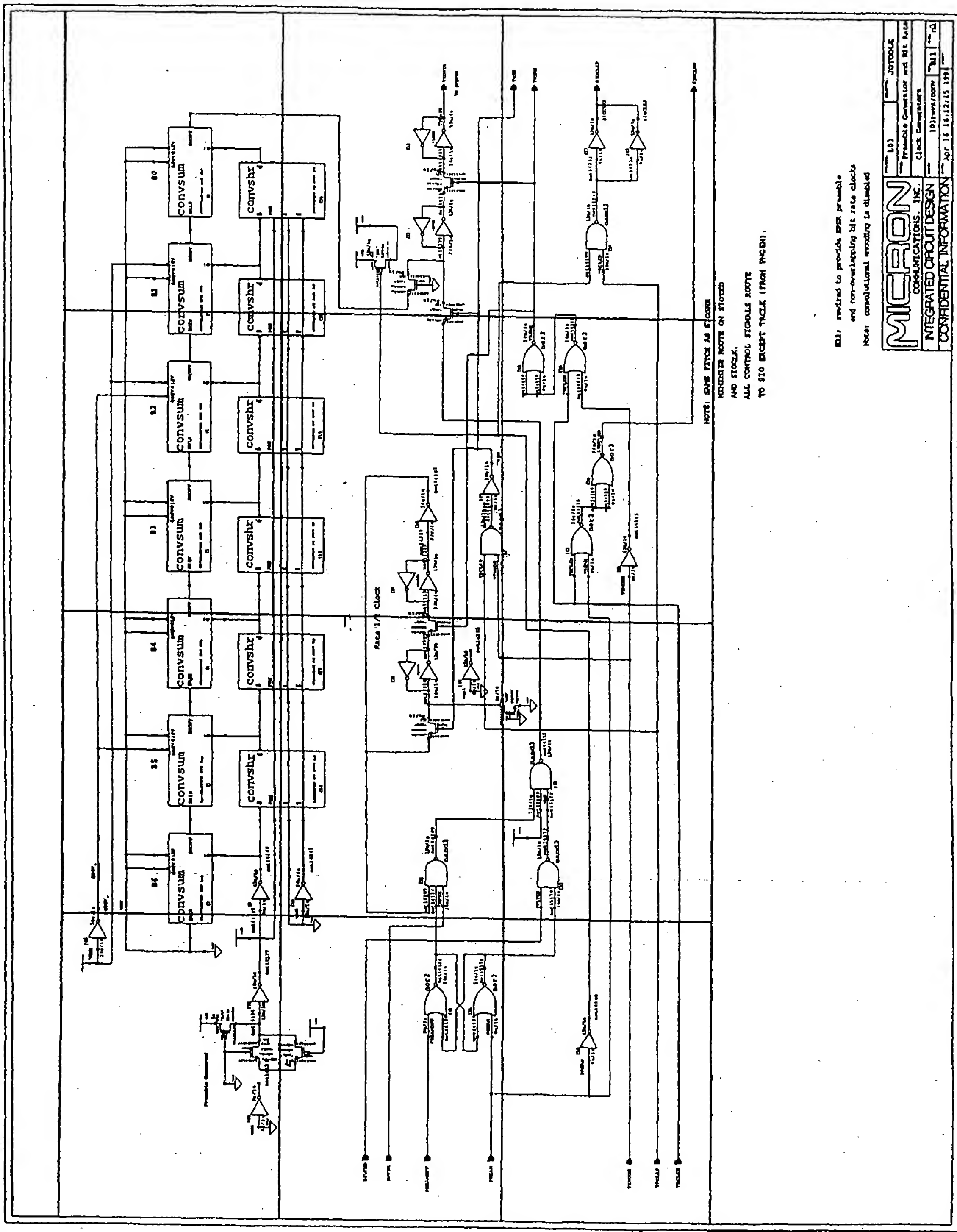
MICRON		PROJECT: L03	DESIGNER: JOTOOLE
COMMUNICATIONS, INC.		TITLE: Data Interleaver Shift	
INTEGRATED CIRCUIT DESIGN		Register Bit	
CONFIDENTIAL INFORMATION		WKS: 103reva/dil_sregbit	REV: B1
		DATE: Sep 27 10:25:07 1994	SHEET: A

7.16AA	7.16AB	7.16AC	7.16AD
7.16BA	7.16BB	7.16BC	7.16BD
7.16CA	7.16CB	7.16CC	7.16CD

II II II II II



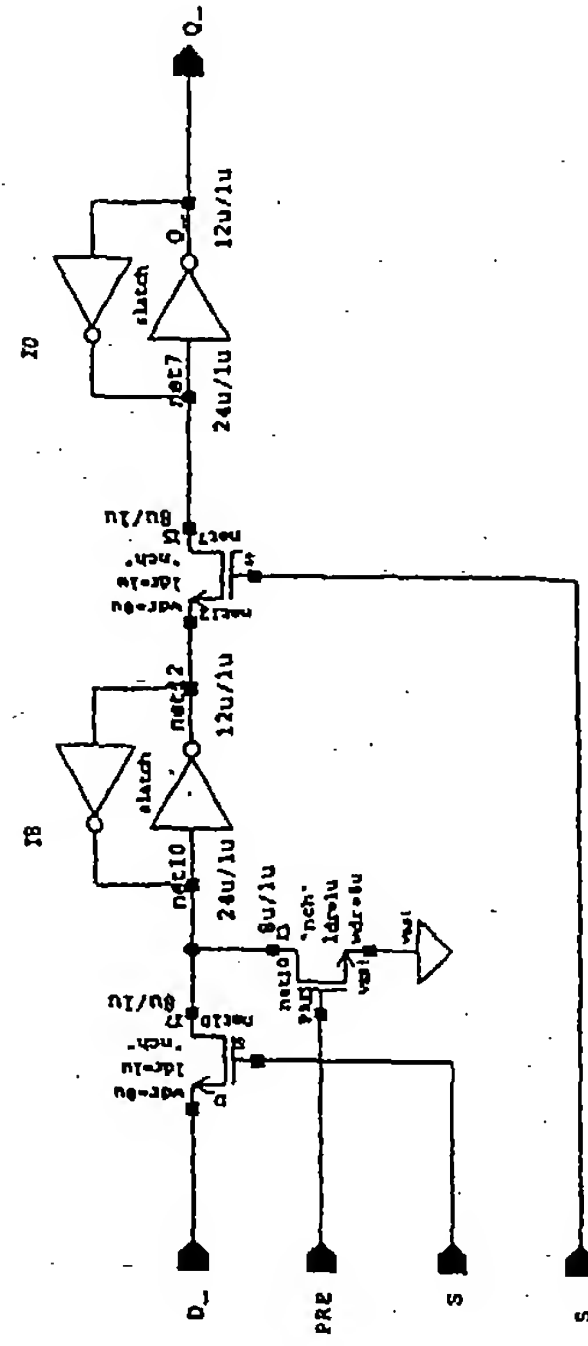
Fig. 7.16



ALL: required to provide both preamble and non-overlapping bit rate clocks. Note: convolutional encoding is disabled.

MICRON		103	JOTOOO
COMMUNICATIONS, INC.		Preamble Generation and Bit Rate	
INTEGRATED CIRCUIT DESIGN		Clock Generation	
CONFIDENTIAL INFORMATION		101rev/conv	7/11
		Apr 16 16:12:15 1991	

Fig. 7.1601



MICRON		PRODUCT: L03	DESIGNER: Rotzoll
COMMUNICATIONS, INC.		TYPE: Convolutional Encoder Shift	
INTEGRATED CIRCUIT DESIGN		REGISTER CELL	
CONFIDENTIAL INFORMATION		NAME: 103reva/convshr	REV: A
		DATE: Sep 2 10:34:27 1994	SHEET: 1

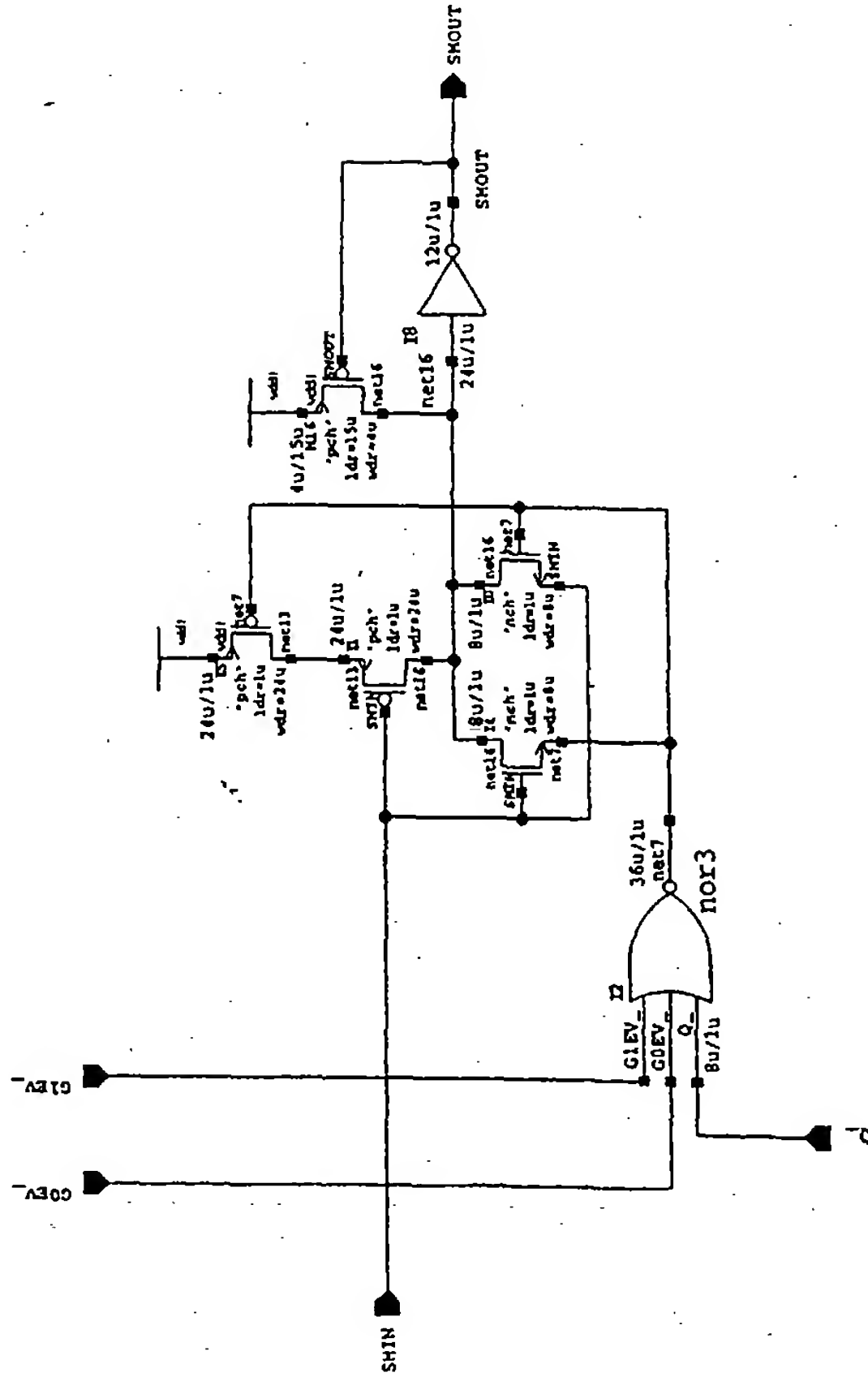


Fig. 7.1602

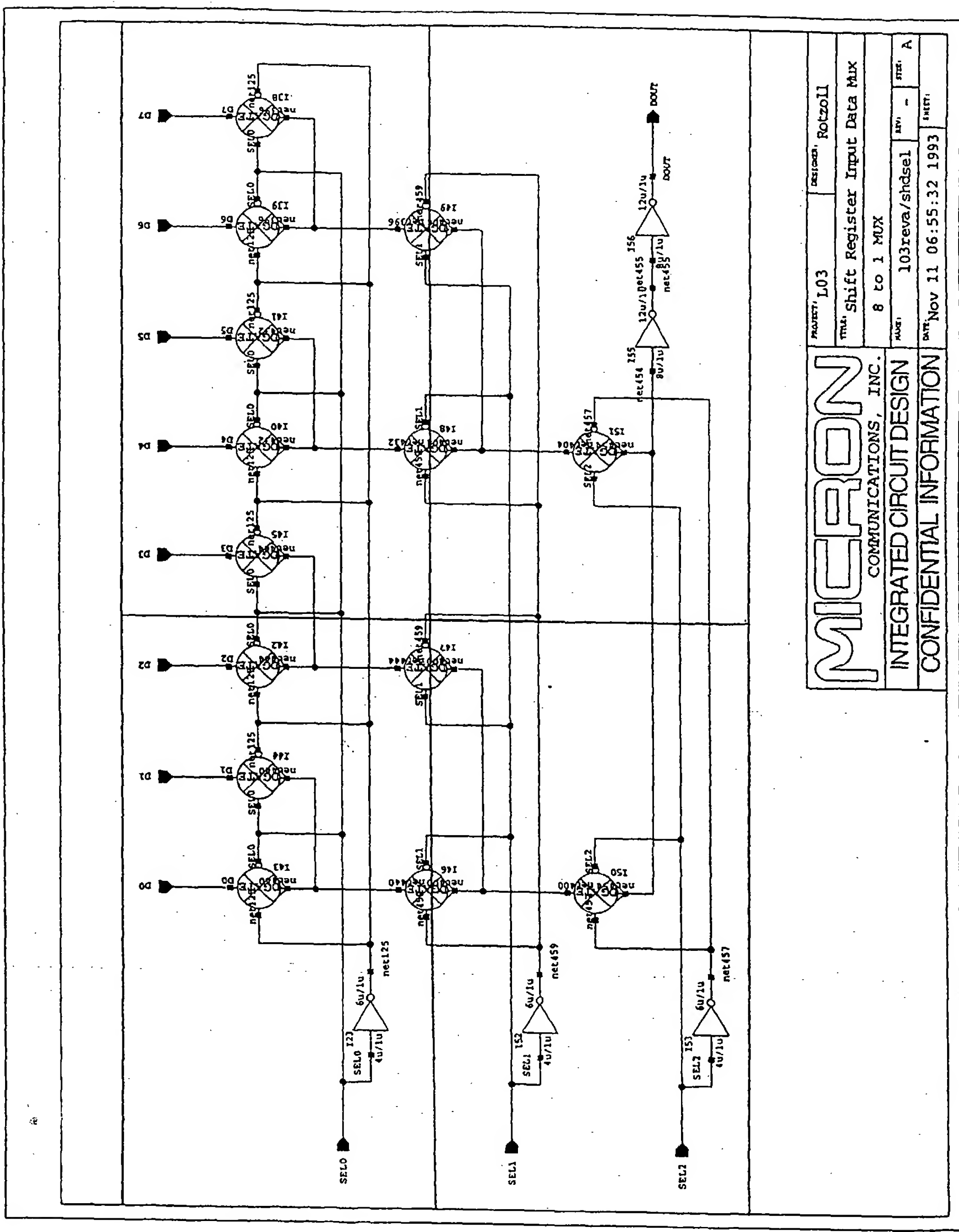
MICRON				DESIGNER: JOTOOLE	
COMMUNICATIONS, INC.				PROJECT: L03	
INTEGRATED CIRCUIT DESIGN				TITLE: Convolutional Encoder Summer	
CONFIDENTIAL INFORMATION					
NAME: 103reva/convsum		REV: B1		SIZE: A	
DATE: Sep 2 10:32:17 1994		PAGE: 1			

**MICRON**  
 COMMUNICATIONS, INC.  
 INTEGRATED CIRCUIT DESIGN  
 CONFIDENTIAL INFORMATION

7.17AB	7.17BB
7.17AA	7.17BA

Ex 11 11.11

Fig. 7.17



MICRON		DESIGN: Rotzoll	
PROJECT: L03			
TITLE: Shift Register Input Data Mux			
8 to 1 MUX			
REV: -	REV: -	REV: -	REV: A
DATE: Nov 11 06:55:32 1993			
SHEET: 1			

**MICRON**  
COMMUNICATIONS, INC.  
INTEGRATED CIRCUIT DESIGN  
CONFIDENTIAL INFORMATION

7.18AA	7.18AB	7.18AC
7.18BA	7.18BB	7.18BC
7.18CA	7.18CB	7.18CC

ILX 007 7.18BB

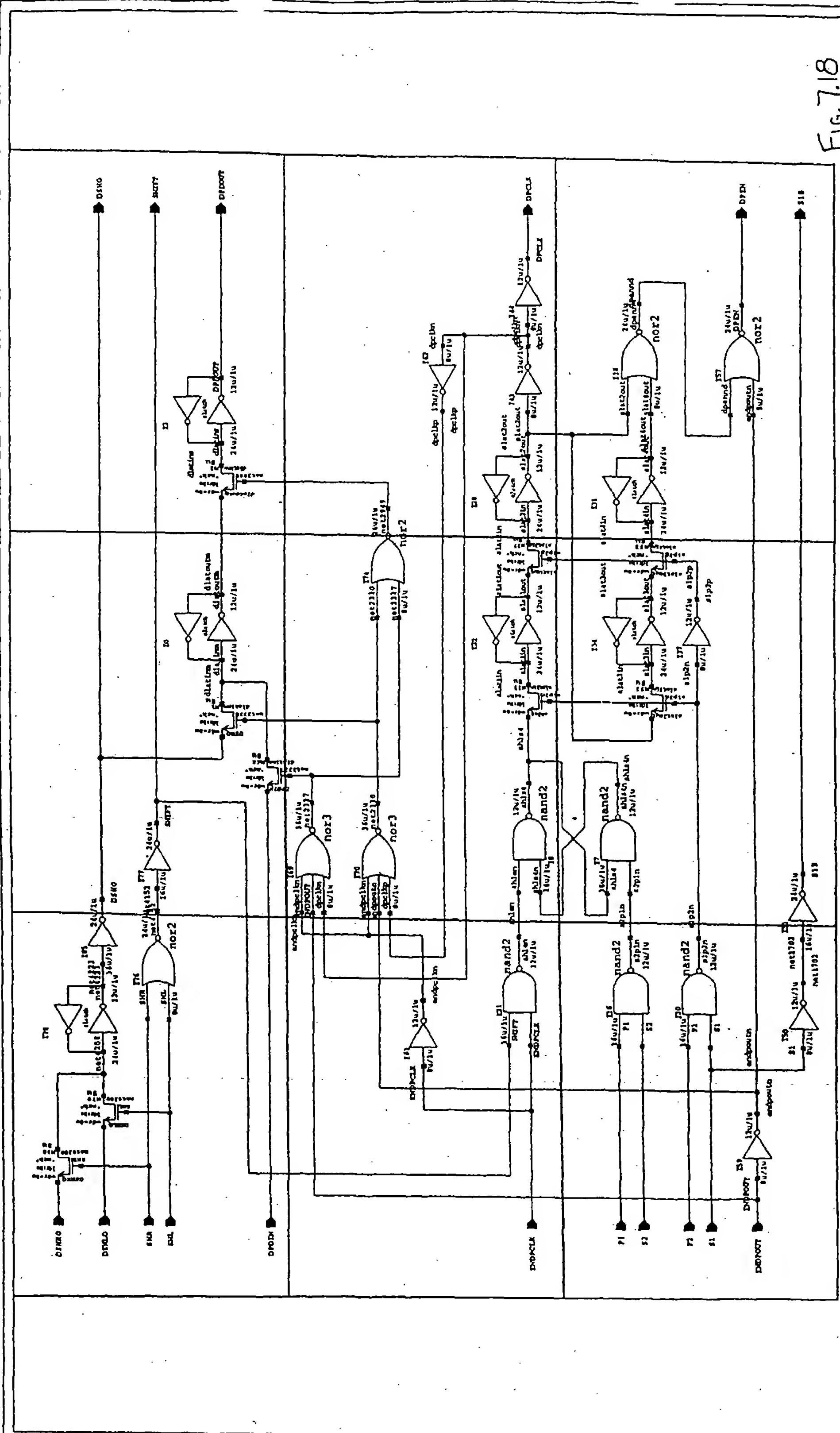


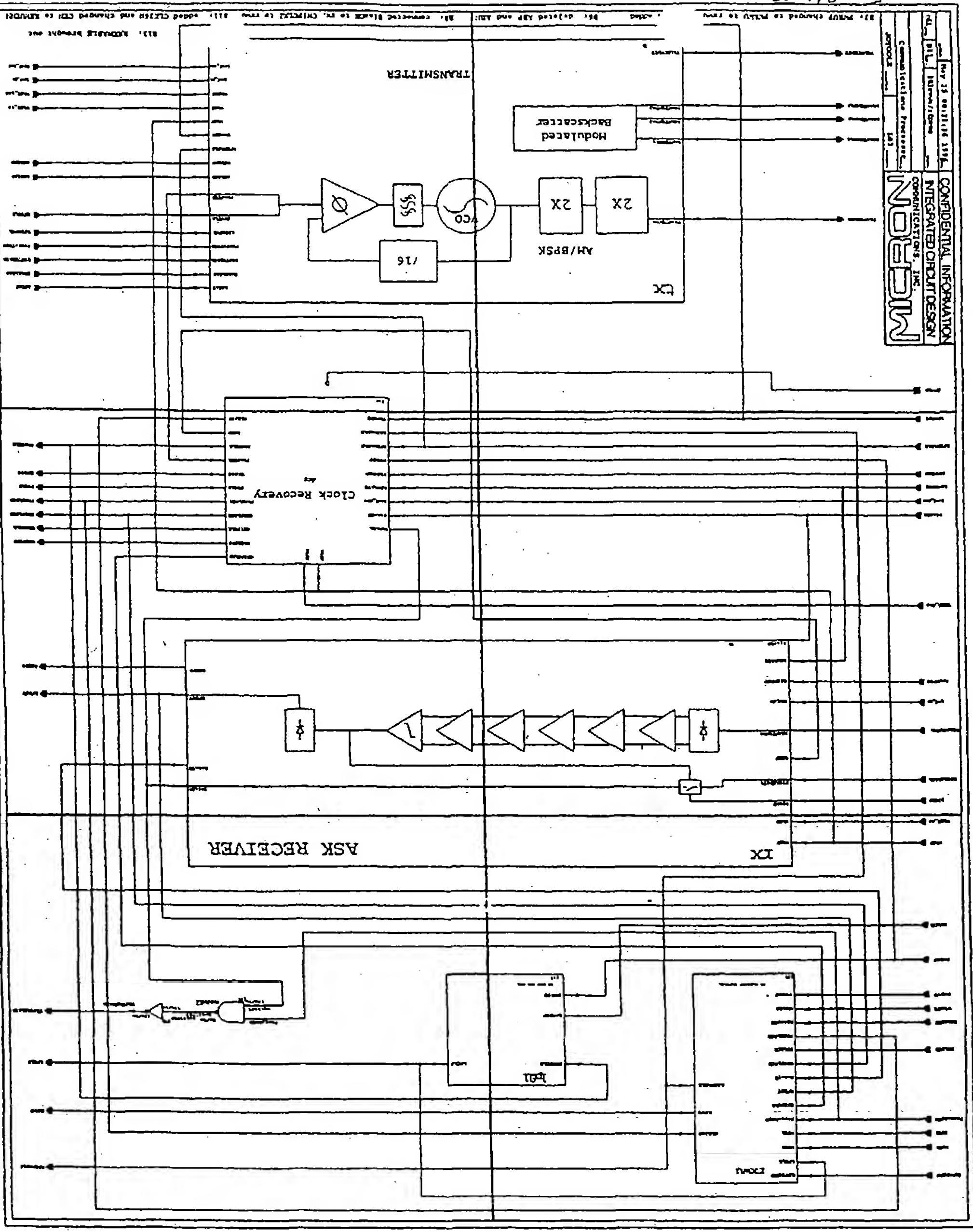
Fig. 7.18

PROJECT: L03		DESIGNED BY: ROZZOLI	
TITLE: Digital Port Output Controller			
NAME: 103 reva/doutport	REV: -	DATE: 11	
CONFIDENTIAL INFORMATION		Nov 12 10:05:40 1993	

8AA	8AB
8BA	8BB
8CA	8CB

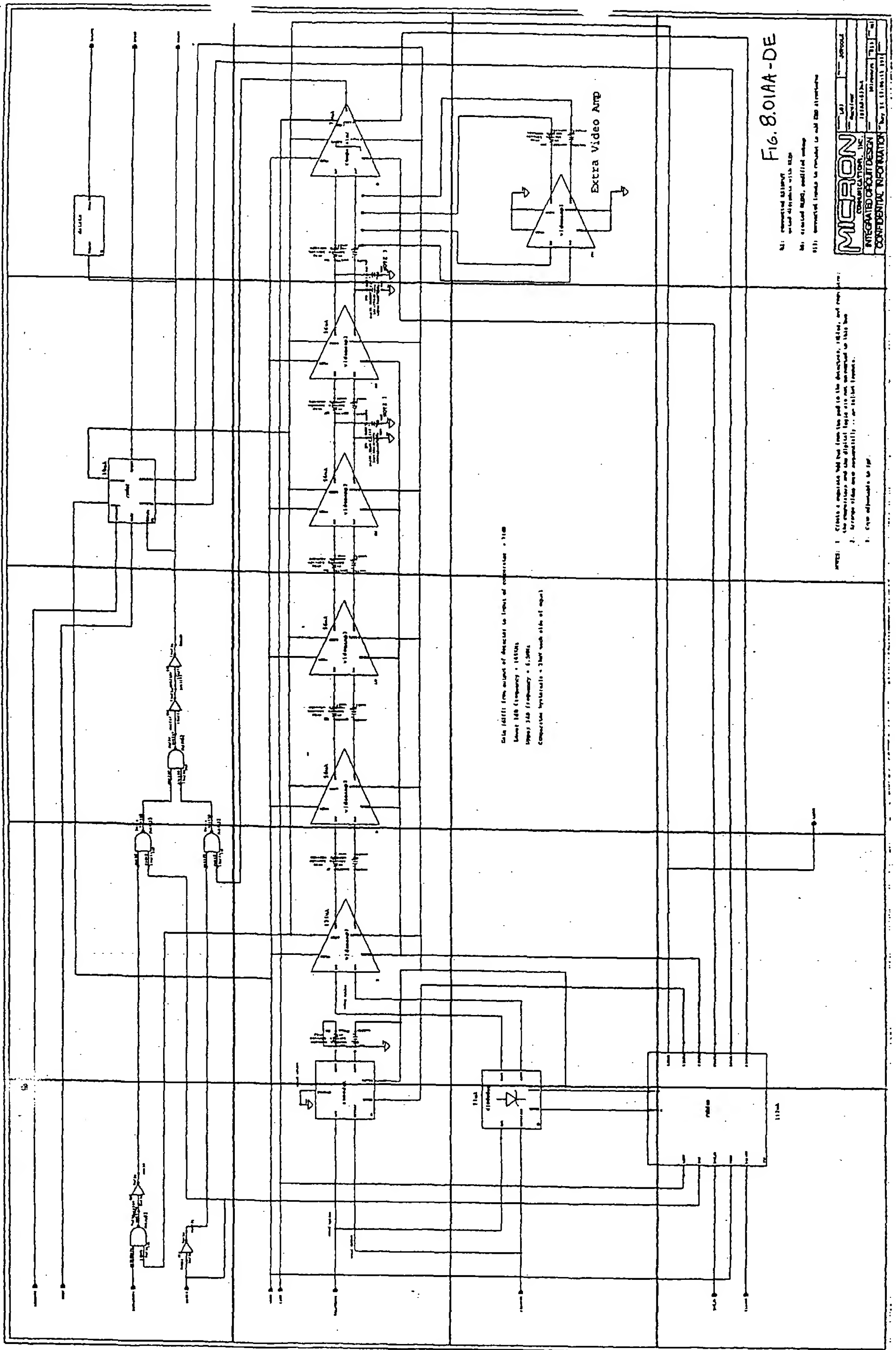


16.84A-CB



8.01AA	8.01AB	8.01AC	8.01AD	8.01AE
8.01BA	8.01BB	8.01BC	8.01BD	8.01BE
8.01CA	8.01CB	8.01CC	8.01CD	8.01CE
8.01DA	8.01DB	8.01DC	8.01DD	8.01DE

II II a II BB III II



8.0101AA	8.0101AB
8.0101BA	8.0101BB
8.0101CA	8.0101CB

II II II II II II II II

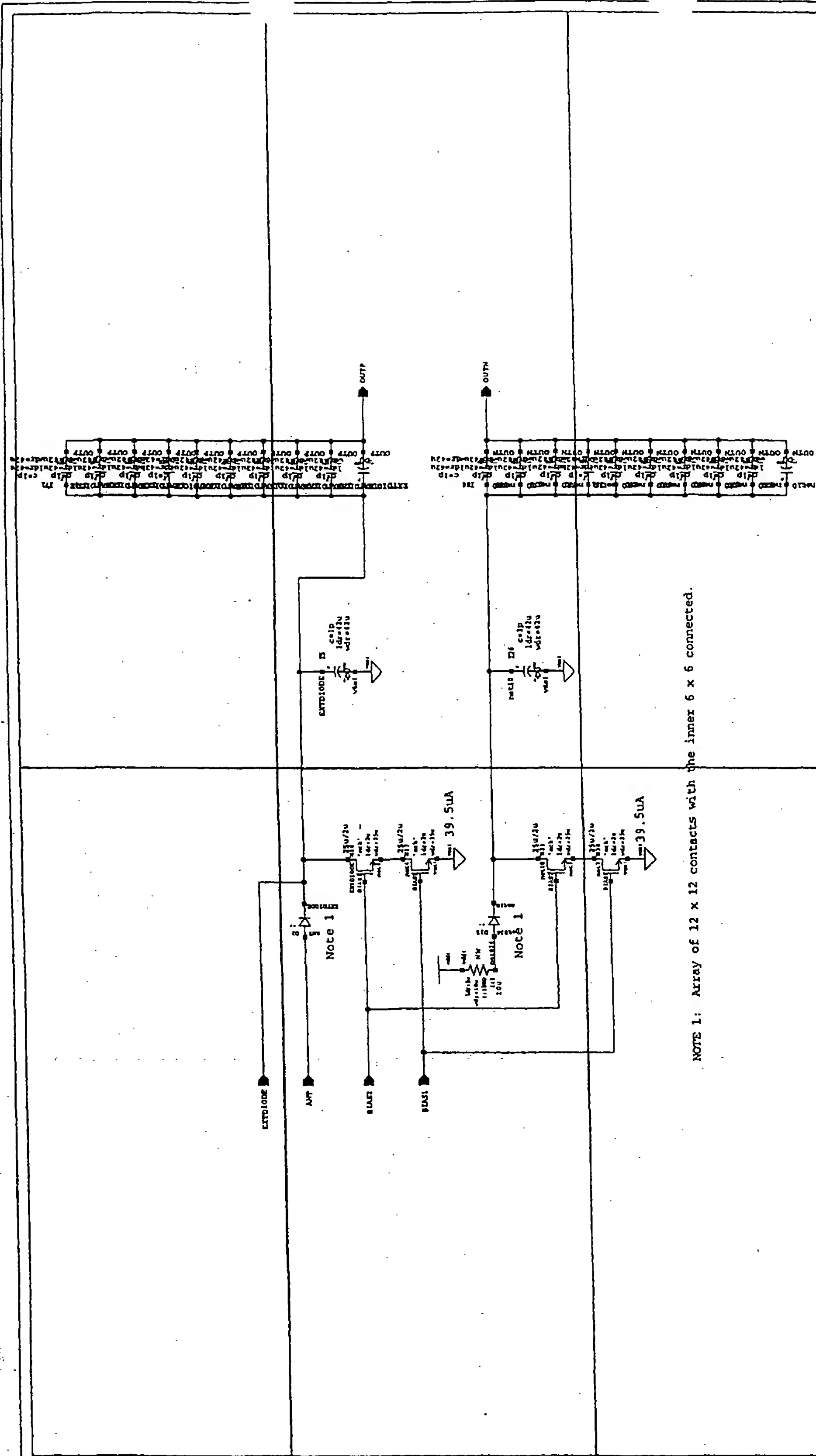


FIG. 8.0101AA-CB

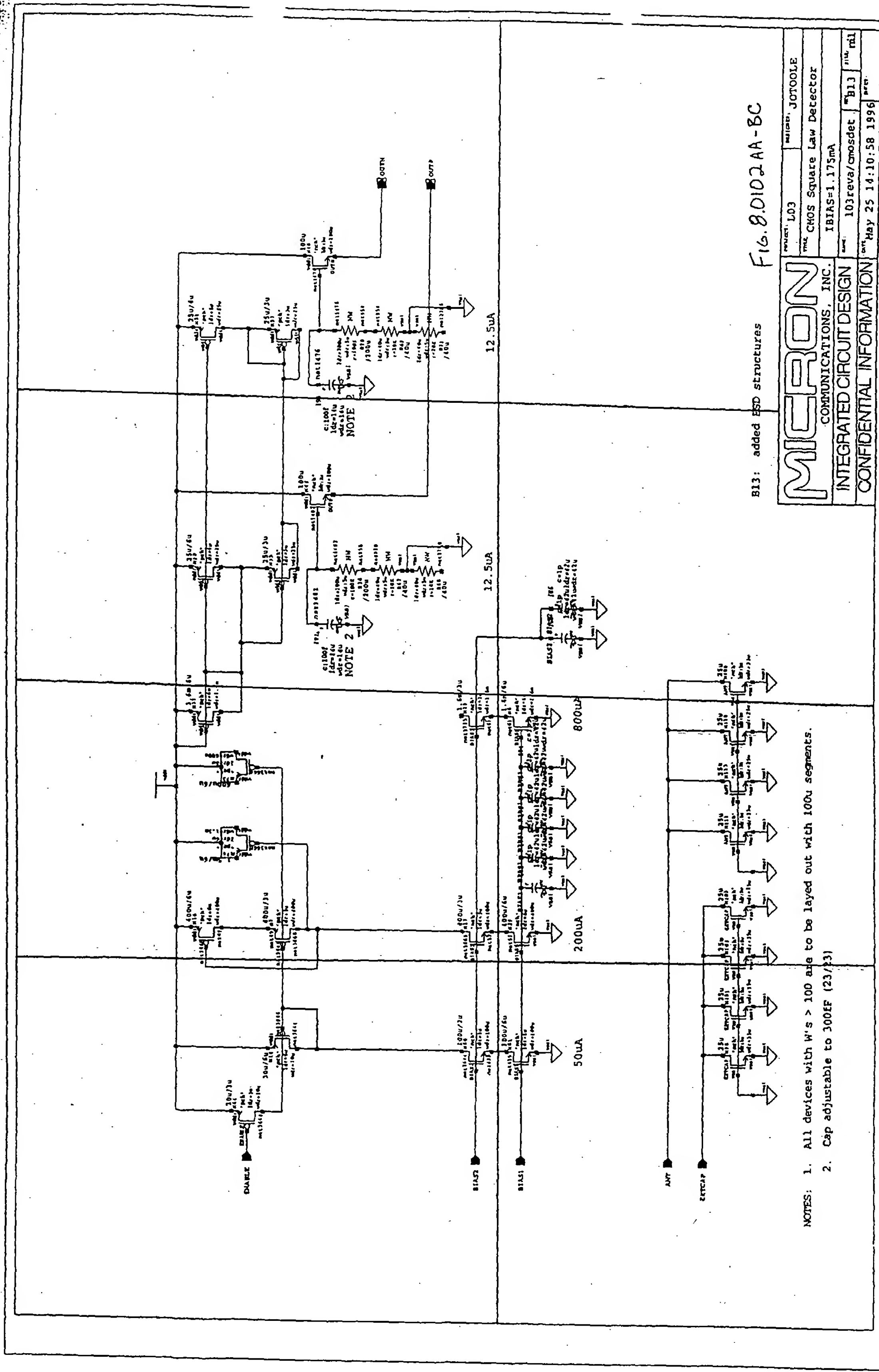
MICRON		PROJECT: L03	REVISION: J0000LE
COMMUNICATIONS, INC.		Title: Schottky Diode Detector	
INTEGRATED CIRCUIT DESIGN		IBIAS=79uA	
CONFIDENTIAL INFORMATION		NAME: 103reva/diode-det	Rev: B13
		DATE: May 24 13:54:28 1996	

- B2: connected EXTDIODE line
- B6: schottky array changed to 6x6  
rf cap reduced to 1pF
- B8: increased Cc to 10pF; decreased Crf to 1pF
- B13: added 1K resistor in series with dummy diode for ESD

NOTE 1: Array of 12 x 12 contacts with the inner 6 x 6 connected.

8.0102AA	8.0102AB	8.0102AC	8.0102AD
8.0102BA	8.0102BB	8.0102BC	

II II III III III III



B13: added ESD structures Fig. 8.0102AA-BC

MICRON		PROJECT L03	REVISION J0700LE
COMMUNICATIONS, INC.		NAME CMOS Square Law Detector	
INTEGRATED CIRCUIT DESIGN		IBIAS=1.175mA	
CONFIDENTIAL INFORMATION		DATE 103revs/amosdet	B13
		DATE May 25 14:10:58 1996	ml

8.0103AA	8.0103AB	8.0103AC	8.0103AD	8.0103AE	8.0103AF
8.0103BA	8.0103BB	8.0103BC	8.0103BD	8.0103BE	8.0103BF
8.0103CA	8.0103CB	8.0103CC	8.0103CD	8.0103CE	8.0103CF

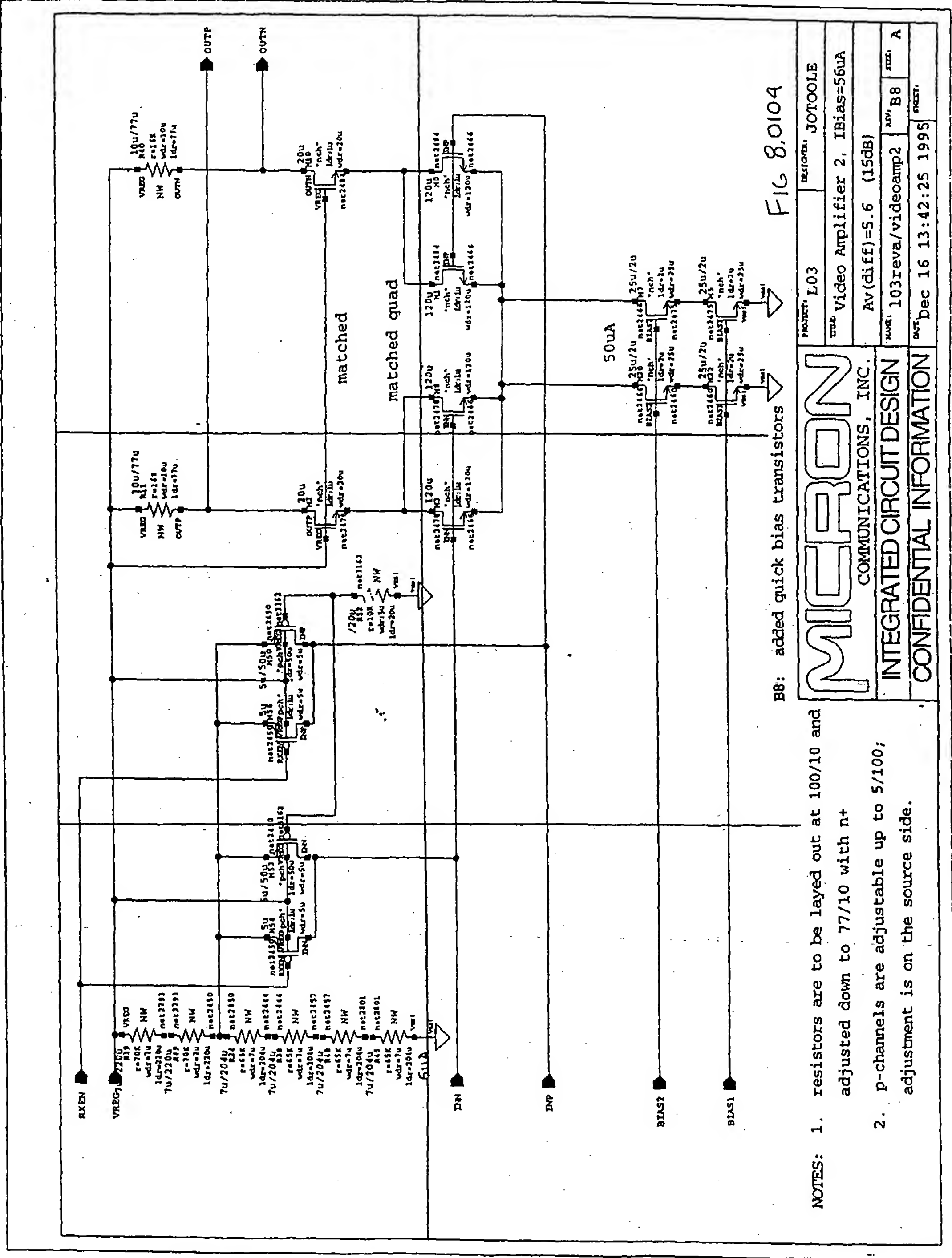
IL 11 00 00 00 00 00





8.0104AA	8.0104AB	8.0104AC
8.0104BA	8.0104BB	8.0104BC

8.0104



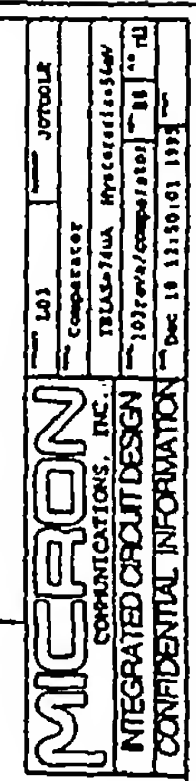
- NOTES:
1. resistors are to be layed out at 100/10 and adjusted down to 77/10 with n+
  2. p-channels are adjustable up to 5/100; adjustment is on the source side.

MICRON	
COMMUNICATIONS, INC.	
INTEGRATED CIRCUIT DESIGN	
CONFIDENTIAL INFORMATION	
PROJECT: L03	DESIGNER: JOTOOLE
TITLE: Video Amplifier 2, IBias=56uA	
AV(diff)=5.6 (15dB)	
DATE: 103revA/videoamp2	REV: B8
PAGE: 1	
DATE: Dec 16 13:42:25 1995	

8.0105AA	8.0105AB	8.0105AC	8.0105AD	
8.0105BA	8.0105BB	8.0105BC	8.0105BD	
8.0105CA	8.0105CB	8.0105CC	8.0105CD	8.0105CE
8.0105DA	8.0105DB	8.0105DC	8.0105DD	8.0105DE
8.0105EA	8.0105EB	8.0105EC	8.0105ED	

IL 11 03 88.00.11.005

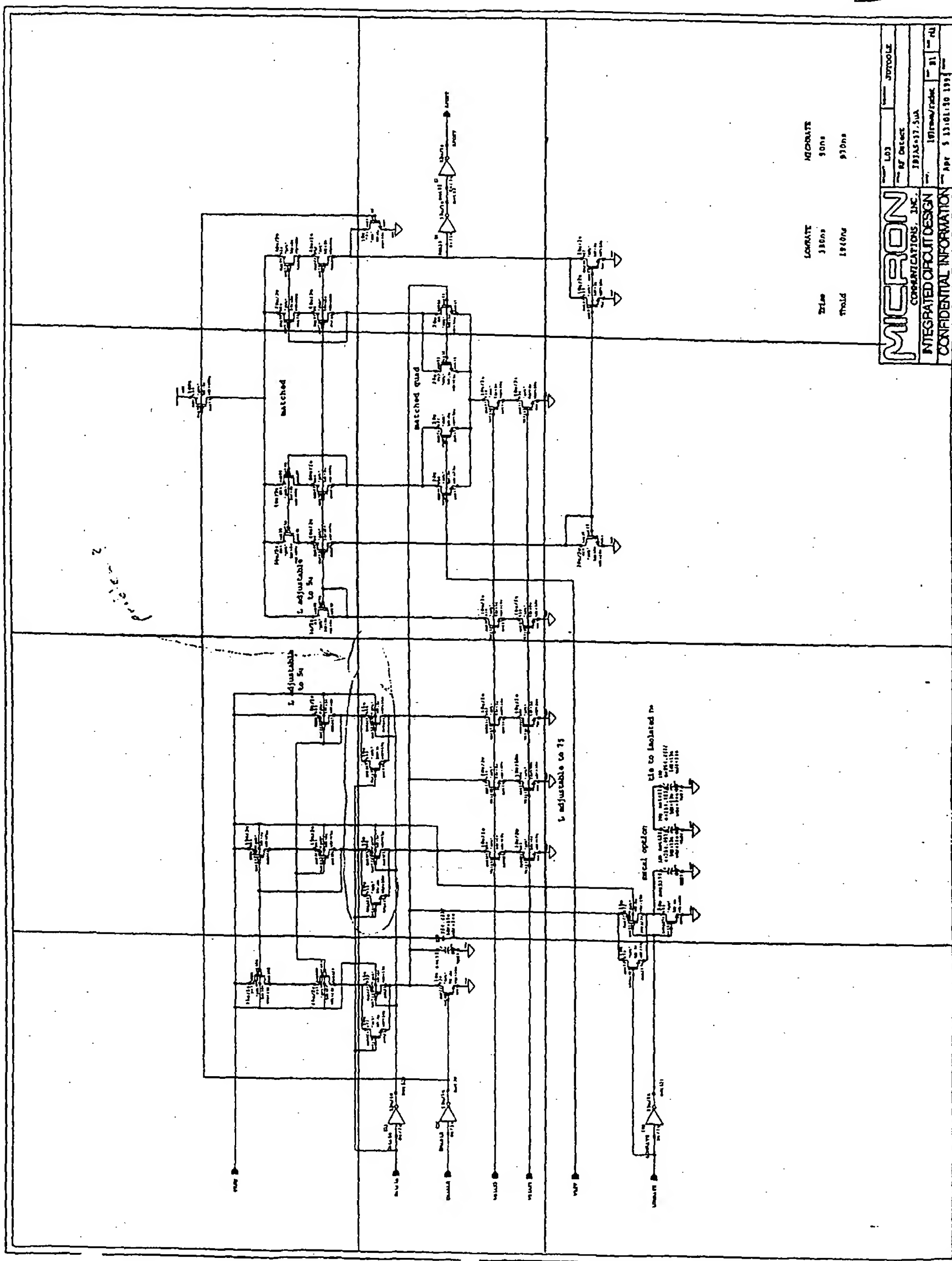
5



8.0106AA	8.0106AB	8.0106AC	8.0106AD
8.0106BA	8.0106BB	8.0106BC	8.0106BD
8.0106CA	8.0106CB	8.0106CC	8.0106CD

ILR 88.00.11.016

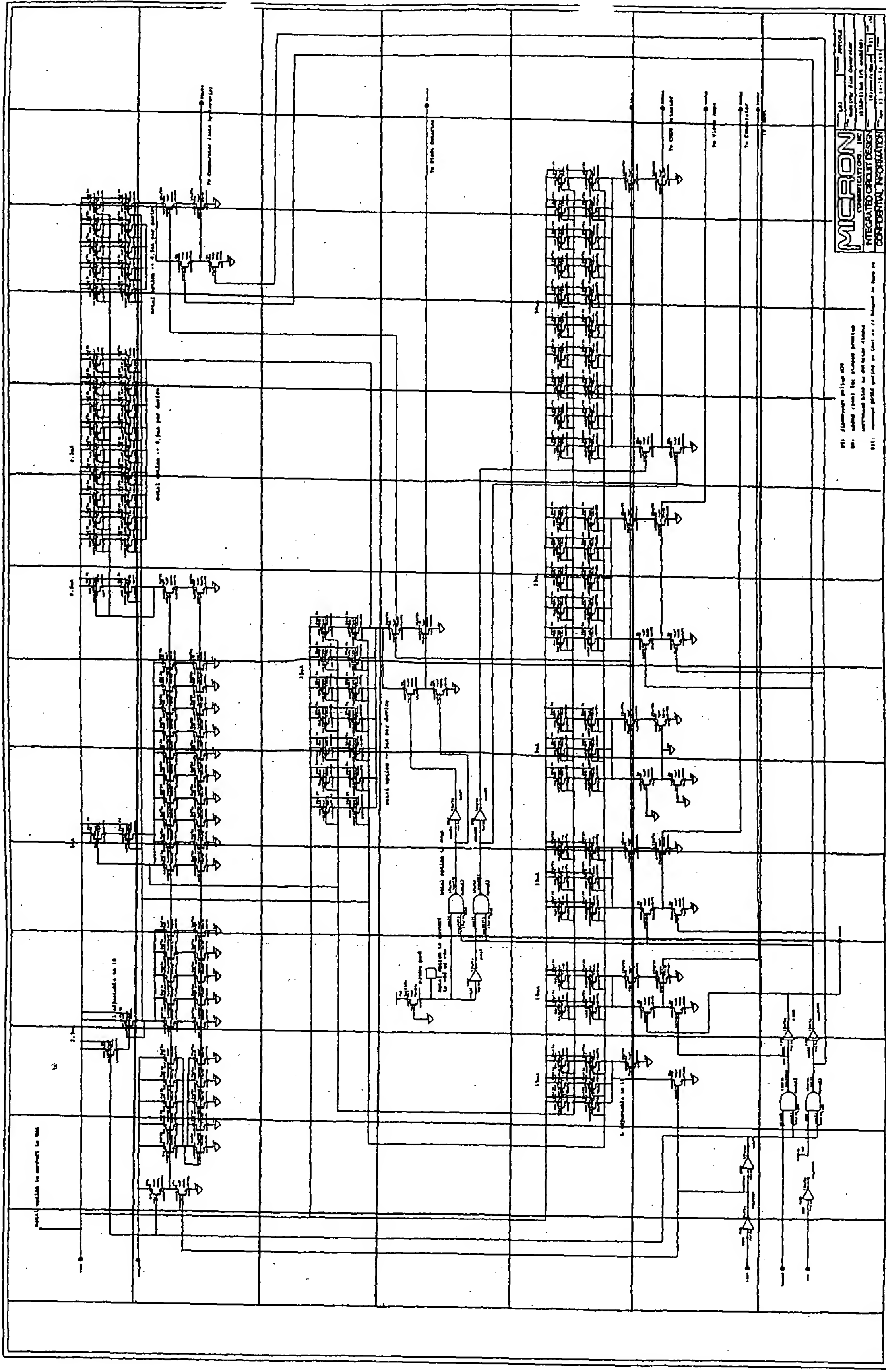
Fig. 8.0106



8.0107AA	8.0107AB	8.0107AC	8.0107AD	8.0107AE	8.0107AF	8.0107AG	8.0107AH	8.0107AI	8.0107AJ	8.0107AK	8.0107AL	8.0107AM	
8.0107BA	8.0107BB	8.0107BC	8.0107BD	8.0107BE	8.0107BF	8.0107BG	8.0107BH	8.0107BI	8.0107BJ	8.0701BK	8.0107BL	8.0107BM	8.0107BN
8.0107CA	8.0107CB	8.0107CC	8.0107CD	8.0107CE	8.0107CF	8.0107CG	8.0107CH	8.0107CI	8.0107CJ	8.0107CK	8.0107CL	8.0107CM	8.0107CN
8.0107DA	8.0107DB	8.0107DC	8.0107DD	8.0107DE	8.0107DF	8.0107DG	8.0107DH	8.0107DI	8.0107DJ	8.0107DK	8.0107DL	8.0107DM	8.0107DN
8.0107EA	8.0107EB	8.0107EC	8.0107ED	8.0107EE	8.0107EF	8.0107EG	8.0107EH	8.0107EI	8.0107EJ	8.0107EK	8.0107EL	8.0107EM	8.0107EN
8.0107FA	8.0107FB	8.0107FC	8.0107FD	8.0107FE	8.0107FF	8.0107FG	8.0107FH	8.0107FI	8.0107FJ	8.0107FK	8.0107FL	8.0107FM	8.0107FN
8.0107GA	8.0107GB	8.0107GC	8.0107GD	8.0107GE	8.0107GF	8.0107GG	8.0107GH	8.0107GI	8.0107GJ	8.0107GK	8.0107GL	8.0107GM	8.0107GN


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**MICRON**  
16K1607  
INTEGRATED CIRCUIT DESIGN  
CONFIDENTIAL INFORMATION  
Page 11 of 12

Placed in place of  
Added (new) for storage  
Removed (old) for storage

16K1607

8.0108AC	8.0108AB	8.0108AA
----------	----------	----------

8.0108AB 8.0108AC 8.0108AA

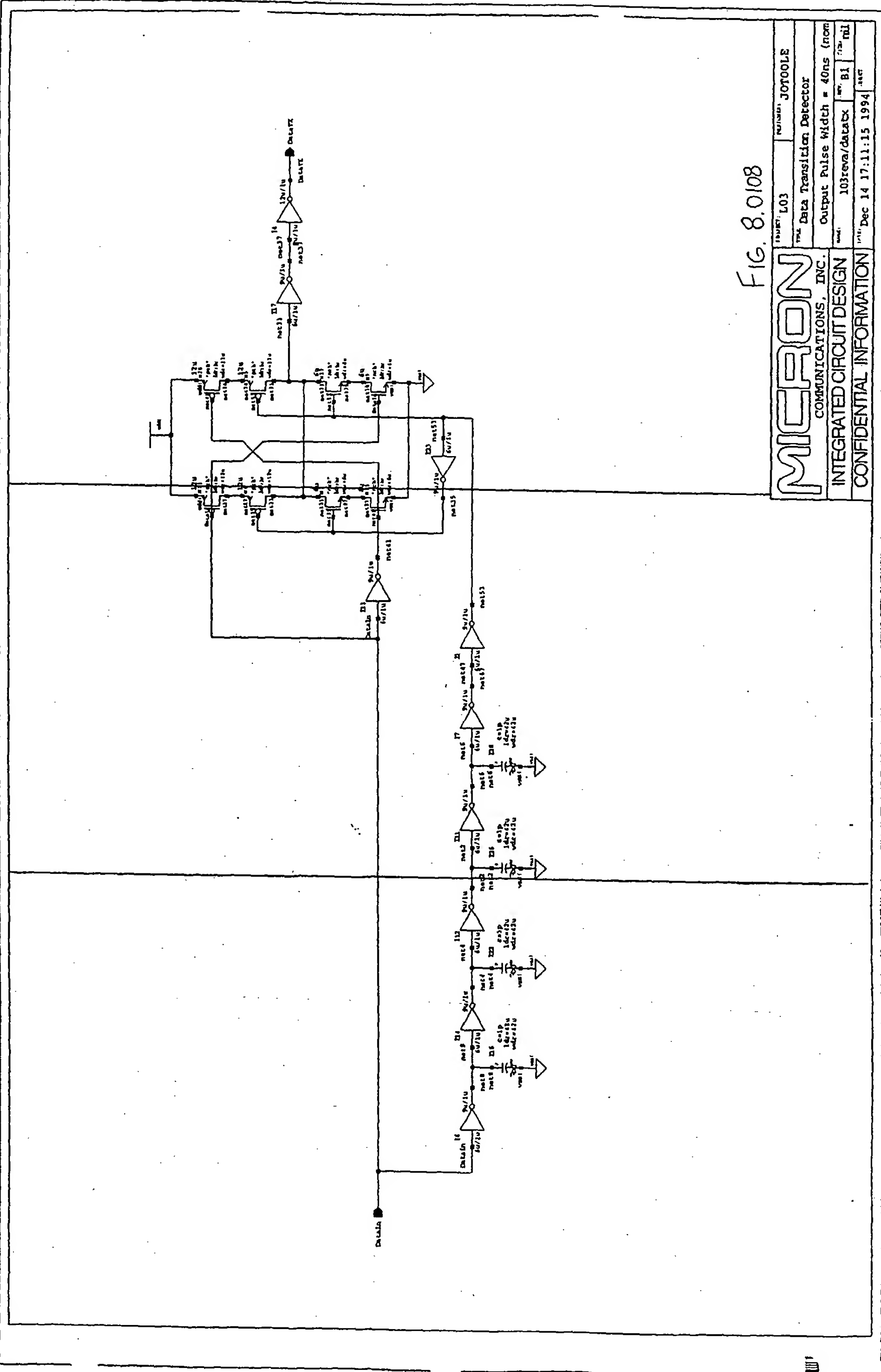


FIG. 8.0108

MICRON		1000001	J0700LE
COMMUNICATIONS, INC.		Data Transition Detector	
INTEGRATED CIRCUIT DESIGN		Output Pulse Width = 40ns (nom)	
CONFIDENTIAL INFORMATION		103revs/databx	BI
		1994	Dec 14 17:11:15 1994





8.0201AB

8.0201AA

8.0201AB

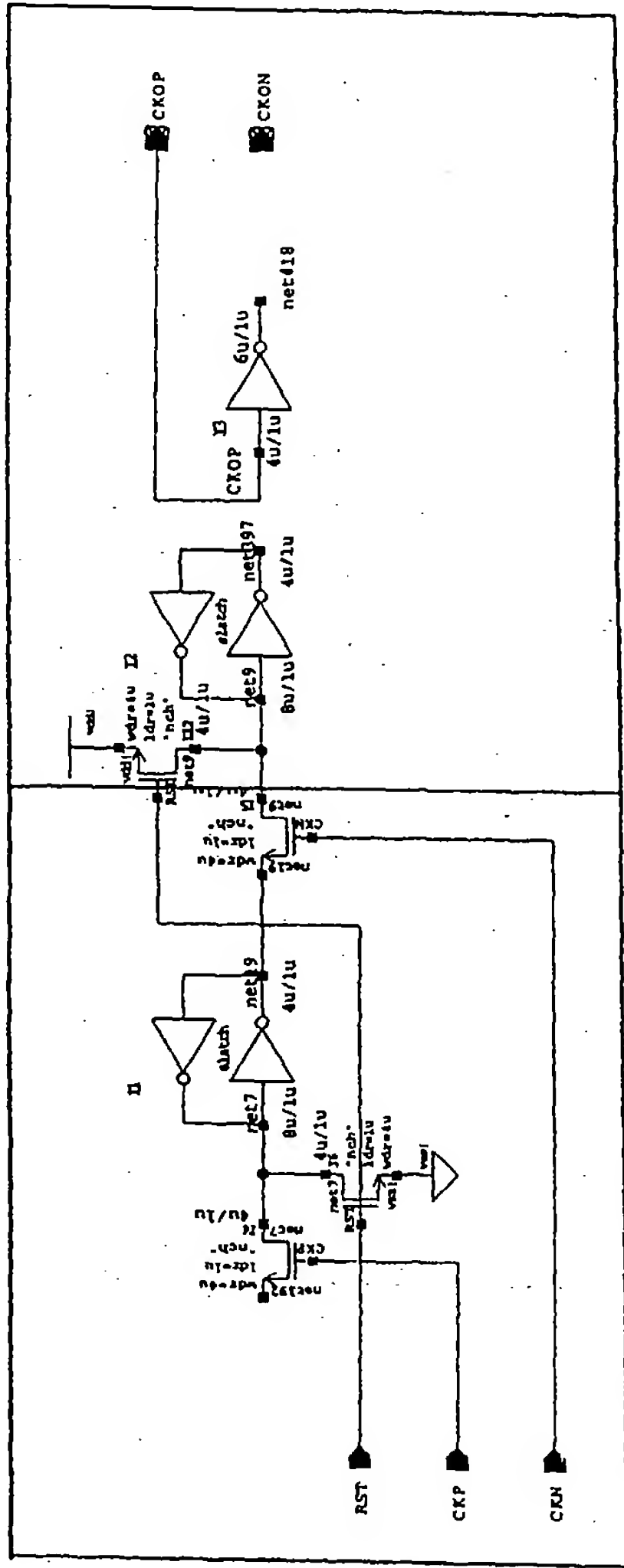


Fig. 8.0201

PROJECT: L03		DESIGNER: JOTOOLE	
TITLE: Timed Lockout Divider Cell			
PART: I03reva/tlcel_bypass		REV: B10	SIZE: A
DATE: Mar 26 13:54:47 1996		SHEET: 1	

B10: new cell to bypass 1st counter stage

**MICRON**  
COMMUNICATIONS, INC.  
INTEGRATED CIRCUIT DESIGN  
CONFIDENTIAL INFORMATION

8.0202AA	8.0202AB	8.0202AC	8.0202AD
8.0202BA	8.0202BB	8.0202BC	8.0202BD
8.0202CA	8.0202CB	8.0202CC	8.0202CD

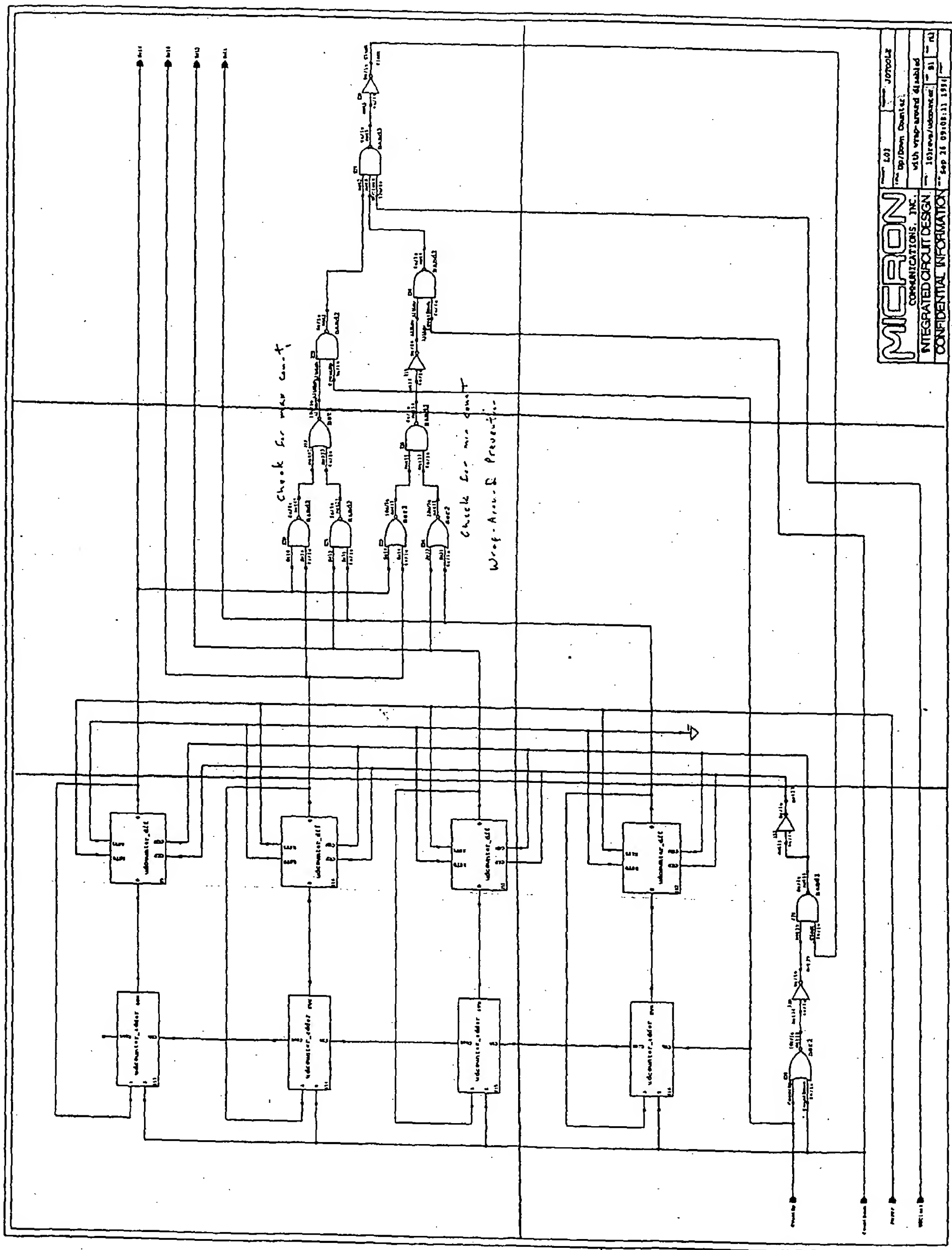
II II 88.000000





8.0203AA	8.0203AB	8.0203AC
8.0203BA	8.0203BB	8.0203BC

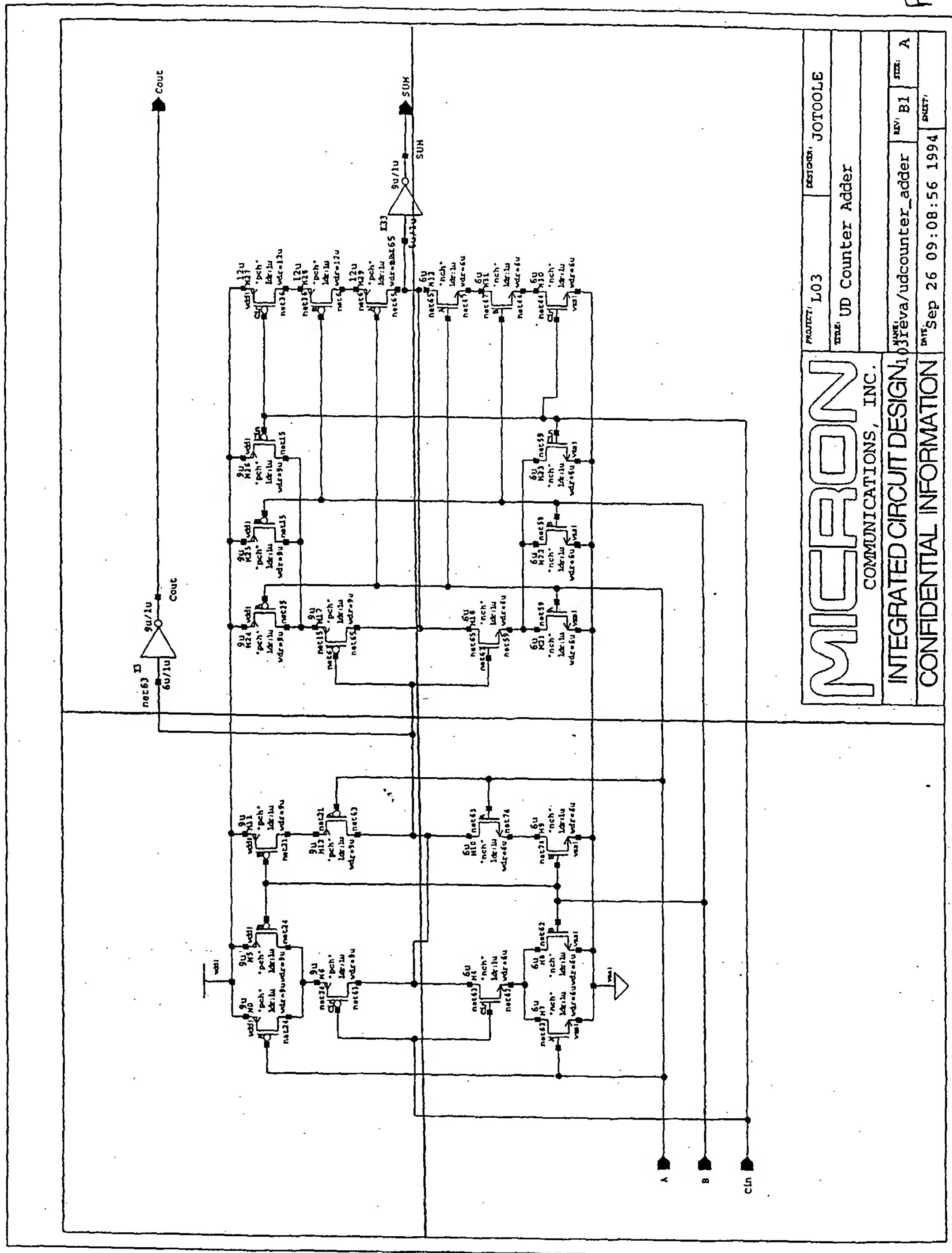
II 8.0203



**MICRON**  
 COMMUNICATIONS, INC.  
 INTEGRATED CIRCUIT DESIGN  
 CONFIDENTIAL INFORMATION  
 L01 J0700L2  
 with wrap-around disabled  
 10/19/94/10/19/94  
 Sep 25 09:08:11 1994

FIG. 8.0203





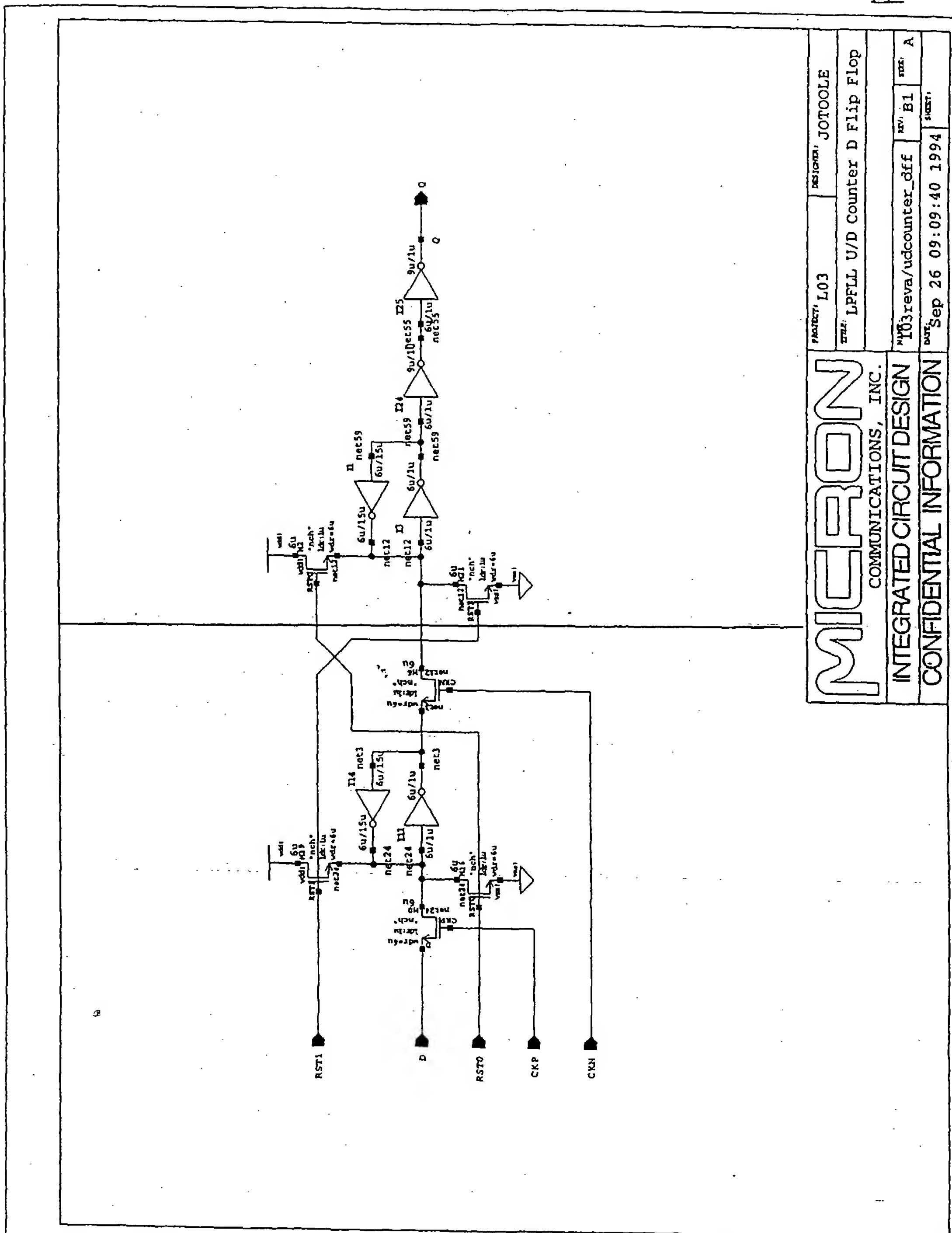
<b>MICRON</b>		PROJECT: L03	DESIGN: J0700LE
COMMUNICATIONS, INC.		UD Counter Adder	
INTEGRATED CIRCUIT DESIGN		FILE: udcounter_addr	REV: A
CONFIDENTIAL INFORMATION		DATE: Sep 26 09:08:56 1994	SHEET: 1

FIG. 8.020301

8.020302AB

8.020302AA

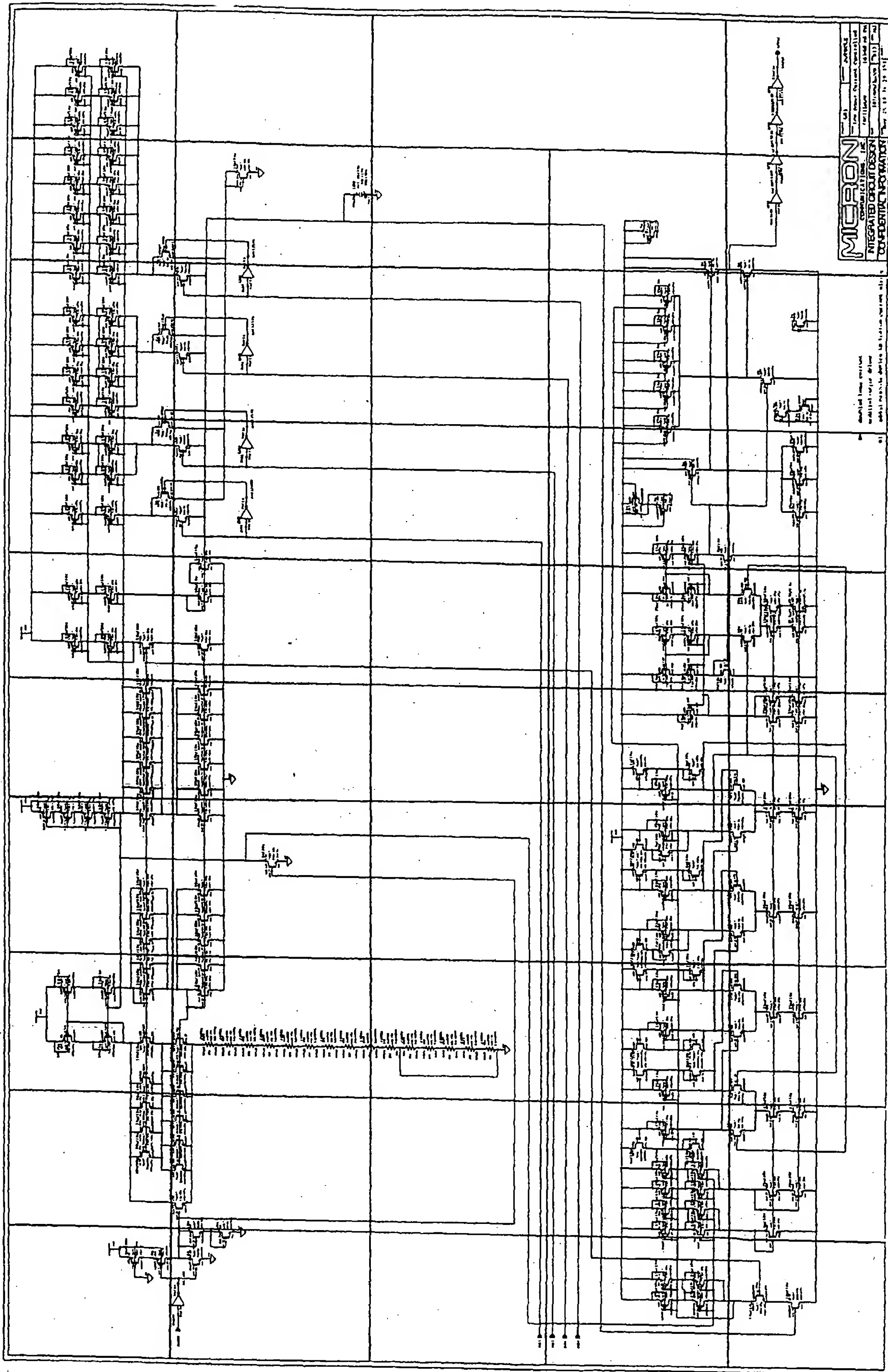
8.020302



8.0204AA	8.0204AB	8.0204AC	8.0204AD	8.0204AE	8.0204AF	8.0204AG	8.0204AH	8.0204AI	8.0204AJ
8.0204BA	8.0204BB	8.0204BC	8.0204BD	8.0204BE	8.0204BF	8.0204BG	8.0204BH	8.0204BI	8.0204BJ
8.0204CA	8.0204CB	8.0204CC	8.0204CD	8.0204CE	8.0204CF	8.0204CG	8.0204CH	8.0204CI	
8.0204DA	8.0204DB	8.0204DC	8.0204DD	8.0204DE	8.0204DF	8.0204DG	8.0204DH	8.0204DI	
8.0204EA	8.0204EB	8.0204EC	8.0204ED	8.0204EE	8.0204EF	8.0204EG	8.0204EH	8.0204EI	8.0204EJ

II II III III III III III III

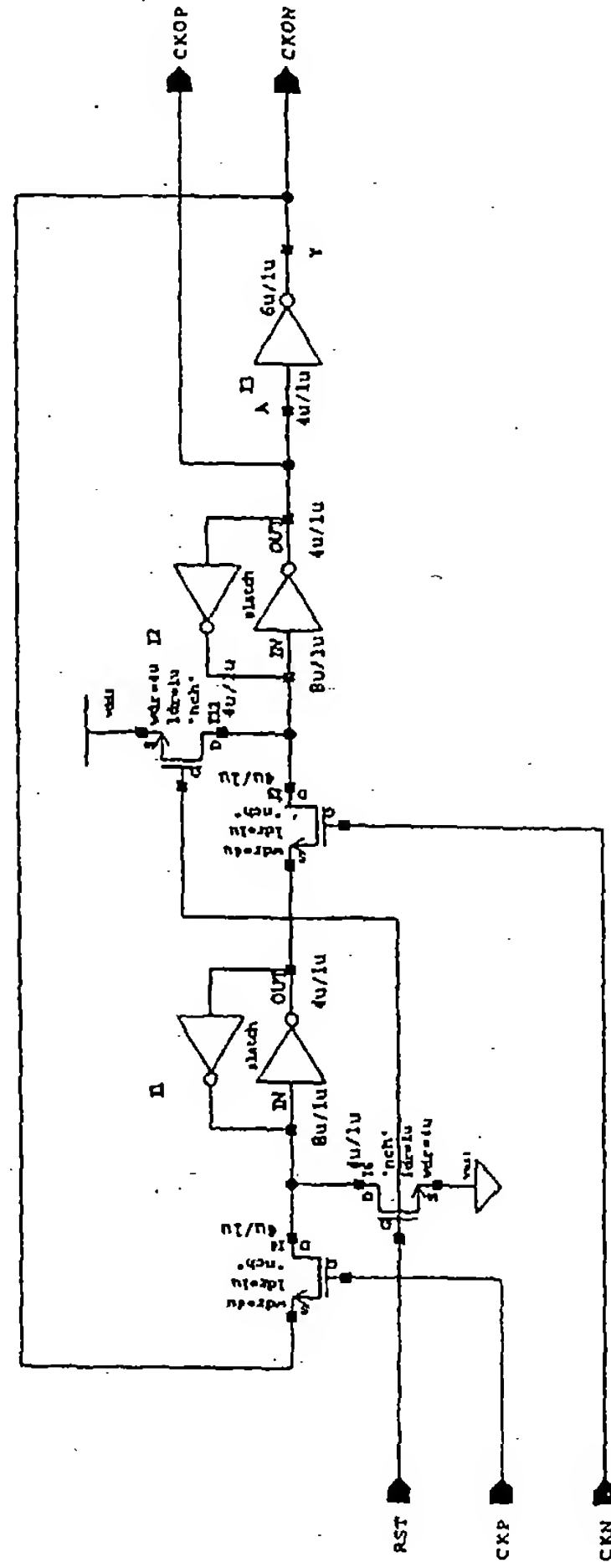




**MICRON**  
INTEGRATED CIRCUIT DESIGN  
CONFIDENTIAL INFORMATION

Fig. 2020AA-EJ

Model 2020AA-EJ  
Model 2020AA-EJ  
Model 2020AA-EJ



12/29/92

<b>MICRON</b>		PROJECT: L03	DESIGNER: Rotzoll
COMMUNICATIONS, INC.		TITLE: Timed Lockout Divider Cell	
INTEGRATED CIRCUIT DESIGN		NAME: 103reva/tldcel	REV: A
CONFIDENTIAL INFORMATION		DATE: Sep 22 15:26:56 1994	

~~F1680205~~  
F1680205

8.03AB

8.03AA

8.03AB

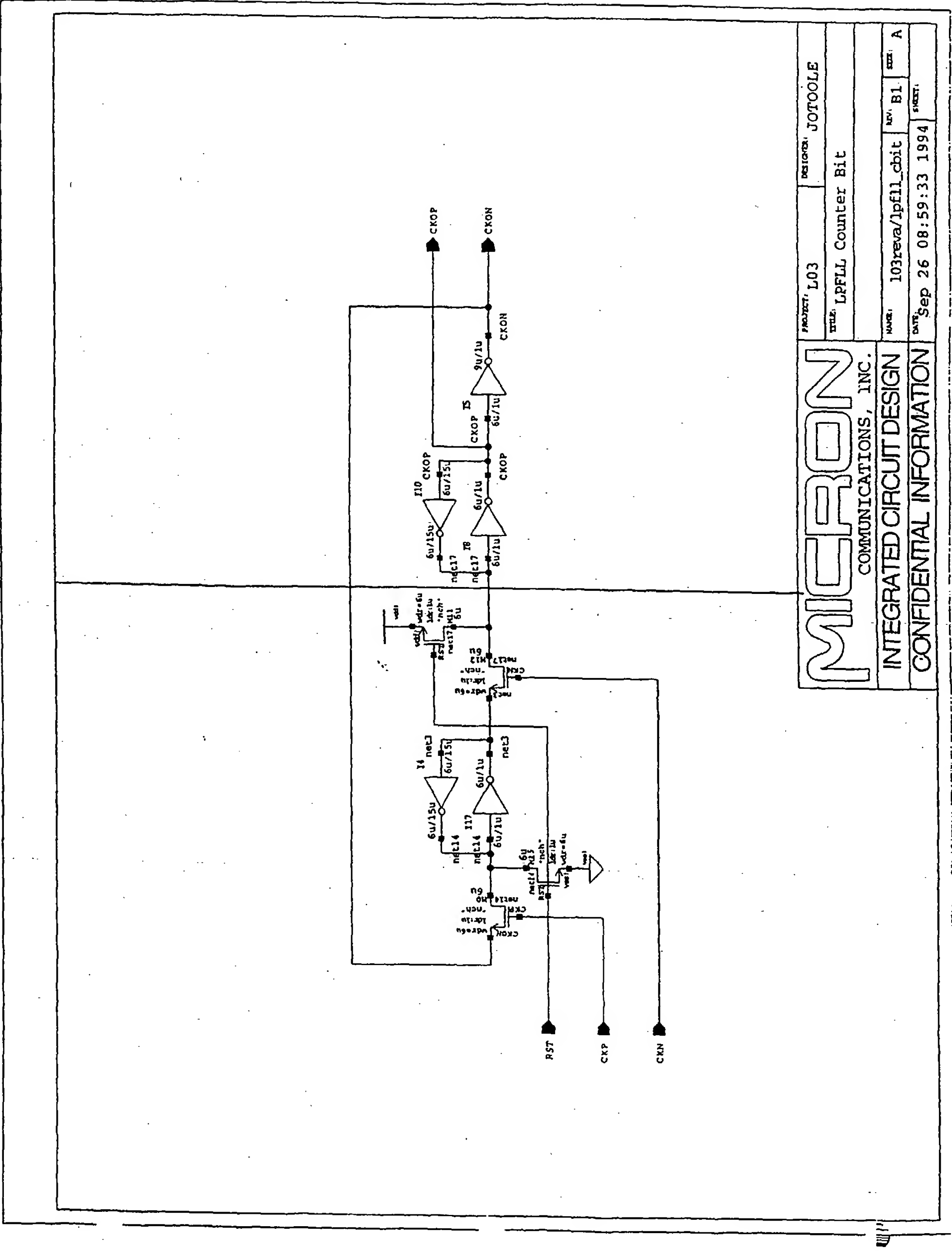
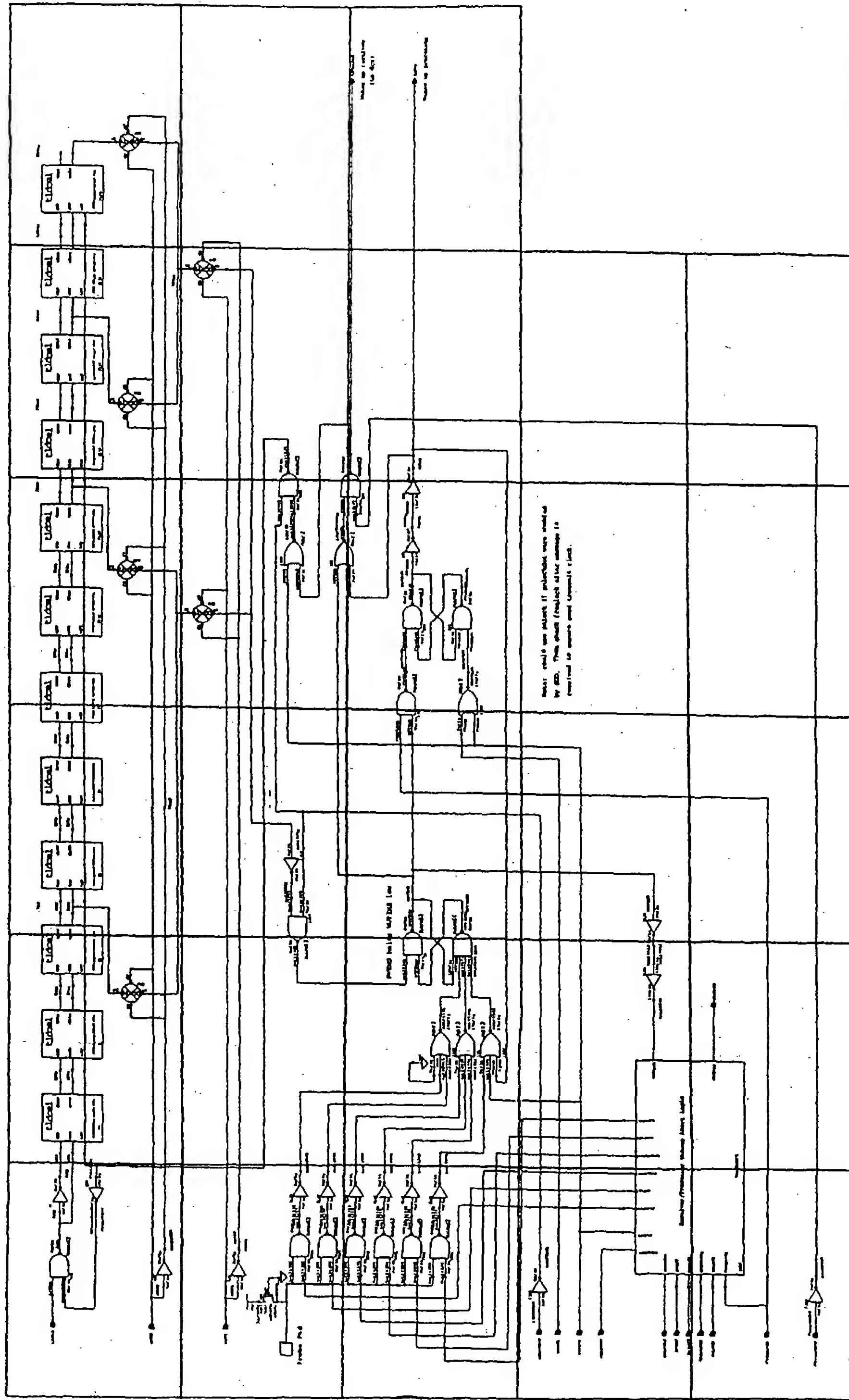


FIG. 8.03

8.04AA	8.04AB	8.04AC	8.04AD	8.04AE	8.04AF
8.04BA	8.04BB	8.04BC	8.04BD	8.04BE	8.04BF
8.04CA	8.04CB	8.04CC	8.04CD	8.04CE	8.04CF
8.04DA	8.04DB	8.04DC	8.04DD	8.04DE	
8.04EA	8.04EB	8.04EC	8.04ED	8.04EE	

II II III III



FL6.804

[illegible]

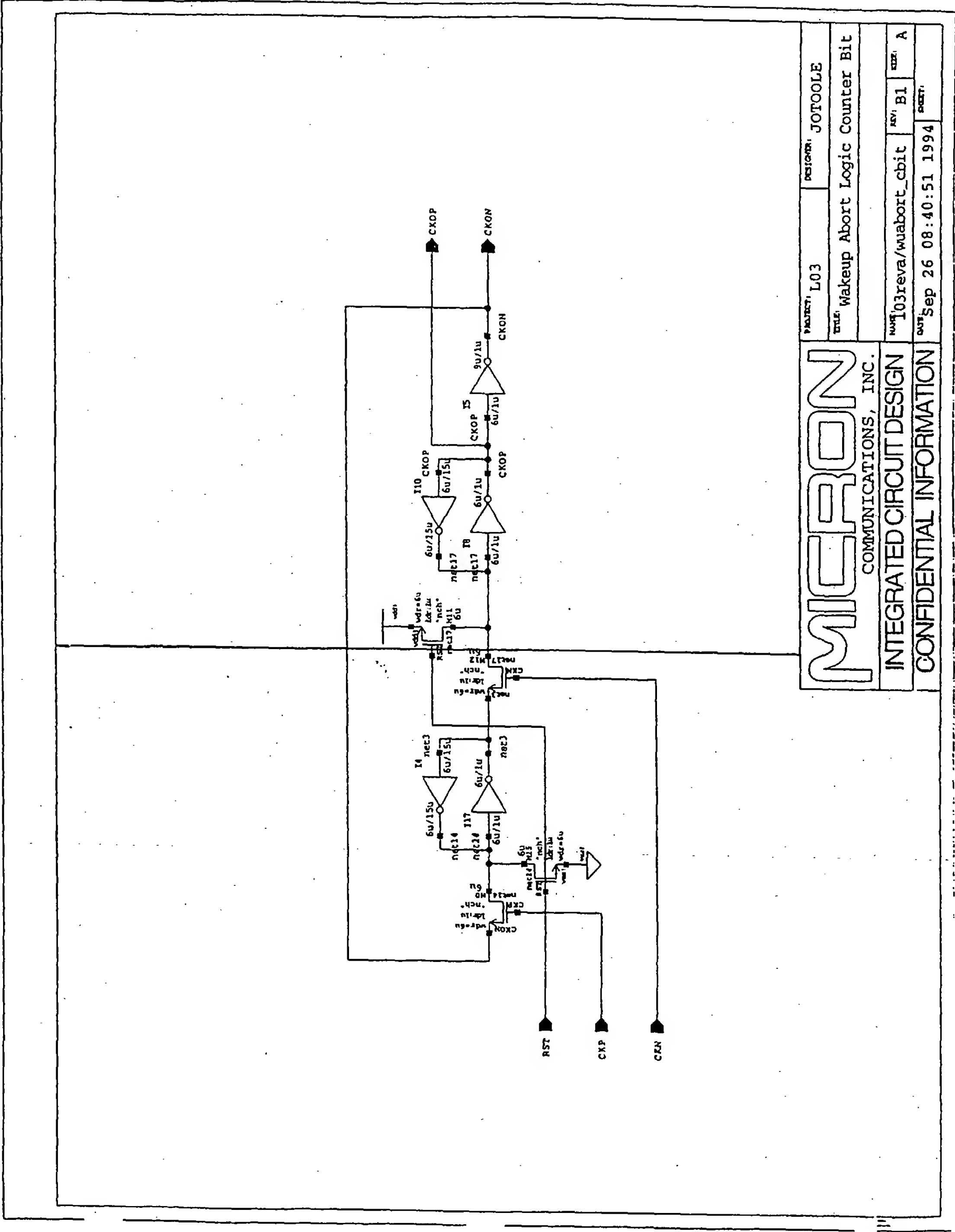
8.0401AA	8.0401AB	8.0401AC	8.0401AD	8.0401AE
8.0401BA	8.0401BB	8.0401BC	8.0401BD	8.0401BE
8.0401CA	8.0401CB	8.0401CC	8.0401CD	8.0401CE
8.0401DA	8.0401DB	8.0401DC	8.0401DD	8.0401DE

II II III III III III









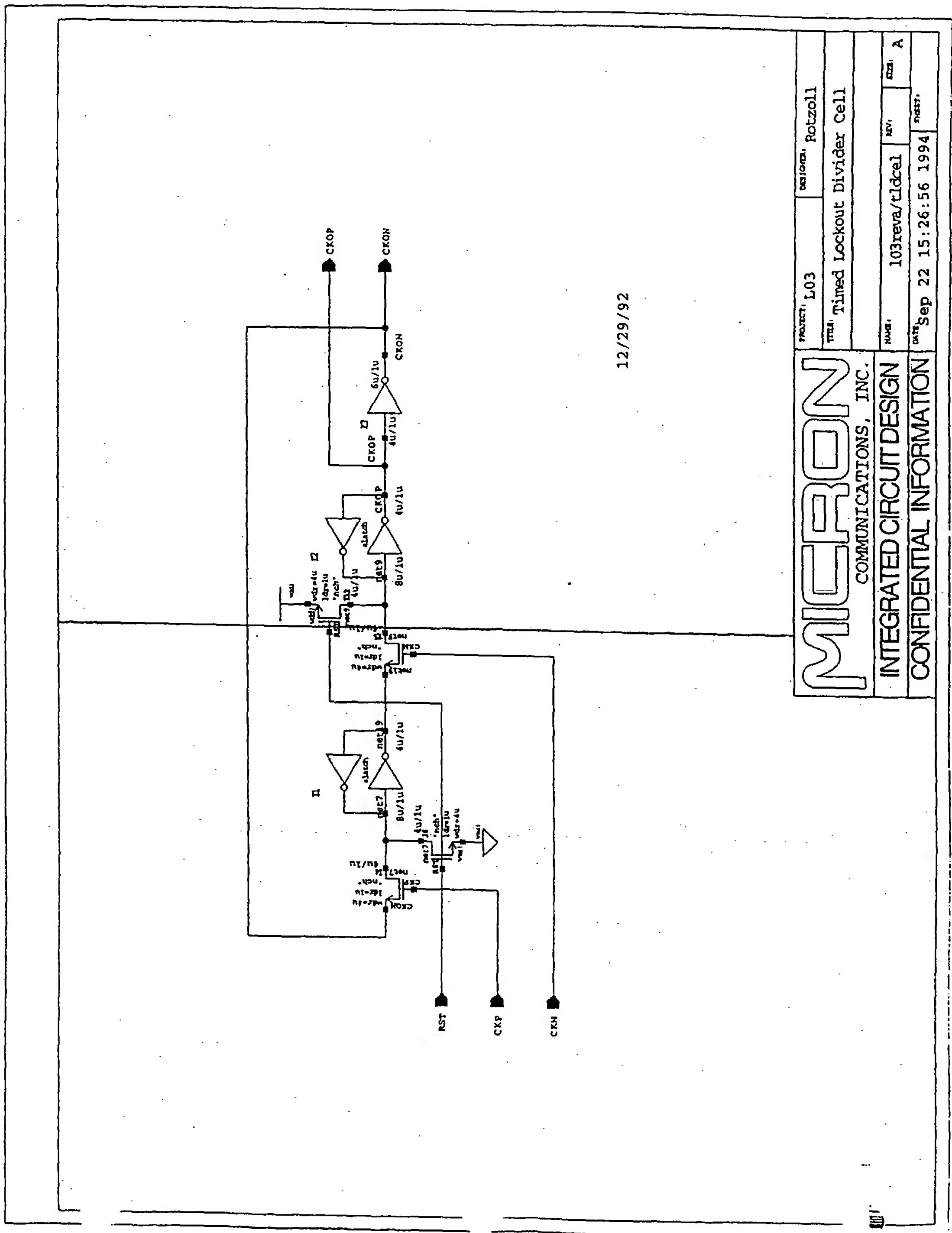
<b>MICRON</b> COMMUNICATIONS, INC.		PROJECT: L03	DESIGNER: JOTOOLE
INTEGRATED CIRCUIT DESIGN		TITLE: Wakeup Abort Logic Counter Bit	
CONFIDENTIAL INFORMATION		WUW: 103reva/wuabort_cbit	REV: B1
		DATE: Sep 26 08:40:51 1994	REV: A

Fig. 8.040101

8.0402AB

8.0402AA

8.0402



12/29/92

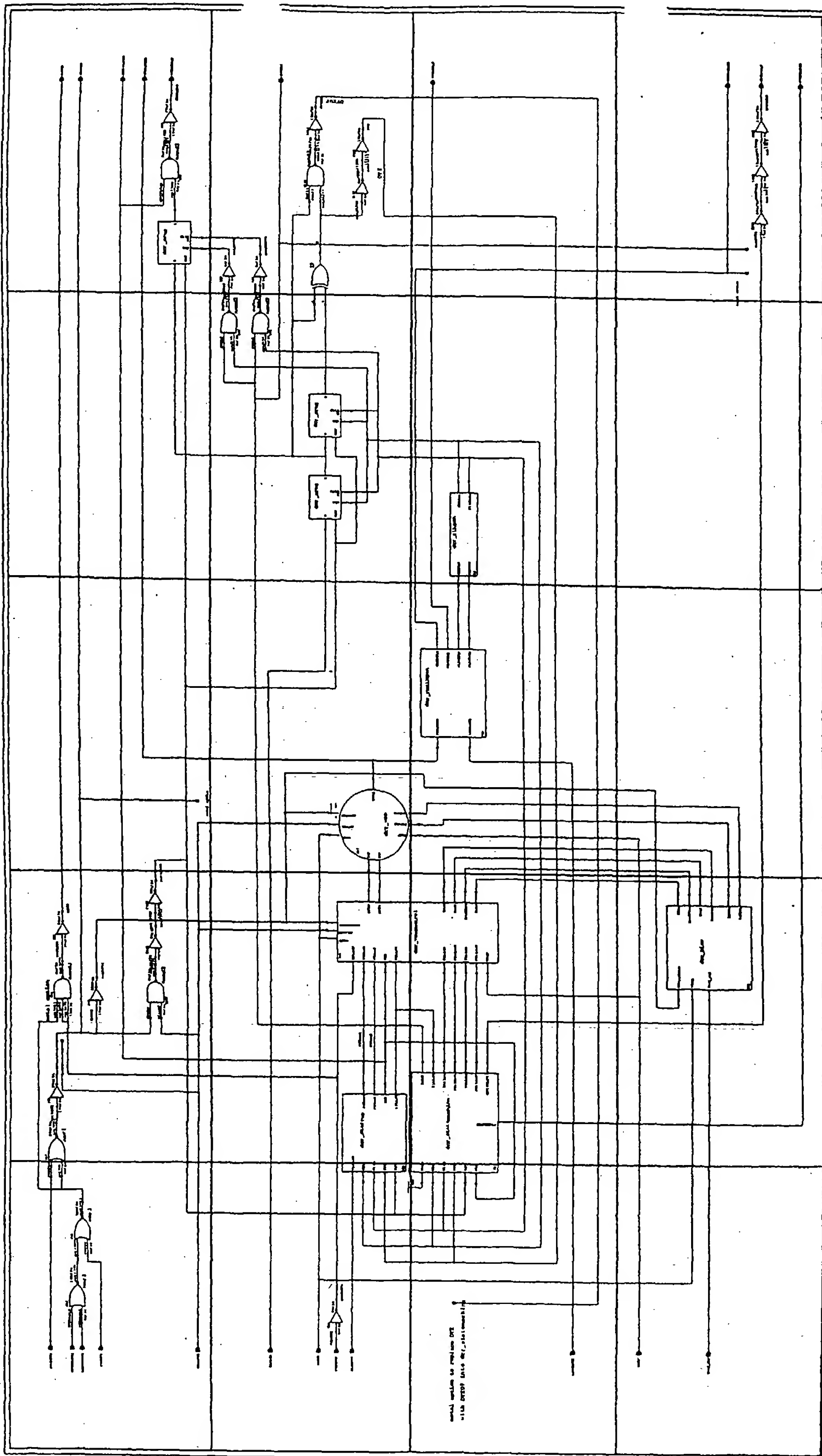
PROJECT: L03		DESIGNER: Rotzoll	
TITLE: Timed Lockout Divider Cell			
NAME: 103reva/tldcel		REV: A	SHEET: 1
DATE: Sep 22 15:26:56 1994			

**MICRON**  
COMMUNICATIONS, INC.  
INTEGRATED CIRCUIT DESIGN  
CONFIDENTIAL INFORMATION

FIG. 8.0402

8.05AA	8.05AB	8.05AC	8.05AD	8.05AE
8.05BA	8.05BB	8.05BC	8.05BD	8.05BE
8.05CA	8.05CB	8.05CC	8.05CD	8.05CE
8.05DA	8.05DB	8.05DC	8.05DD	8.05DE

EE BB.005



- (A) clocked reset logic
- (B) address bus and RAM
- (C) data bus and ROM
- (D) data bus and RAM
- (E) data bus and ROM
- (F) data bus and RAM
- (G) data bus and ROM
- (H) data bus and RAM
- (I) data bus and ROM
- (J) data bus and RAM
- (K) data bus and ROM
- (L) data bus and RAM
- (M) data bus and ROM
- (N) data bus and RAM
- (O) data bus and ROM
- (P) data bus and RAM
- (Q) data bus and ROM
- (R) data bus and RAM
- (S) data bus and ROM
- (T) data bus and RAM
- (U) data bus and ROM
- (V) data bus and RAM
- (W) data bus and ROM
- (X) data bus and RAM
- (Y) data bus and ROM
- (Z) data bus and RAM

Fig. 8.05

**MICRON**  
 COMMUNICATIONS, INC.  
 INTEGRATED CIRCUIT DESIGN  
 CONFIDENTIAL INFORMATION

DATE	DESIGNED BY	CHECKED BY
10/10/77	J. J. J.	J. J. J.

8.0501AA	8.0501AB	8.0501AC	8.0501AD	8.0501AE
8.0501BA	8.0501BB	8.0501BC	8.0501BD	8.0501BE

II II III III III III III III

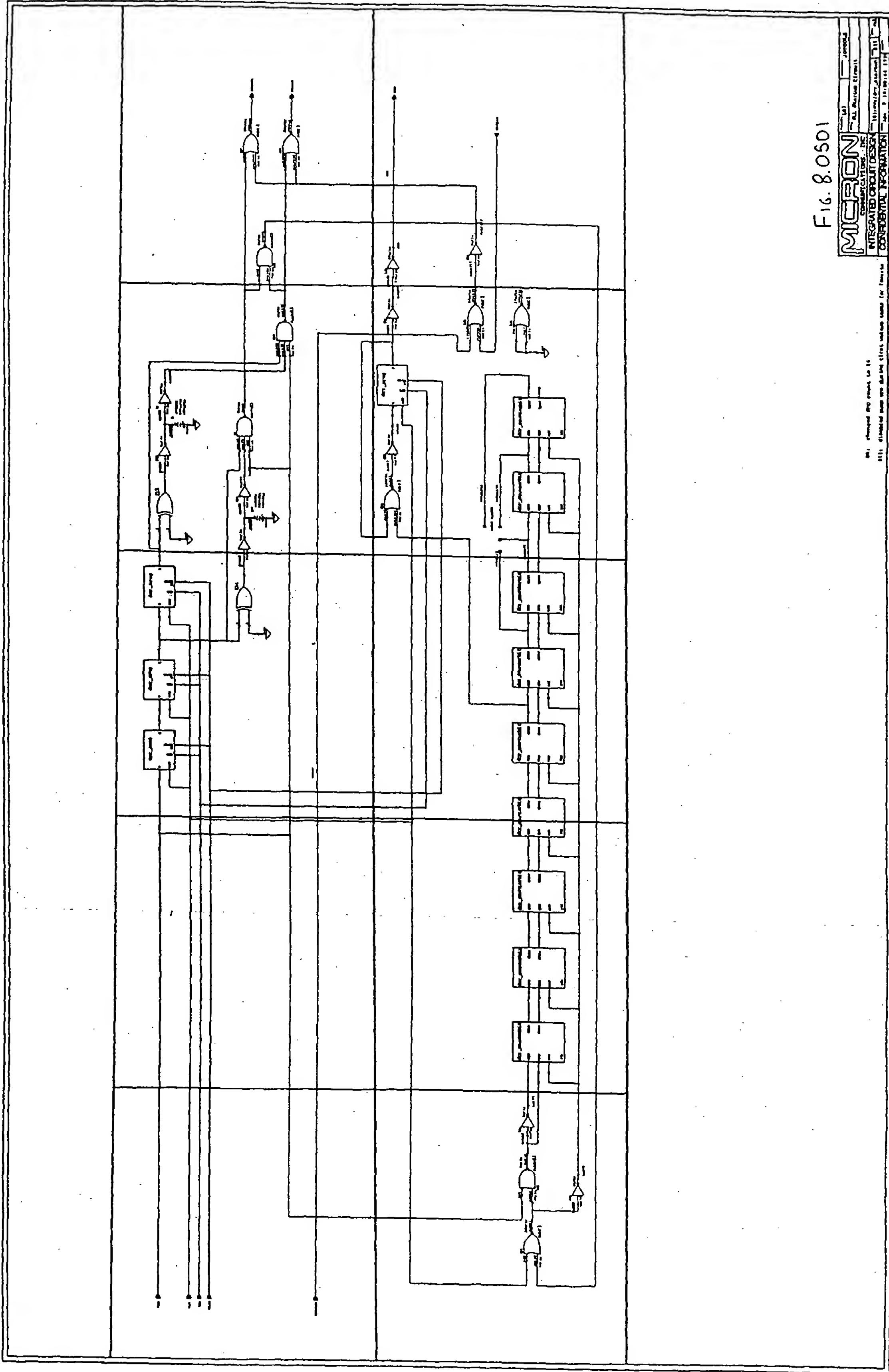


FIG. 8.0501

**MICRON**  
 CORPORATION  
 INTEGRATED CIRCUIT DESIGN  
 CONFIDENTIAL INFORMATION

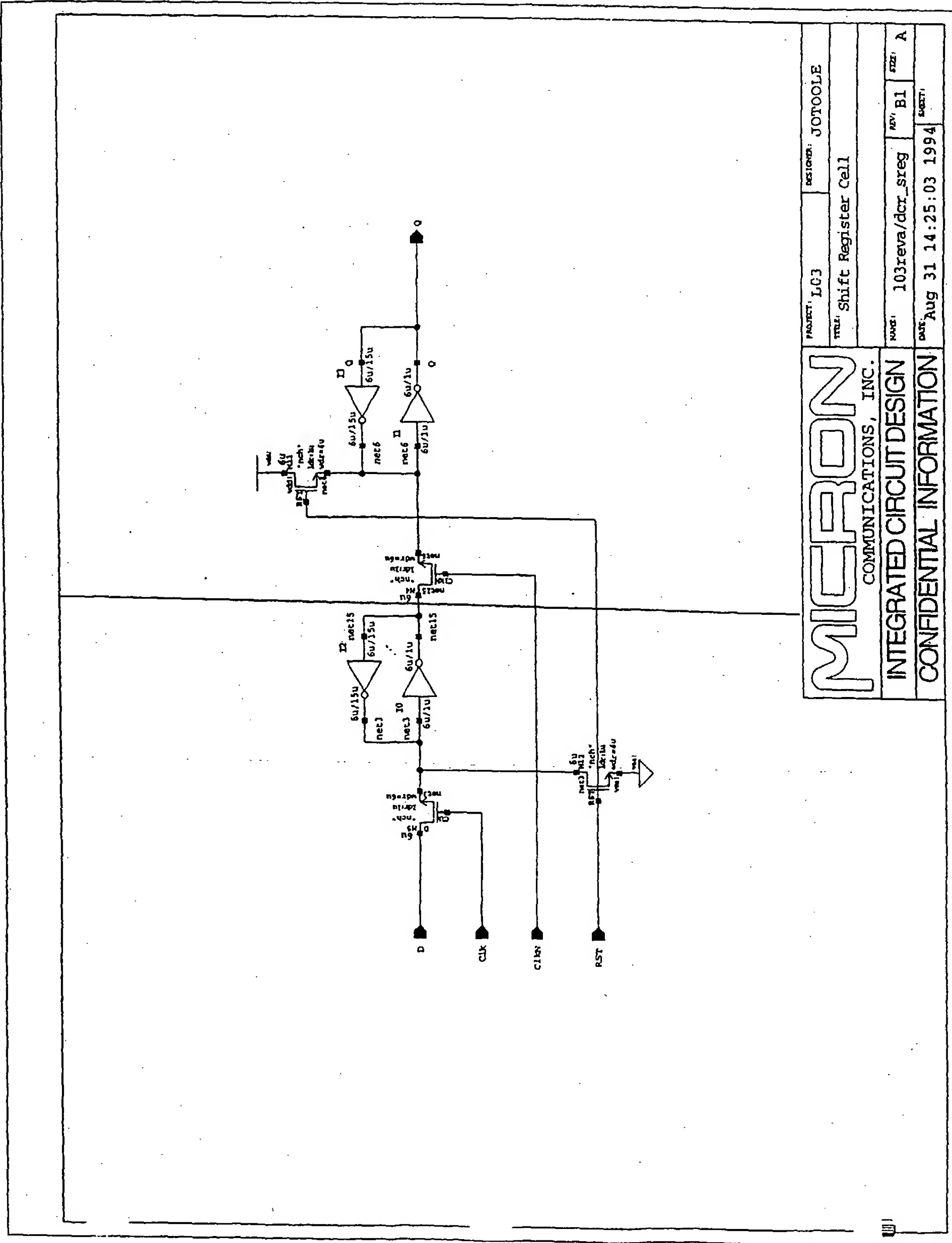
Rev. 1: Changed AND output to 14  
 All: Circled data are shown (14) values same for Rev. 1



8.050101AB

8.050101AA

8.050101AA



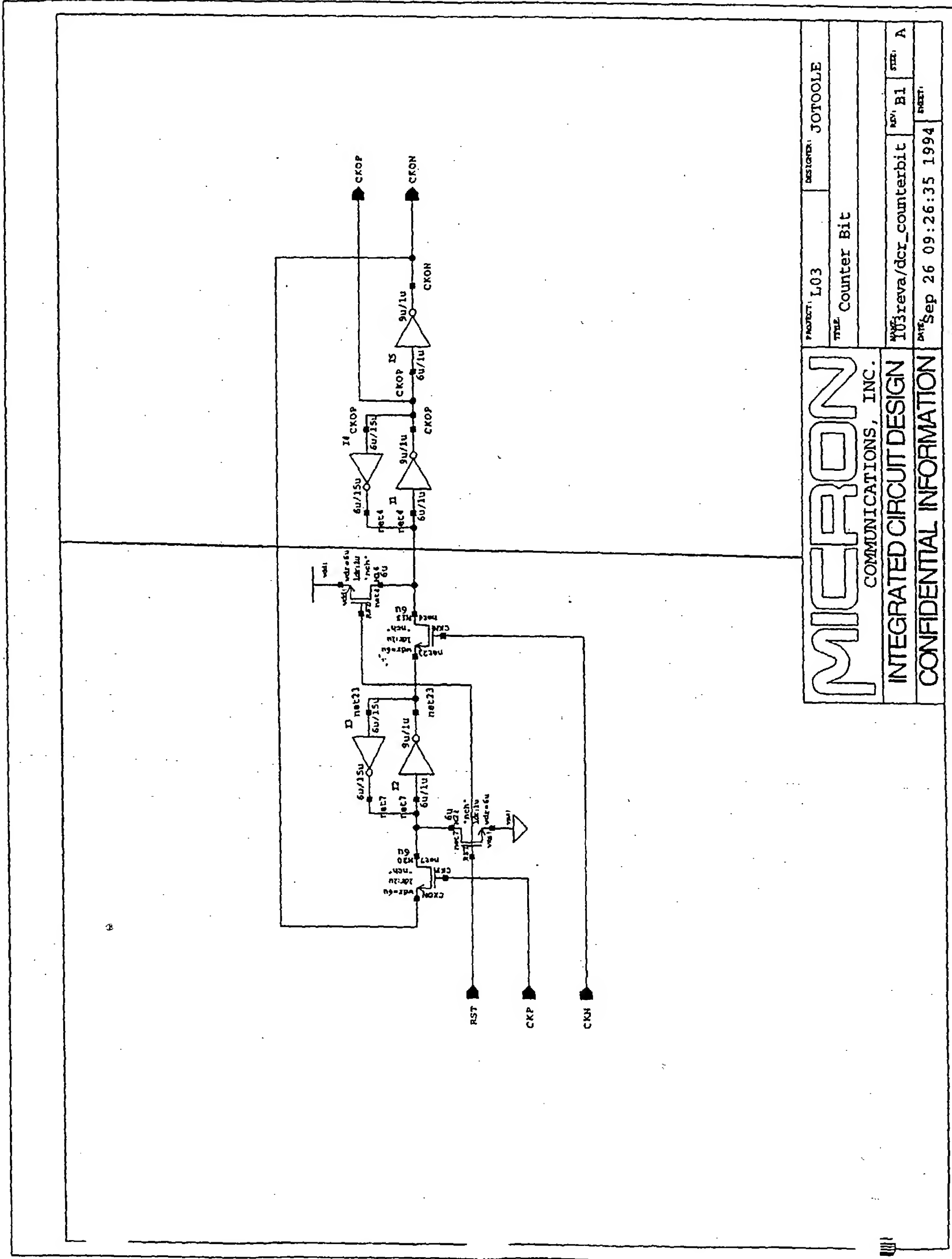
MICRON		PROJECT: LC3	DESIGNER: JOTOOLE
COMMUNICATIONS, INC.		TITLE: Shift Register Cell	
INTEGRATED CIRCUIT DESIGN		NOVA: 103reva/dcr_sreg	REV: B1
CONFIDENTIAL INFORMATION		DATE: Aug 31 14:25:03 1994	SIZE: A

FIG. 8.050101

8.050102AB

8.050102AA

8.050102



<b>MICRON</b>		PROJECT: L03	DESIGNER: JOTOOLE
COMMUNICATIONS, INC.		TITLE: Counter Bit	
INTEGRATED CIRCUIT DESIGN		W33 reva/dcr_counterbit	REV: B1
CONFIDENTIAL INFORMATION		DATE: Sep 26 09:26:35 1994	SHEET: A

Fig. 8.050102

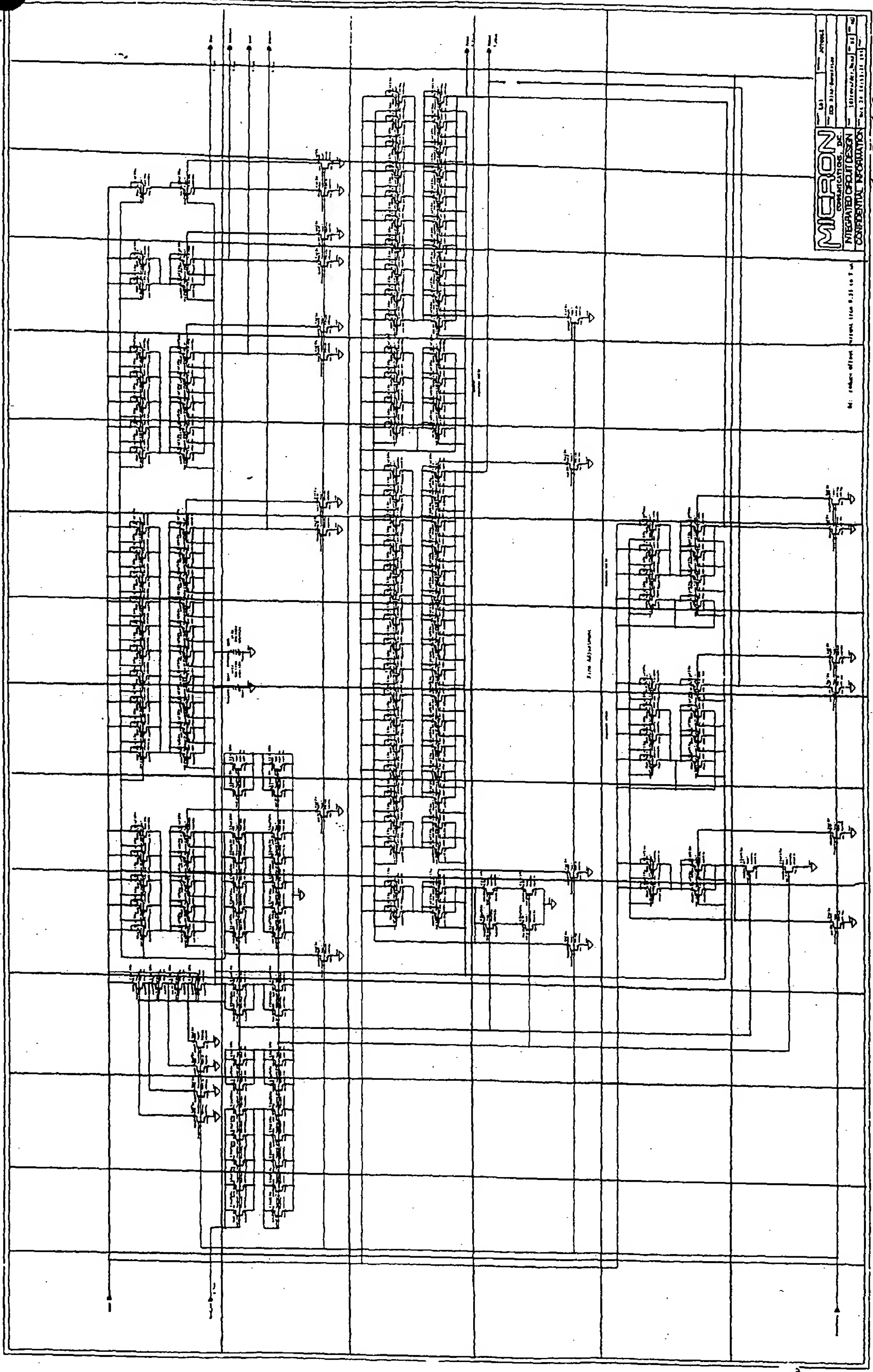
8.0502AA	8.0502AB	8.0502AC	8.0502AD
8.0502BA	8.0502BB	8.0502BC	8.0502BD
8.0502CA	8.0502CB	8.0502CC	8.0502CD

EE 88.0502



8.0503AA	8.0503AB	8.0503AC	8.0503AD	8.0503AE	8.0503AF	8.0503AG	8.0503AH	8.0503AI	8.0503AJ	8.0503AK	8.0503AL	8.0503AM	8.0503AN	8.0503AO
8.0503BA	8.0503BB	8.0503BC	8.0503BD	8.0503BE	8.0503BF	8.0503BG	8.0503BH	8.0503BI	8.0503BJ	8.0503BK	8.0503BL	8.0503BM	8.0503BN	8.0503BO
8.0503CA	8.0503CB	8.0503CC	8.0503CD	8.0503CE	8.0503CF	8.0503CG	8.0503CH	8.0503CI	8.0503CJ	8.0503CK	8.0503CL	8.0503CM	8.0503CN	8.0503CO
8.0503DA	8.0503DB	8.0503DC	8.0503DD	8.0503DE	8.0503DF	8.0503DG	8.0503DH	8.0503DI	8.0503DJ	8.0503DK	8.0503DL	8.0503DM	8.0503DN	8.0503DO
8.0503EA	8.0503EB	8.0503EC	8.0503ED	8.0503EE	8.0503EF	8.0503EG	8.0503EH	8.0503EI	8.0503EJ	8.0503EK	8.0503EL	8.0503EM	8.0503EN	
8.0503FA	8.0503FB	8.0503FC	8.0503FD	8.0503FE	8.0503FF	8.0503FG	8.0503FH	8.0503FI	8.0503FJ	8.0503FK	8.0503FL	8.0503FM	8.0503FN	


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8.0504AA	8.0504AB	8.0504AC	8.0504AD	
8.0504BA	8.0504BB	8.0504BC	8.0504BD	
8.0506CA	8.0504CB	8.0504CC	8.0504CD	8.0504CE
8.0504DA	8.0504DB	8.0504DC	8.0504DD	8.0504DE
8.0504EA	8.0504EB	8.0504EC	8.0504ED	8.0504EE

EE BB.0500-1

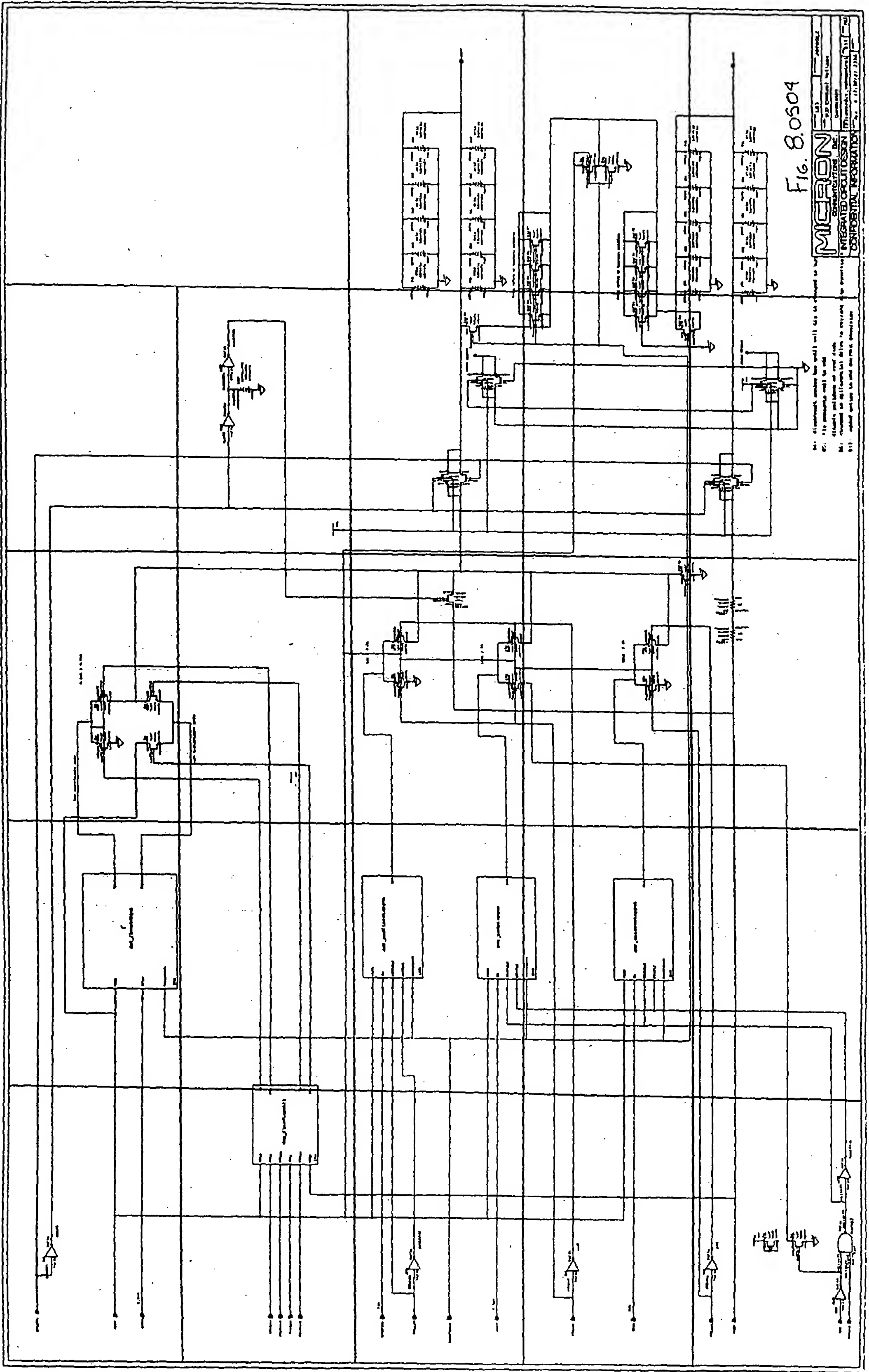


FIG. 8.0504

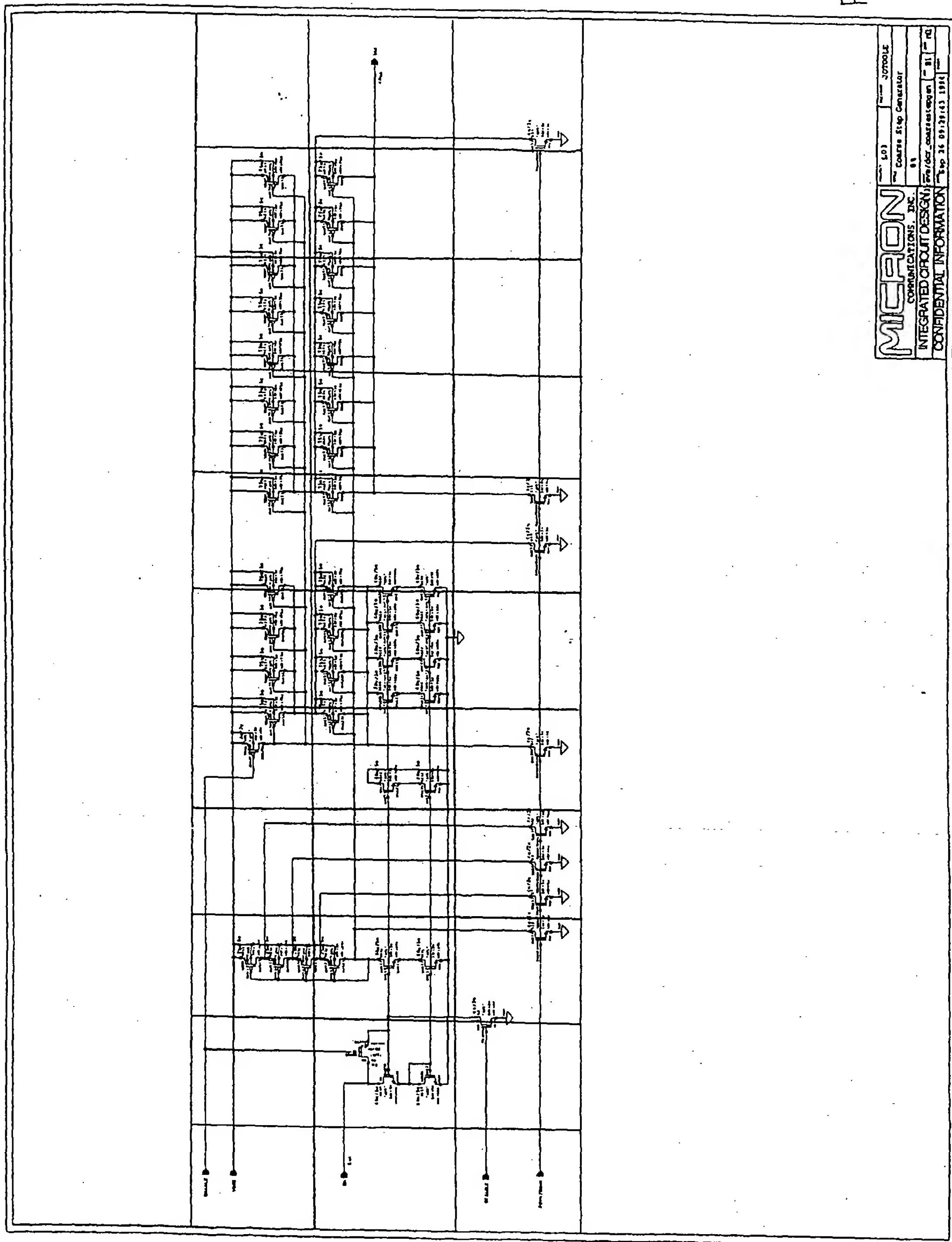
**MICRON**  
 INTEGRATED CIRCUITS  
 CORPORATION  
 3600 WEST 14TH AVENUE  
 DENVER, COLORADO 80202  
 (303) 751-1000

NOTES:  
 1. All dimensions are in inches.  
 2. All dimensions are in millimeters.  
 3. All dimensions are in centimeters.  
 4. All dimensions are in meters.

8.050401AA	8.050401AB	8.050401AC	8.050401AD	8.050401AE	8.050401AF	8.050401AG	8.050401AH	8.050401AJ	8.050401AK
8.050401BA	8.050401BB	8.050401BC	8.050401BD	8.050401BE	8.050401BF	8.050401BG	8.050401BH	8.050401BJ	8.050401BK
8.050401CA	8.050401CB	8.050401CC	8.050401CD	8.050401CE	8.050401CF	8.050401CG	8.050401CH	8.050401CJ	8.050401CK

Итого 8.050401

Fig 8.050401



<b>MICRON</b> COMMUNICATIONS, INC. INTEGRATED CIRCUIT DESIGN	LO3	20700LE
	Coarse Step Generator	
	81	
	Order: 08/29/83 1983	
CONFIDENTIAL INFORMATION		

8.050402AA	8.050402AB	8.050402AC	8.050402AD	8.050402AE	8.050402AF	8.050402AG	8.050402AH	8.050402AI	8.050402AJ
8.050402BA	8.050402BB	8.050402BC	8.050402BD	8.050402BE	8.050402BF	8.050402BG	8.050402BH	8.050402BI	8.050402BJ
8.050402CA	8.050402CB	8.050402CC	8.050402CD	8.050402CE	8.050402CF	8.050402CG	8.050402CH	8.050402CI	8.050402CJ

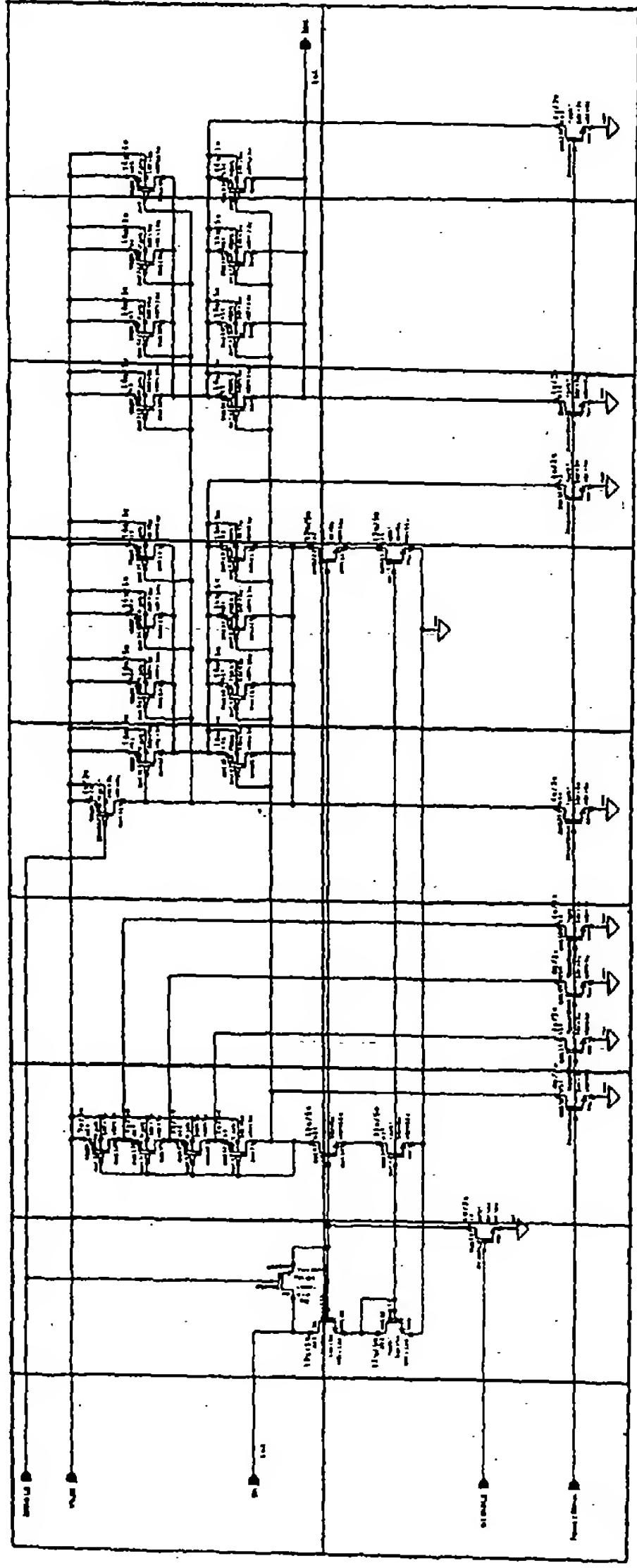
BB.050402



8.050403AA	8.050403AB	8.050403AC	8.050403AD	8.050403AE	8.050403AF	8.050403AG	8.050403AH	8.050403AI
8.050403BA	8.050403BB	8.050403BC	8.050403BD	8.050403BE	8.050403BF	8.050403BG	8.050403BH	8.050403BI

EE 88.00500-1003

Fig. 8.050403



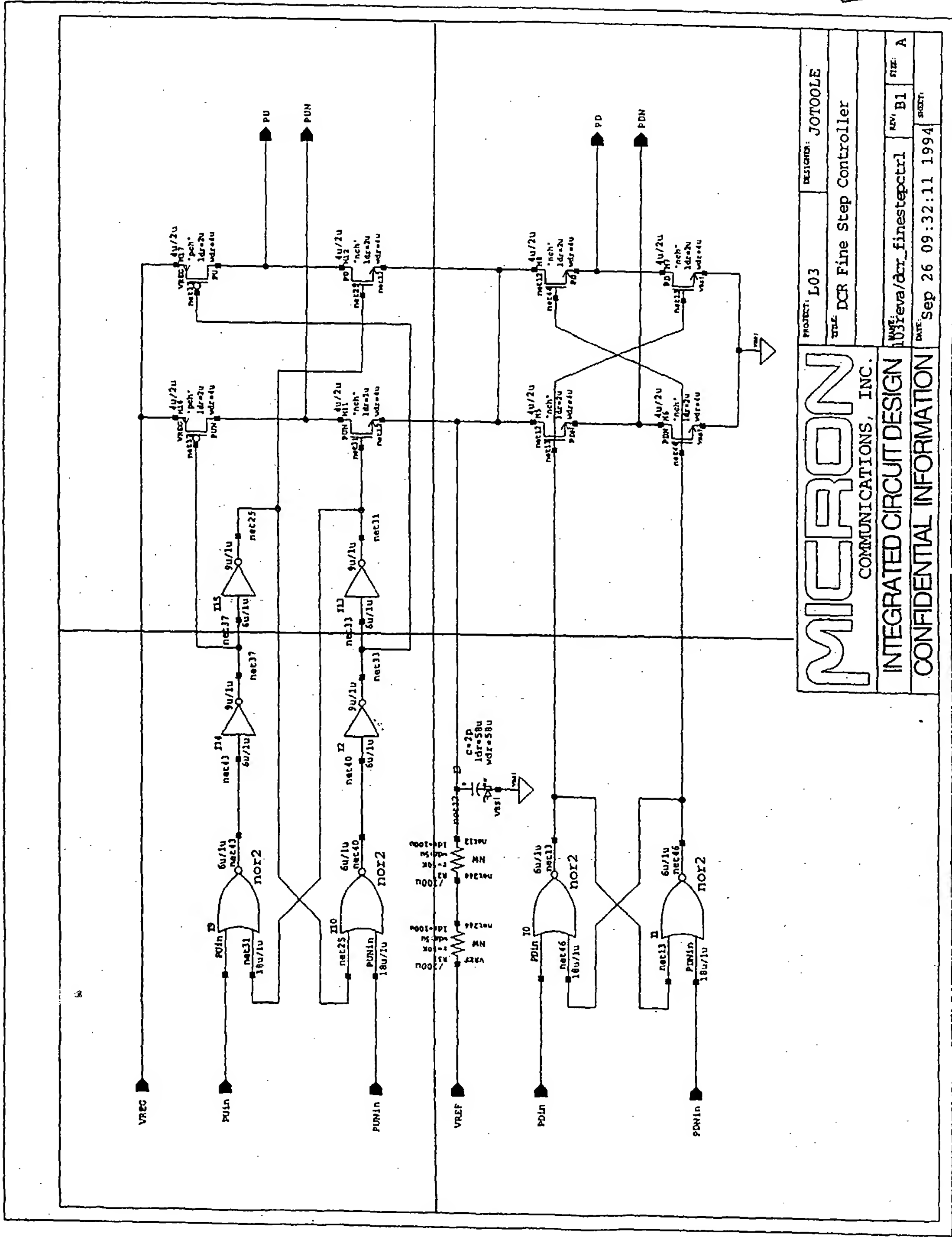
**MICRON**  
COMMUNICATIONS, INC.  
INTEGRATED CIRCUIT DESIGN  
CONFIDENTIAL INFORMATION

Lot	101	JOYCE
Medium Flow Stop Generator	0.21	
Integrated Circuit Design	0.21	rd
Confidential Information	0.21	rd



8.050404AA	8.050404AB
8.050404BA	8.050404BB

Ex 8.050404



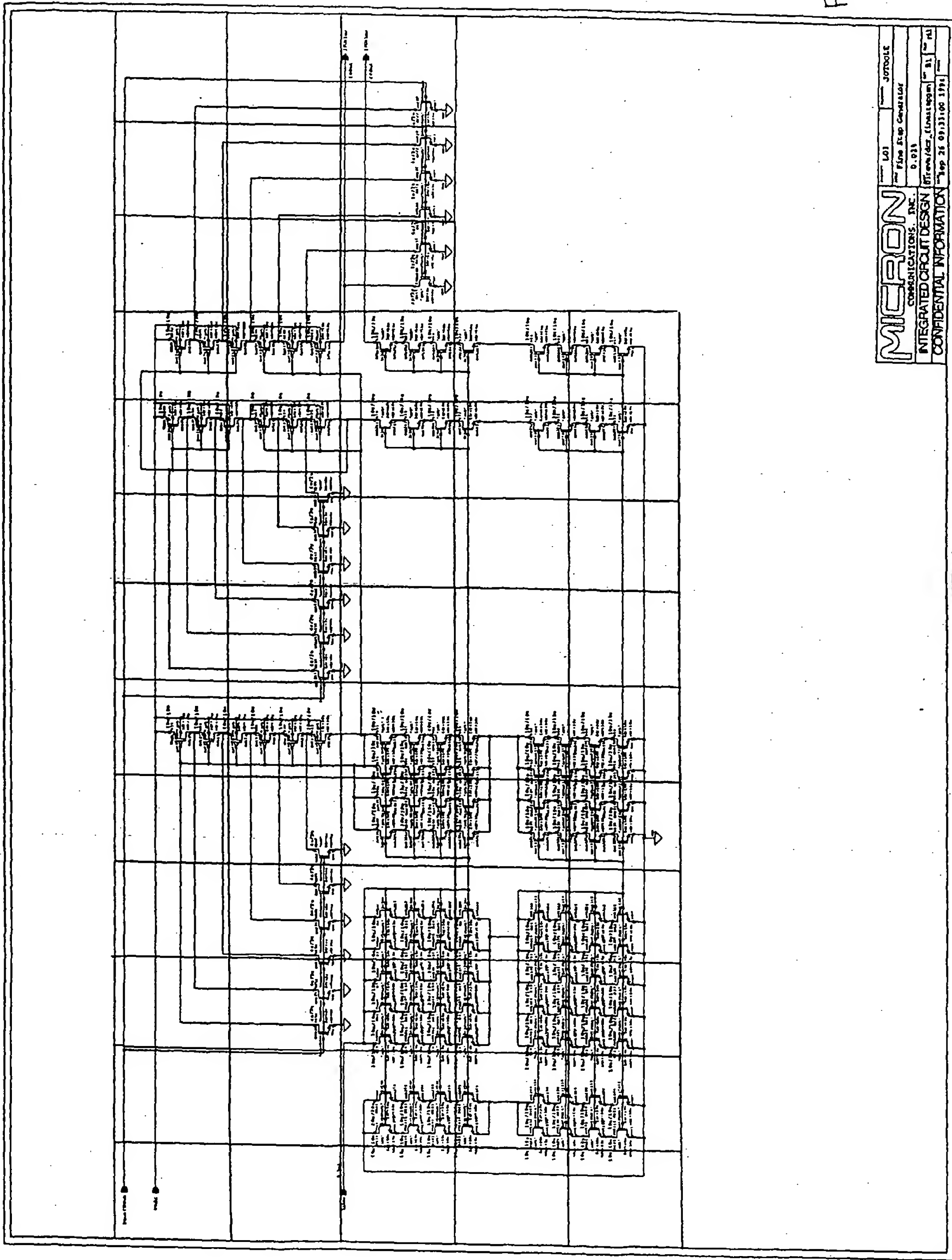
MICRON				COMMUNICATIONS, INC.	
INTEGRATED CIRCUIT DESIGN					
CONFIDENTIAL INFORMATION					
PROJECT: L03		DESIGNER: JOTOOLE			
TITLE: DCR Fine Step Controller					
NAME: J03fava/dcr_finestepctrl		REV: B1		SIZE: A	
DATE: Sep 26 09:32:11 1994		SHEET: 1			

FIG. 8.050404

8.050405AA	8.050405AB	8.050405AC	8.050405AD	8.050405AE	8.050405AF	8.050405AG	8.050405AH	8.050405AI	8.050405AJ	8.050405AK	8.050405AL	8.050405AM
8.050405BA	8.050405BB	8.050405BC	8.050405BD	8.050405BE	8.050405BF	8.050405BG	8.050405BH	8.050405BI	8.050405BJ	8.050405BK	8.050405BL	8.050405BM
8.050405CA	8.050405CB	8.050405CC	8.050405CD	8.050405CE	8.050405CF	8.050405CG	8.050405CH	8.050405CI	8.050405CJ	8.050405CK	8.050405CL	8.050405CM
8.050405DA	8.050405DB	8.050405DC	8.050405DD	8.050405DE	8.050405DF	8.050405DG	8.050405DH	8.050405DI	8.050405DJ			
8.050405EA	8.050405EB	8.050405EC	8.050405ED	8.050405EE	8.050405EF	8.050405EG	8.050405EH	8.050405EI	8.050405EJ			

IF II 05 88.005000-0005

FIG 8.050405



MICRON		LOI	JOTDILE
COMMUNICATIONS, INC.		Film Strip Condition	
INTEGRATED CIRCUIT DESIGN		0.011	
CONFIDENTIAL INFORMATION		ET:ena/daz, f:naast:epm	SI: M
		Top 26 09:31:00 1991	



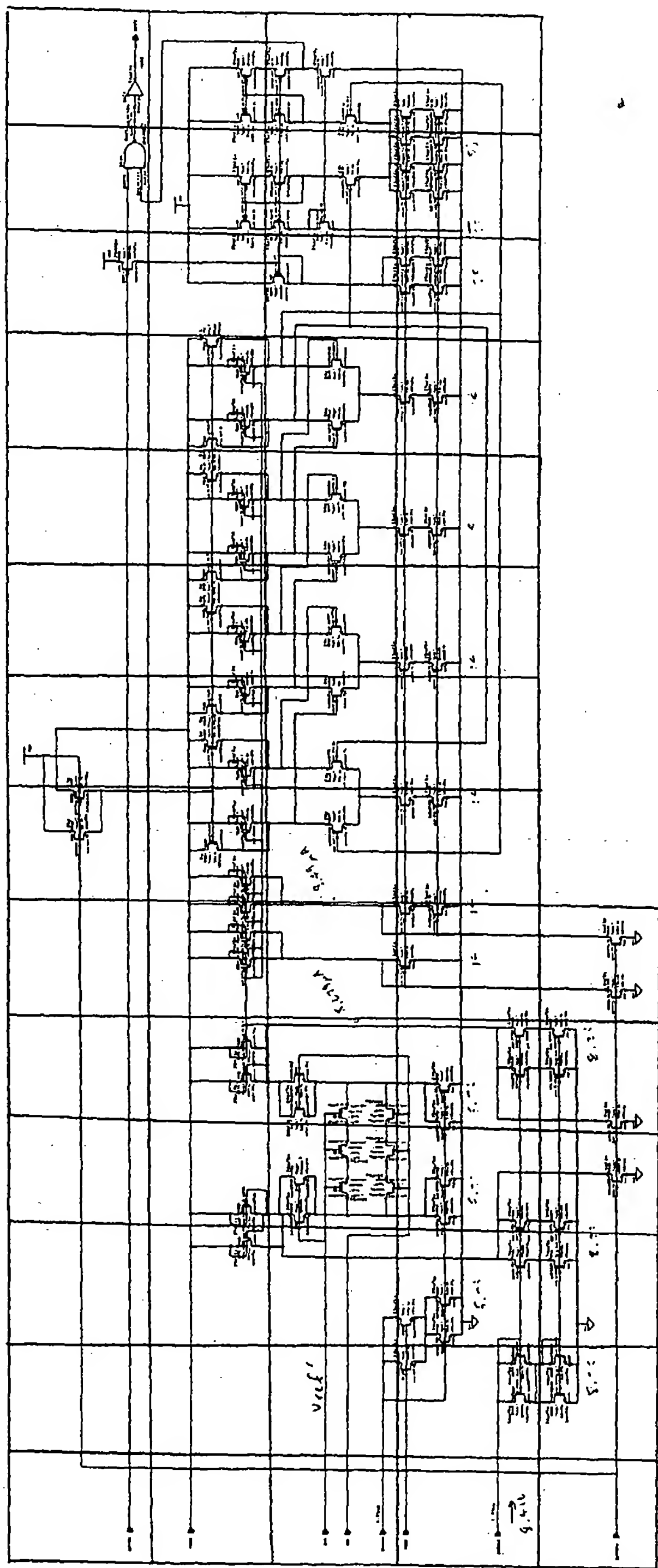


FIG. 8.0505

238A

8.0506AA	8.0506AB
8.0506BA	8.0506BB

II BB.0506

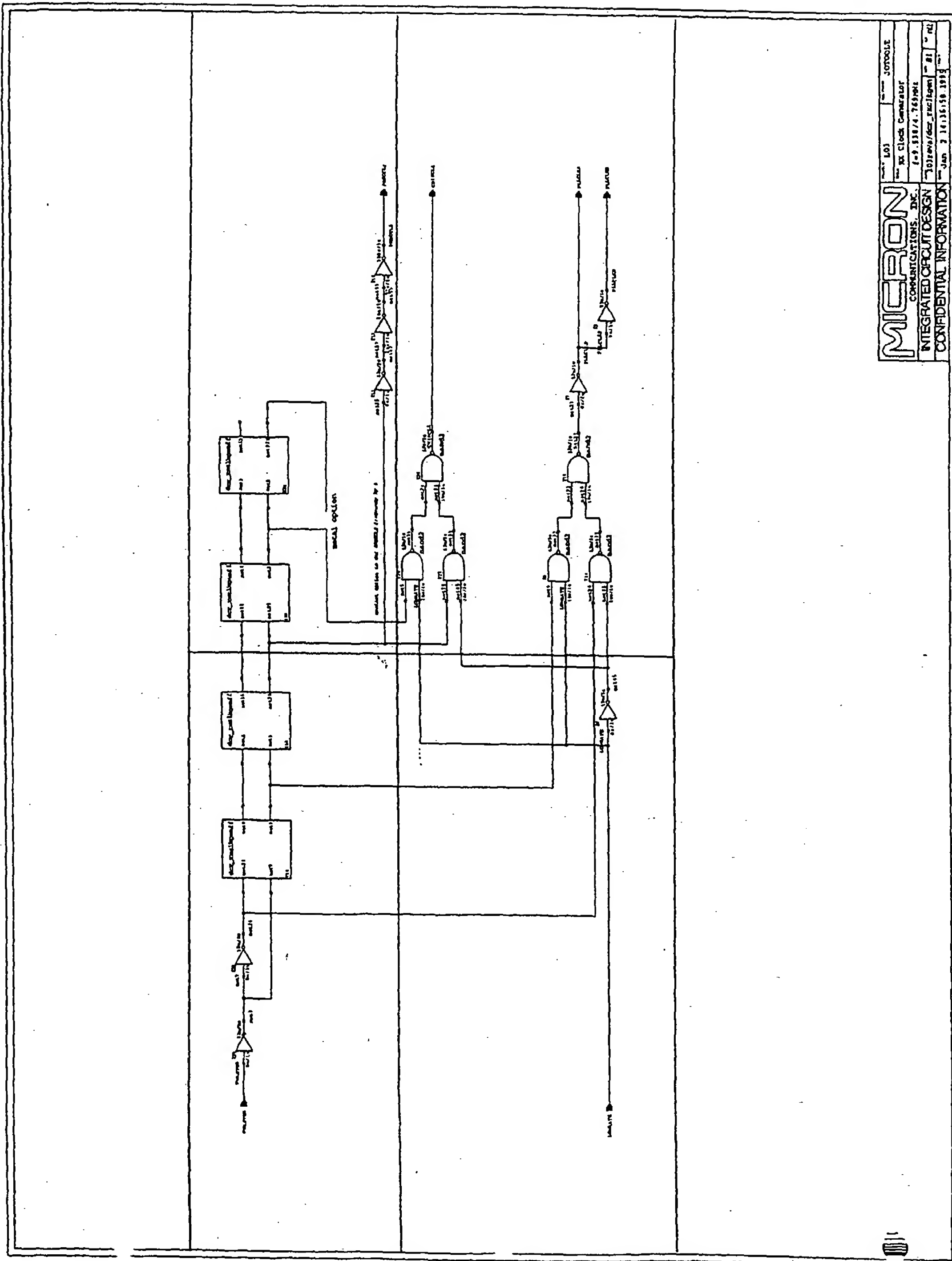


FIG. 8.0506

<b>MICRON</b>		LO3	JOT001E
COMMUNICATIONS, INC.		32 Clock Generator	
INTEGRATED CIRCUIT DESIGN		1-9 11874-769M1	
CONFIDENTIAL INFORMATION		101000/002 101000/002 101000/002 101000/002	
		Jan 2 10:35:58 1983	



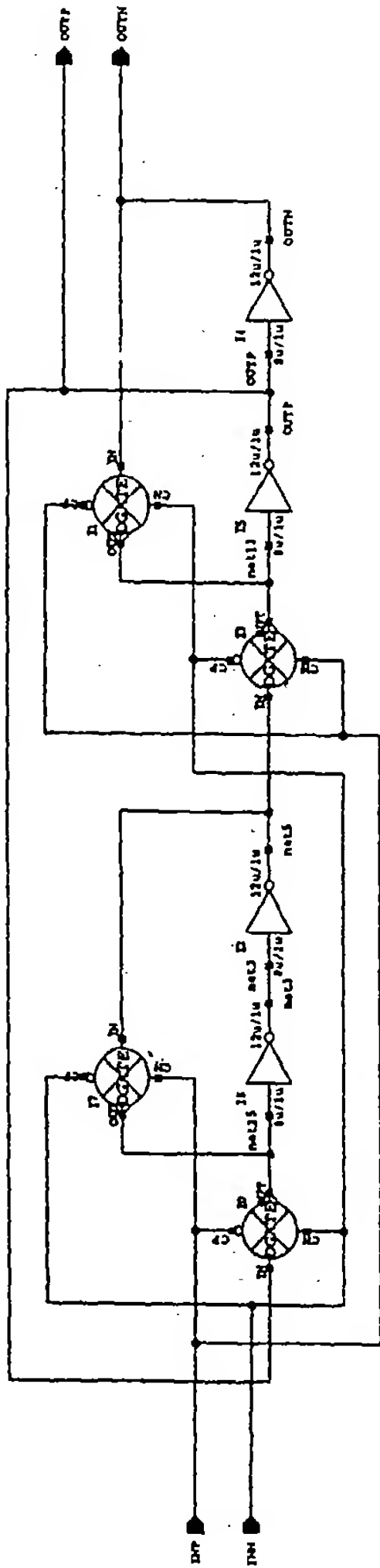


FIG. 8.050601

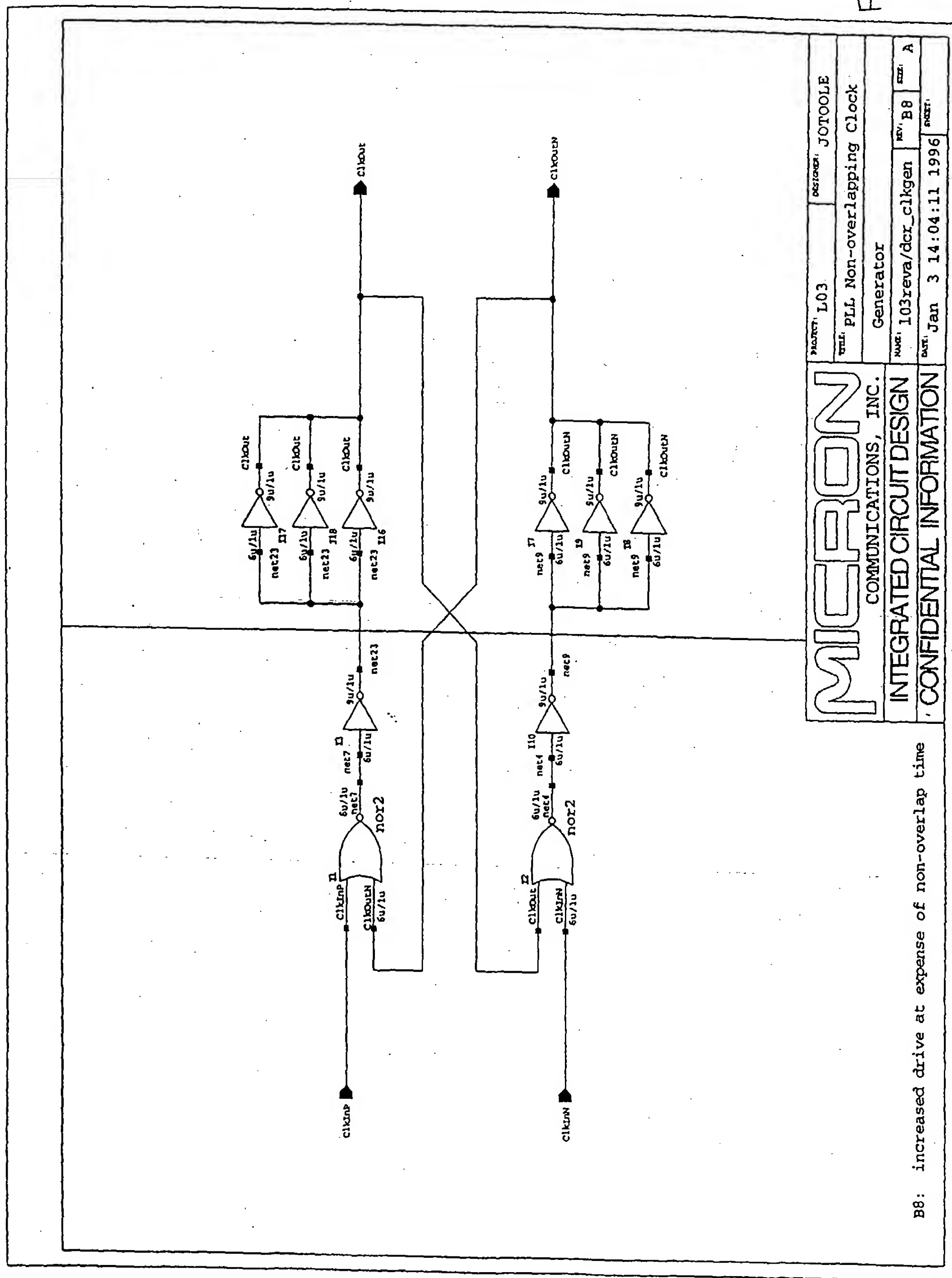
MICRON		PROJECT: L03	REVISION: J0700LE
COMMUNICATIONS, INC.		NEW Rx Clock Generator	
INTEGRATED CIRCUIT DESIGN		Flip-Flop	
CONFIDENTIAL INFORMATION		Y03rev0/dcr_rxclkgenff	Rev. B1
		Rev. Sep 26 09:36:05 1994	Rev. 1112

--	--

8.0507AB

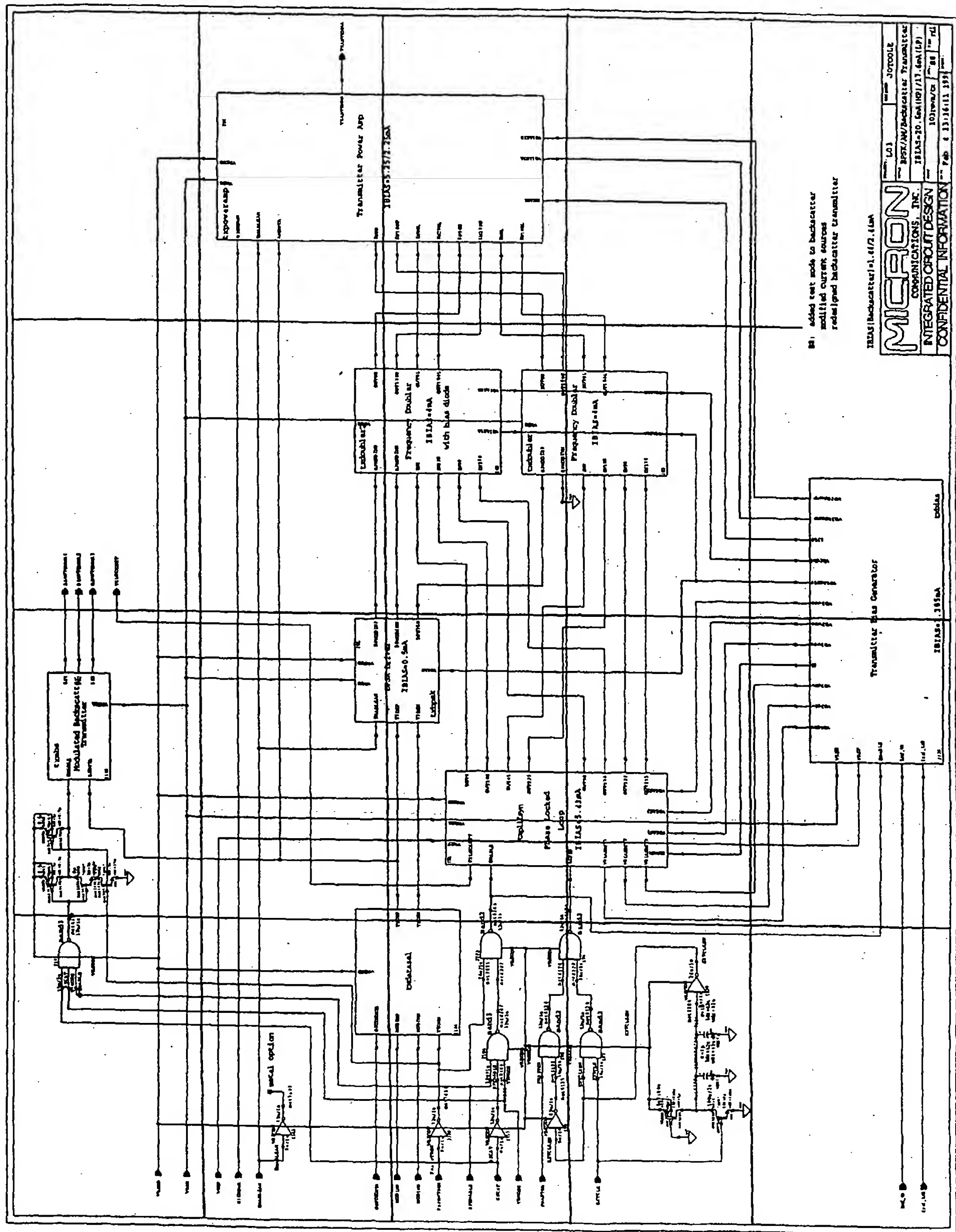
8.0507AA

EX-88.0507



8.06AA	8.06AB	8.06AC	8.06AD
8.06BA	8.06BB	8.06BC	8.06BD
8.06CA	8.06CB	8.06CC	8.06CD
8.06DA	8.06DB	8.06DC	8.06DD
8.06EA	8.06EB	8.06EC	8.06ED

IL 11 001 88.0016



88) added test mode to backscatter  
modified current source  
redesigned backscatter transmitter

[illegible]

# INNOVATION

**COMMUNICATIONS, INC.**

INTEGRATED CIRCUIT DESIGN  
CONFIDENTIAL INFORMATION

---

8.0601AA	8.0601AB
8.0601BA	8.0601BB

II II III III III III III III



8.060101AA	8.060101AB	8.060101AC
8.060101BA	8.060101BB	8.060101BC
8.060101CA	8.060101CB	8.060101CC

IF II 037 BB.006000 II 00 II



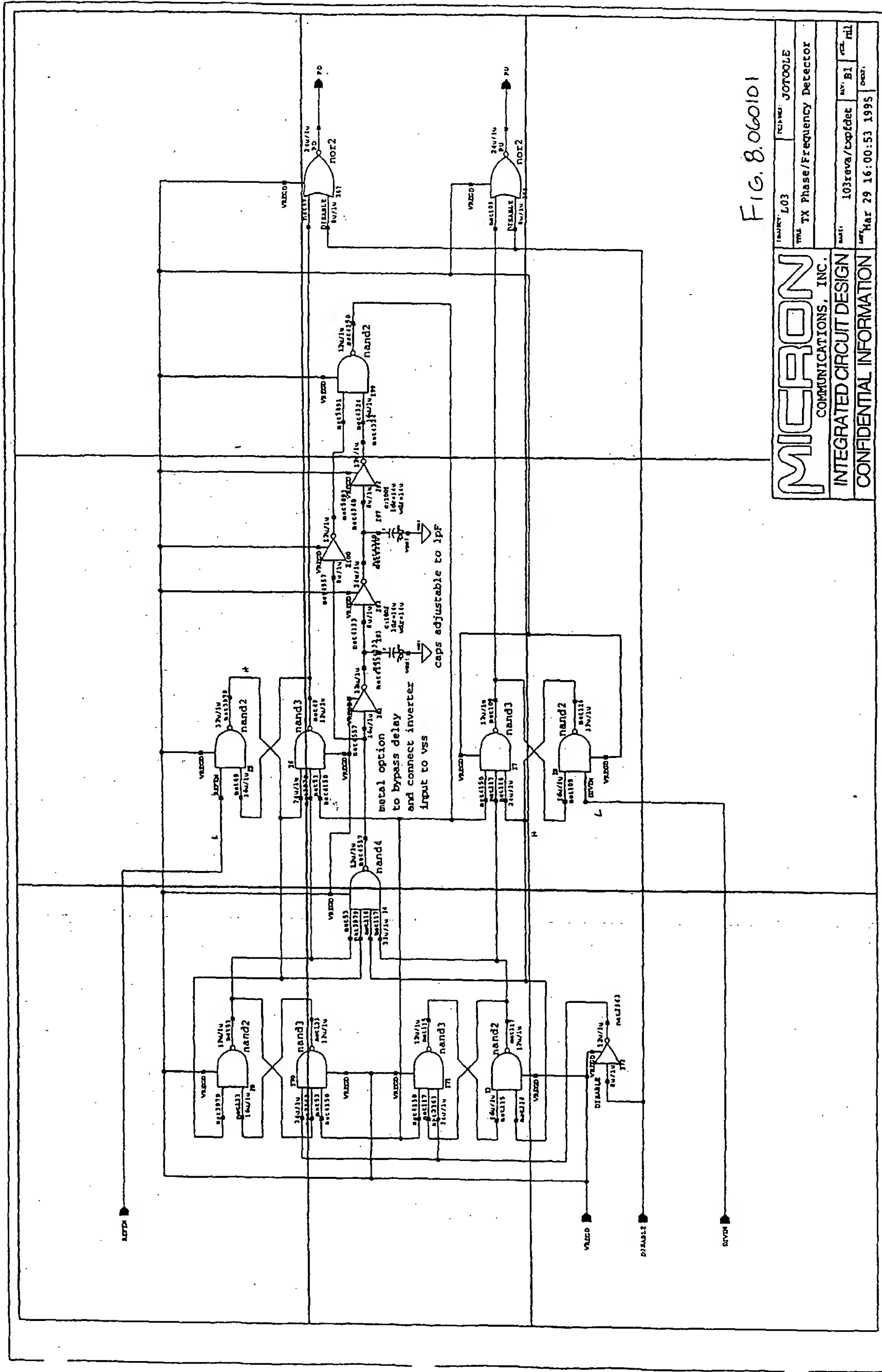


FIG. 8.060101

MICRON		FIG. 8.060101	NAME: JOTOOLE
COMMUNICATIONS, INC.		TX Phase/Frequency Detector	
INTEGRATED CIRCUIT DESIGN		103revs/Expdet	REV B1
CONFIDENTIAL INFORMATION		Mar 29 16:00:53 1995	DESIGN

8.060102AA	8.060102AB
8.060102BA	8.060102BB

8.060102

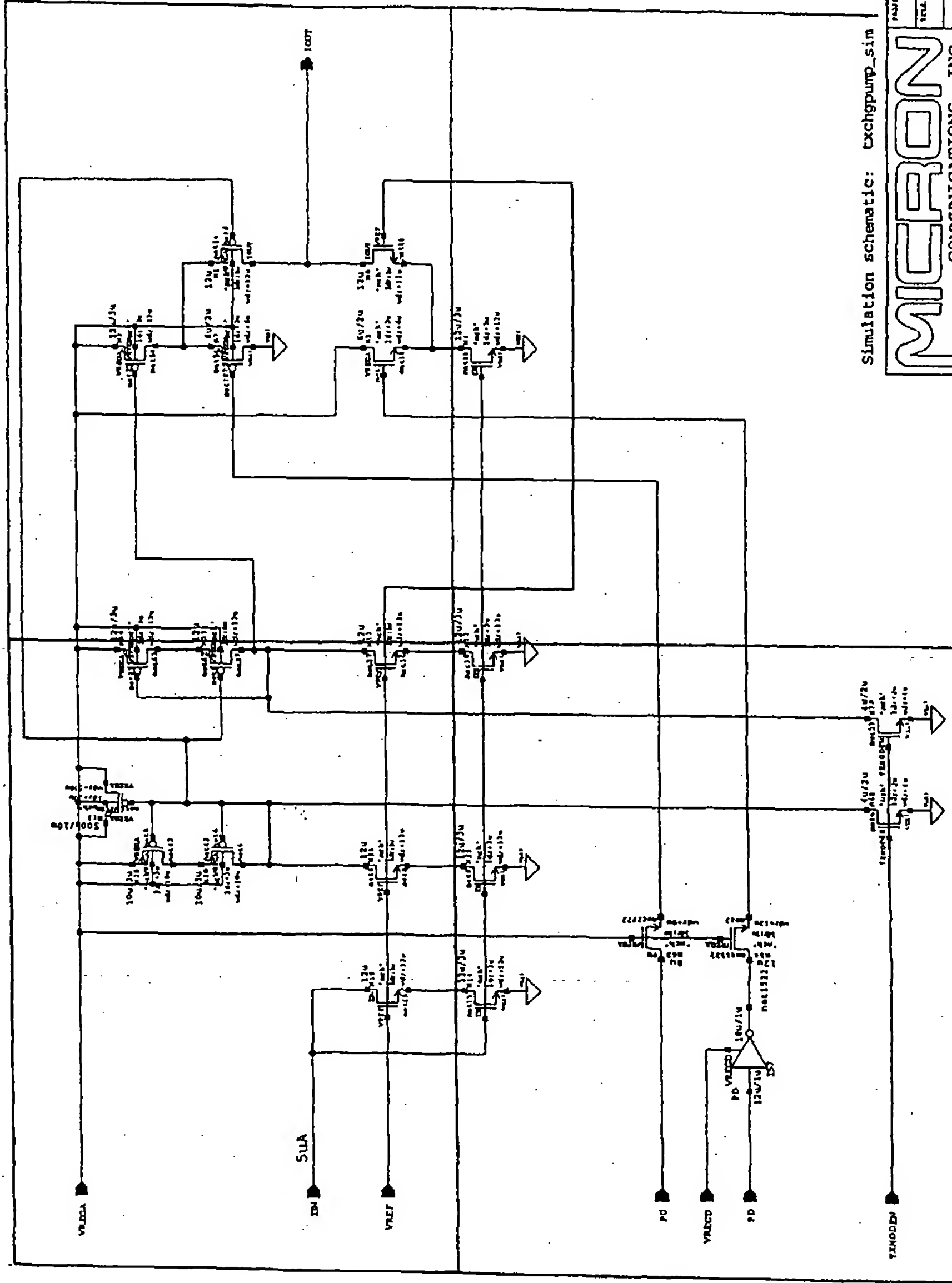


FIG. 8.060102

Simulation schematic: txchgump\_sim

<b>MICRON</b>		PROJECT: L03	DESIGNER: JOTOOLE
COMMUNICATIONS, INC.		FILE: TX PLL Charge Pump	
INTEGRATED CIRCUIT DESIGN		DATE: 103reva/txchgump	REV: B1
CONFIDENTIAL INFORMATION		DATE: Feb 28 09:55:50 1995	FILE: txll

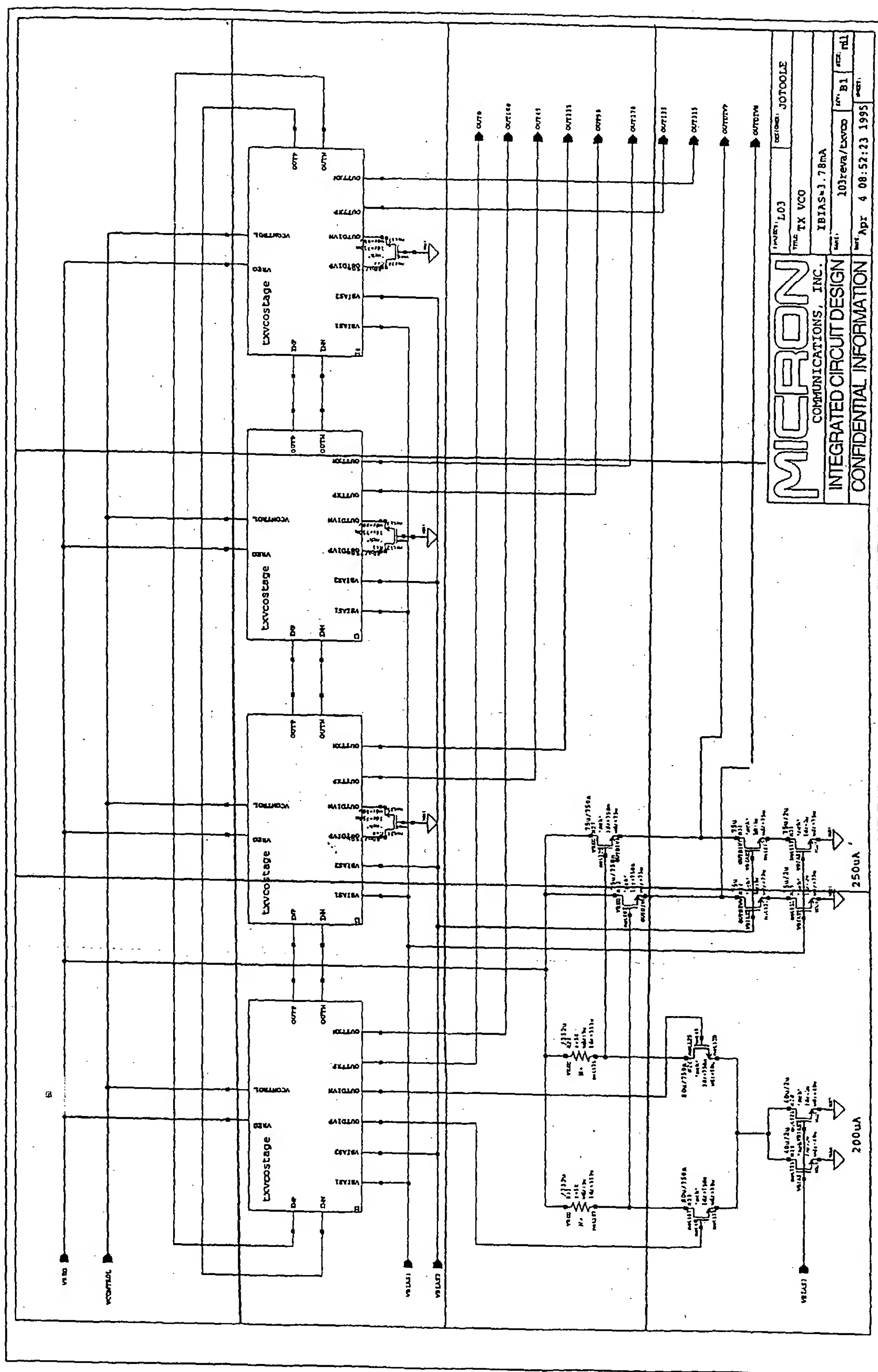
8.060103AA	8.060103AB
8.060103BA	8.060103BB
8.060103CA	8.060103CB

8.060103AA



8.060104AA	8.060104AB	8.060104AC
8.060104BA	8.060104BB	8.060104BC
8.060104CA	8.060104CB	8.060104CC
8.060104DA	8.060104DB	8.060104DC

SECRET



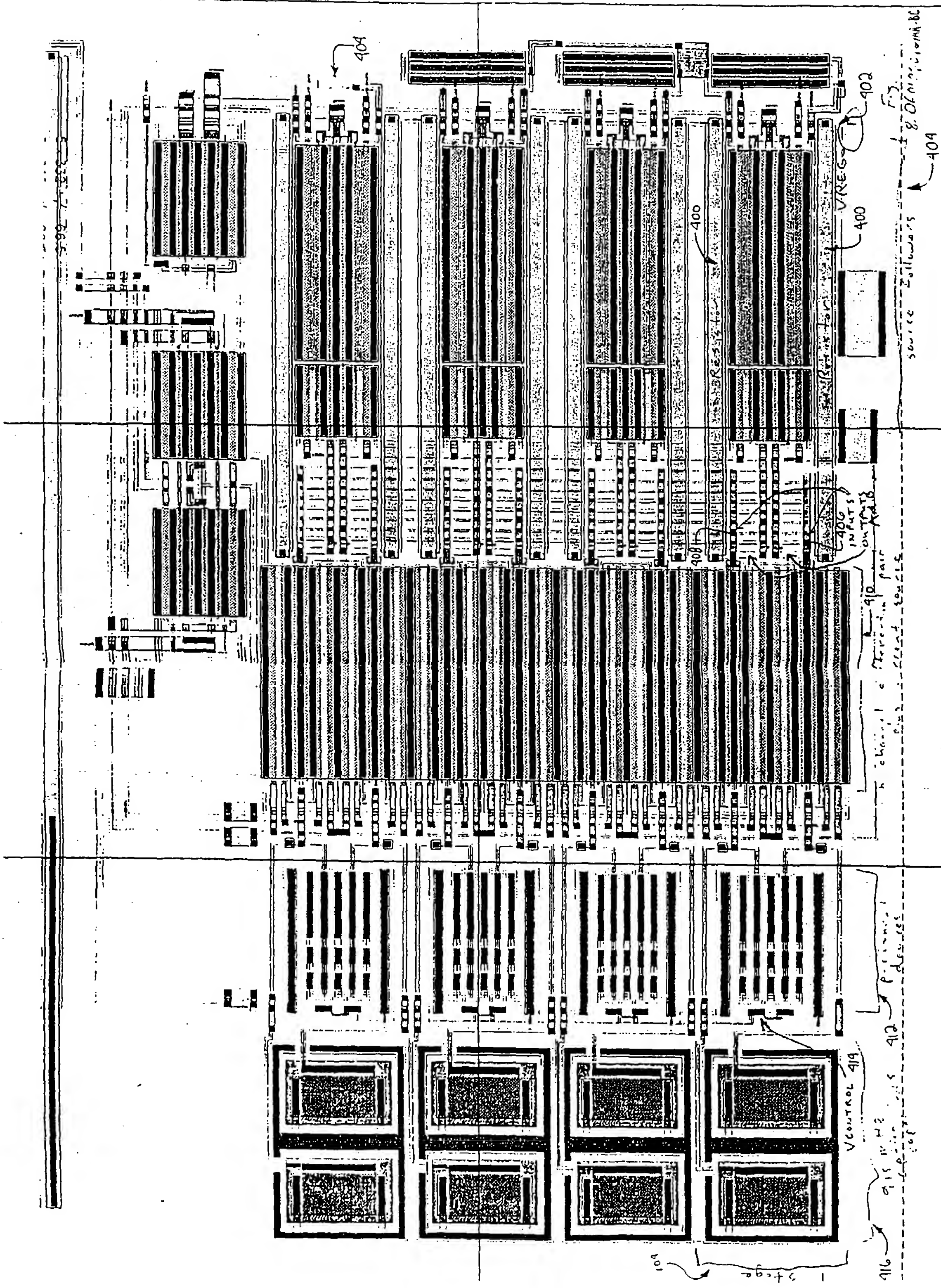
8.06010401AA	8.06010401AB	8.06010401AC	8.06010401AD
8.06010401BA	8.06010401BB	8.06010401BC	8.06010401BD

EX 8.06010401





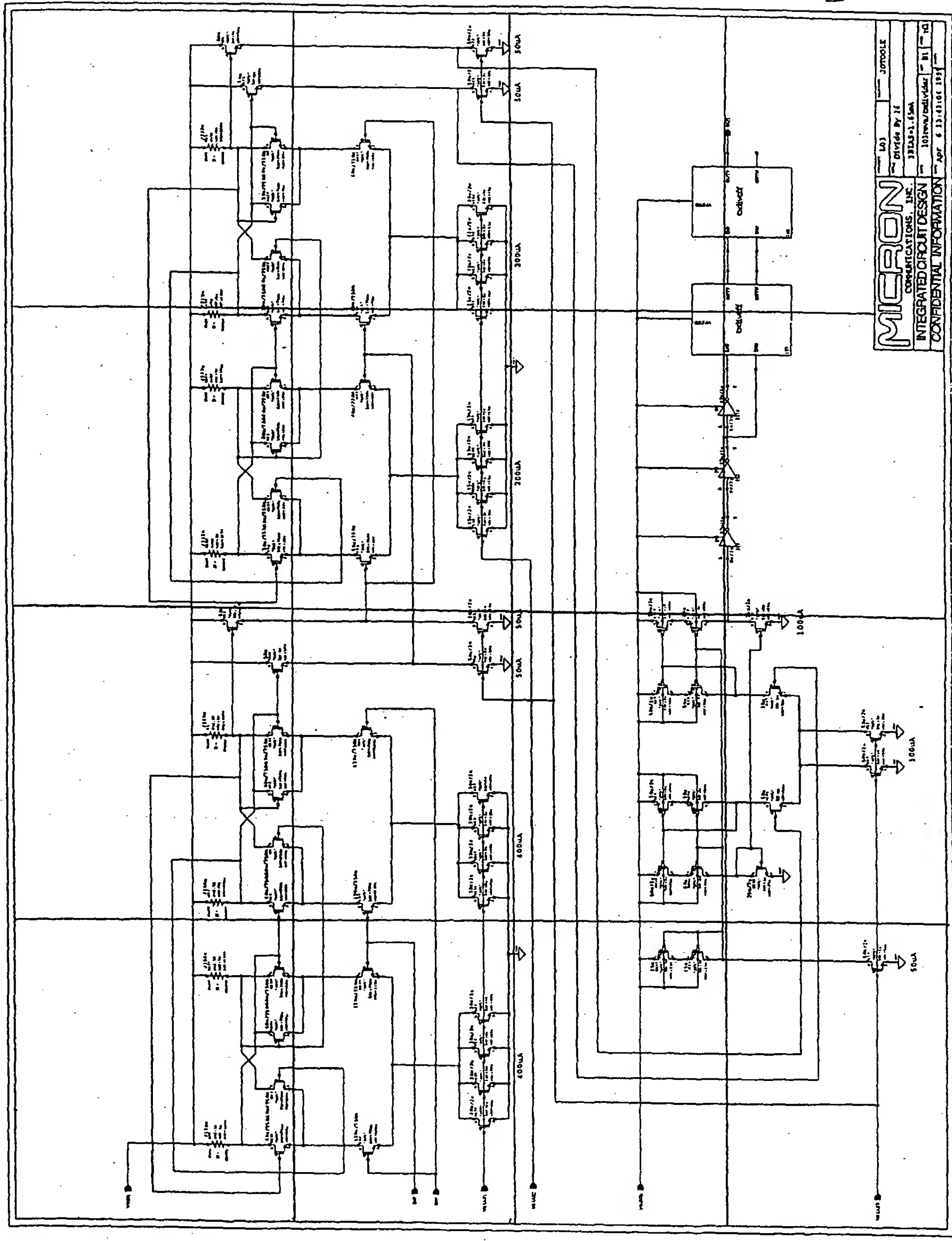




8.060105AA	8.060105AB	8.060105AC	8.060105AD
8.060105BA	8.060105BB	8.060105BC	8.060105BD
8.060105CA	8.060105CB	8.060105CC	8.060105CD
8.060105DA	8.060105DB	8.060105DC	8.060105DD

IL 11 05 88.060105

FIG. 8.060105 1



8.06010501AA	8.06010501AB
--------------	--------------

II II 8.06010501

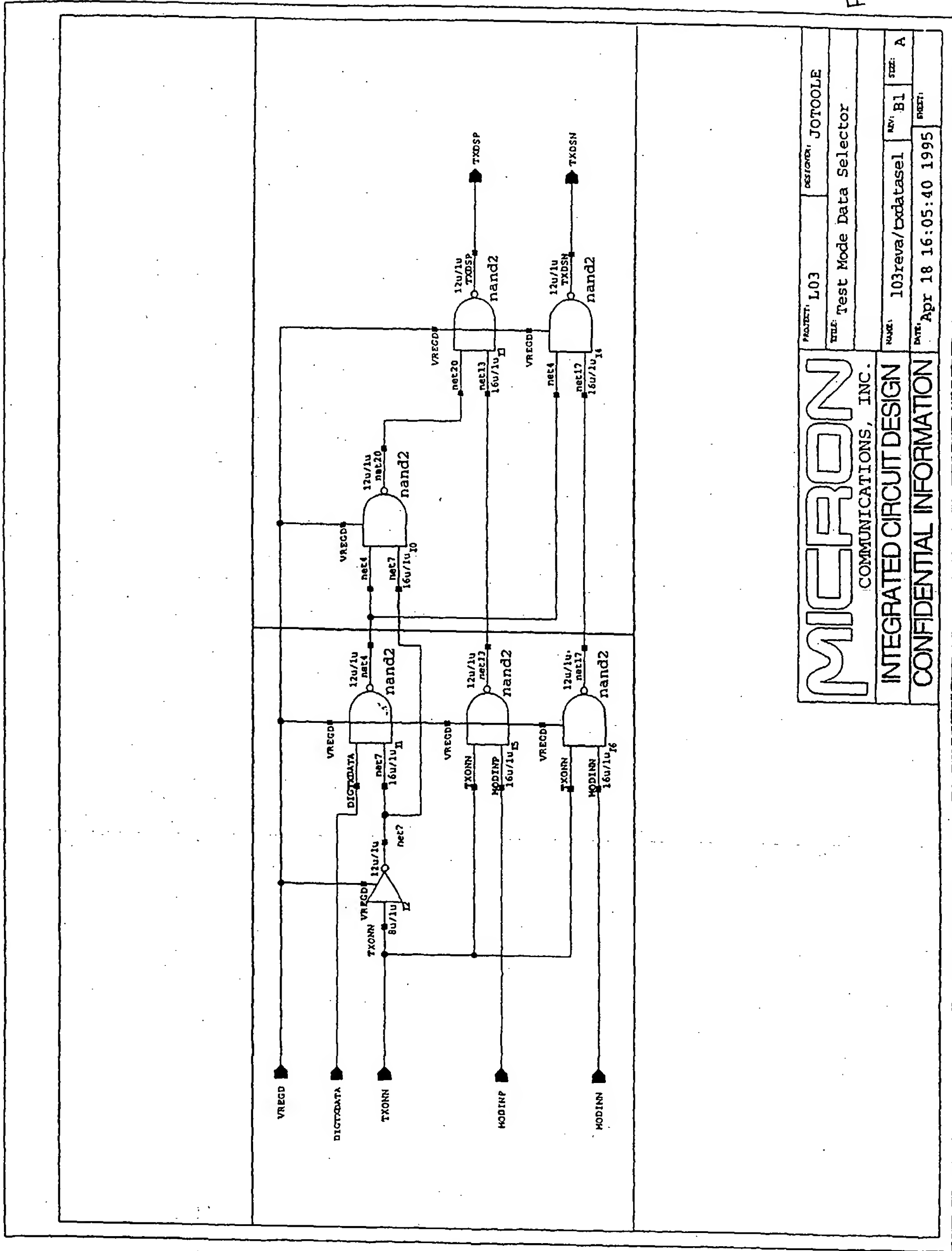


8.0602AA	8.0602AB
----------	----------

EX 88.0602



Fig. 8.0602



8.0603AA	8.0603AB
----------	----------

8.0603

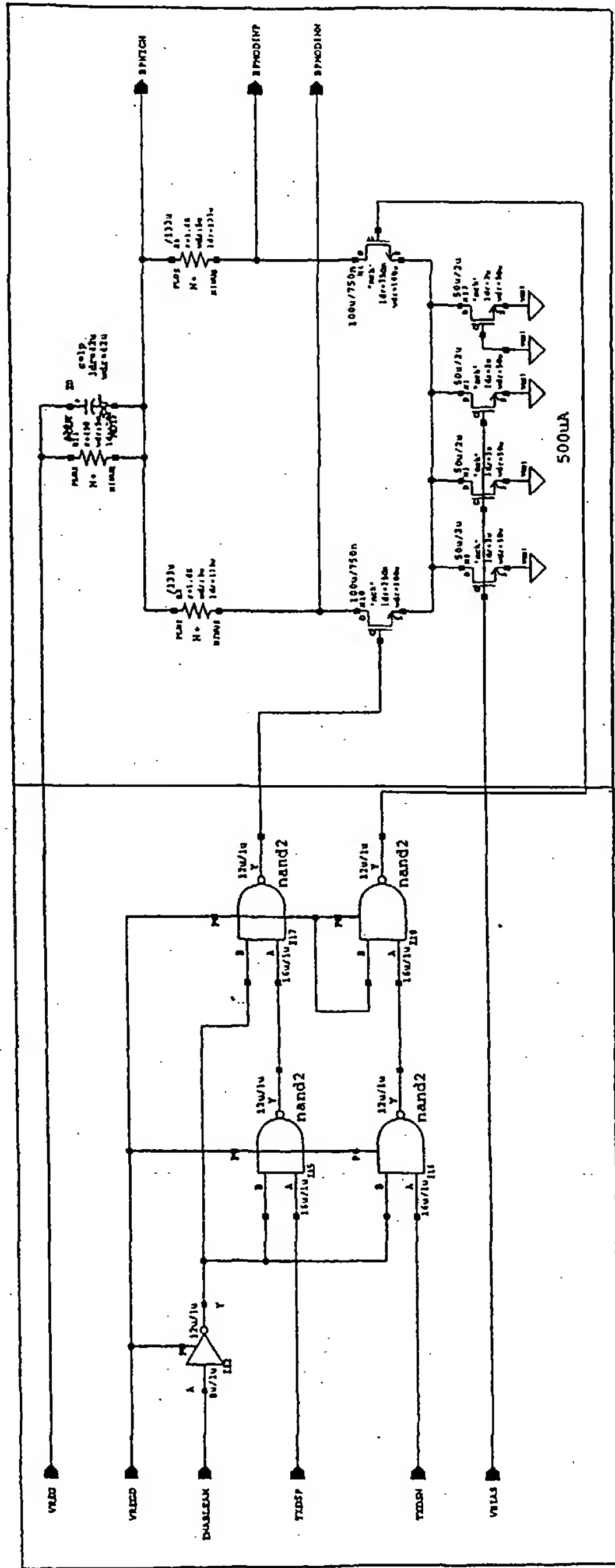


FIG. 8.0603

MICRON		DESIGNER	JOTOOLE
COMMUNICATIONS, INC.		DATE	103
INTEGRATED CIRCUIT DESIGN		TYPE	BPSK Modulation Driver
CONFIDENTIAL INFORMATION		IBIAS=500uA	
		103reva/txbpsk	B8
		DATE	Jan 18 10:28:46 1996

B8: modified current source

8.0604AB

8.0604AA

8.0604

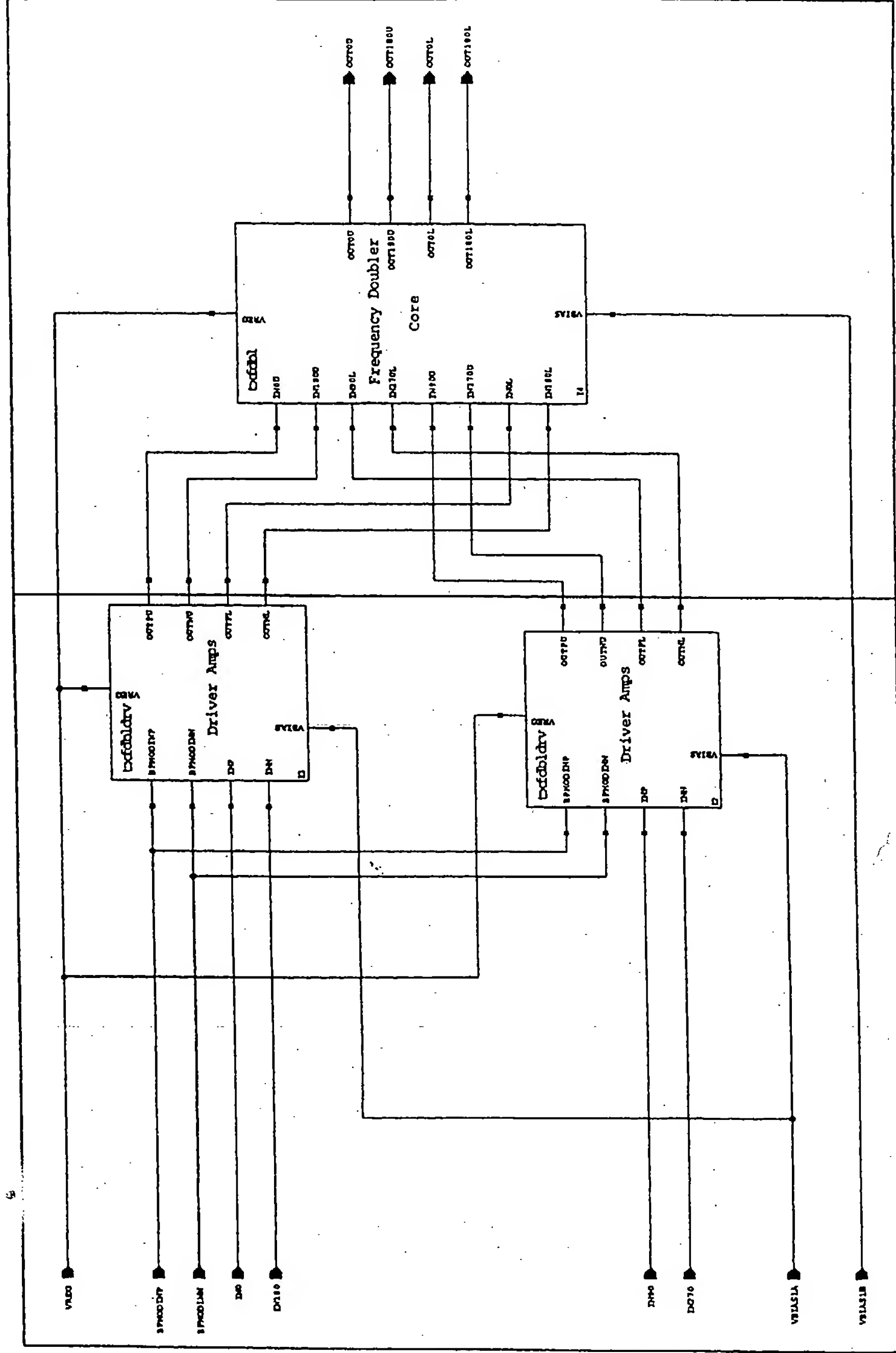
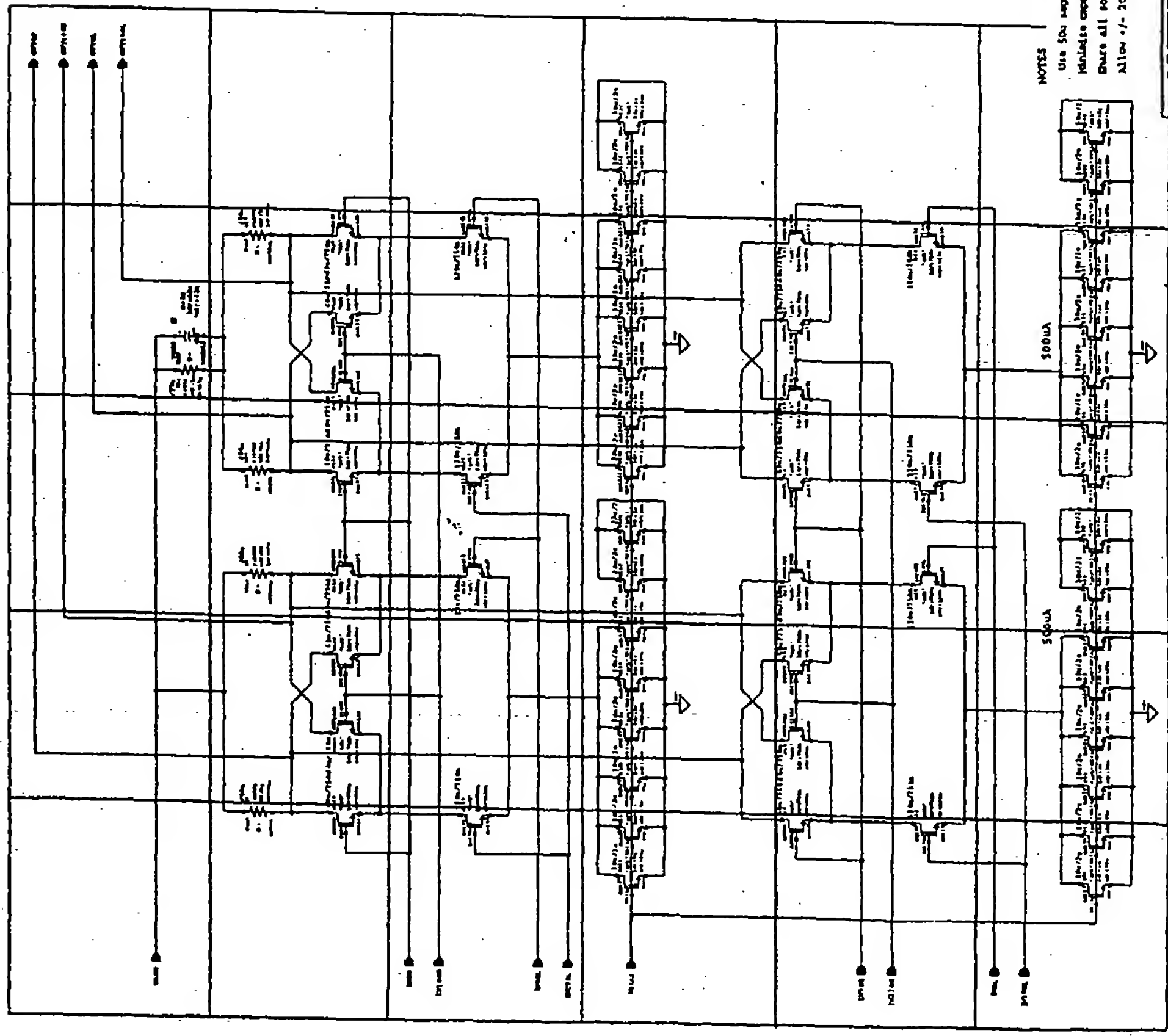


FIG. 8.0604

MICRON		PROJECT: L03	REVISION: J0700LE
COMMUNICATIONS, INC.		TITLE: Frequency Doubler	
INTEGRATED CIRCUIT DESIGN		IBIAS=4mA	
CONFIDENTIAL INFORMATION		DATE: 103rev/bdoubler	REV: B1
		DATE: Apr 5 10:17:13 1995	REV: 001

8.060401AA	8.060401AB	8.060401AC	8.060401AD	8.060401AE
8.060401BA	8.060401BB	8.060401BC	8.060401BD	8.060401BE
8.060401CA	8.060401CB	8.060401CC	8.060401CD	8.060401CE
8.060401DA	8.060401DB	8.060401DC	8.060401DD	8.060401DE
8.060401EA	8.060401EB	8.060401EC	8.060401ED	8.060401EE
8.060401FA	8.060401FB	8.060401FC	8.060401FD	8.060401FE

И.И.С. 8.06040100



NOTES  
 Use 50k segments for all devices.  
 Indicate capacitance on all nodes (unless have priority).  
 Show all source and drain nodes.  
 Allow +/- 20% adjustment on resistors at power supply end.

<b>MICRON</b>		103	207001E
COMMUNICATIONS, INC.		Frequency Doubler Core	
INTEGRATED CIRCUIT DESIGN		June 10, 1982 for 3.310KHz	
CONFIDENTIAL INFORMATION		10/20/82/0001	28
		Jan 12 15:55:25 1992	

M1, modified current sources

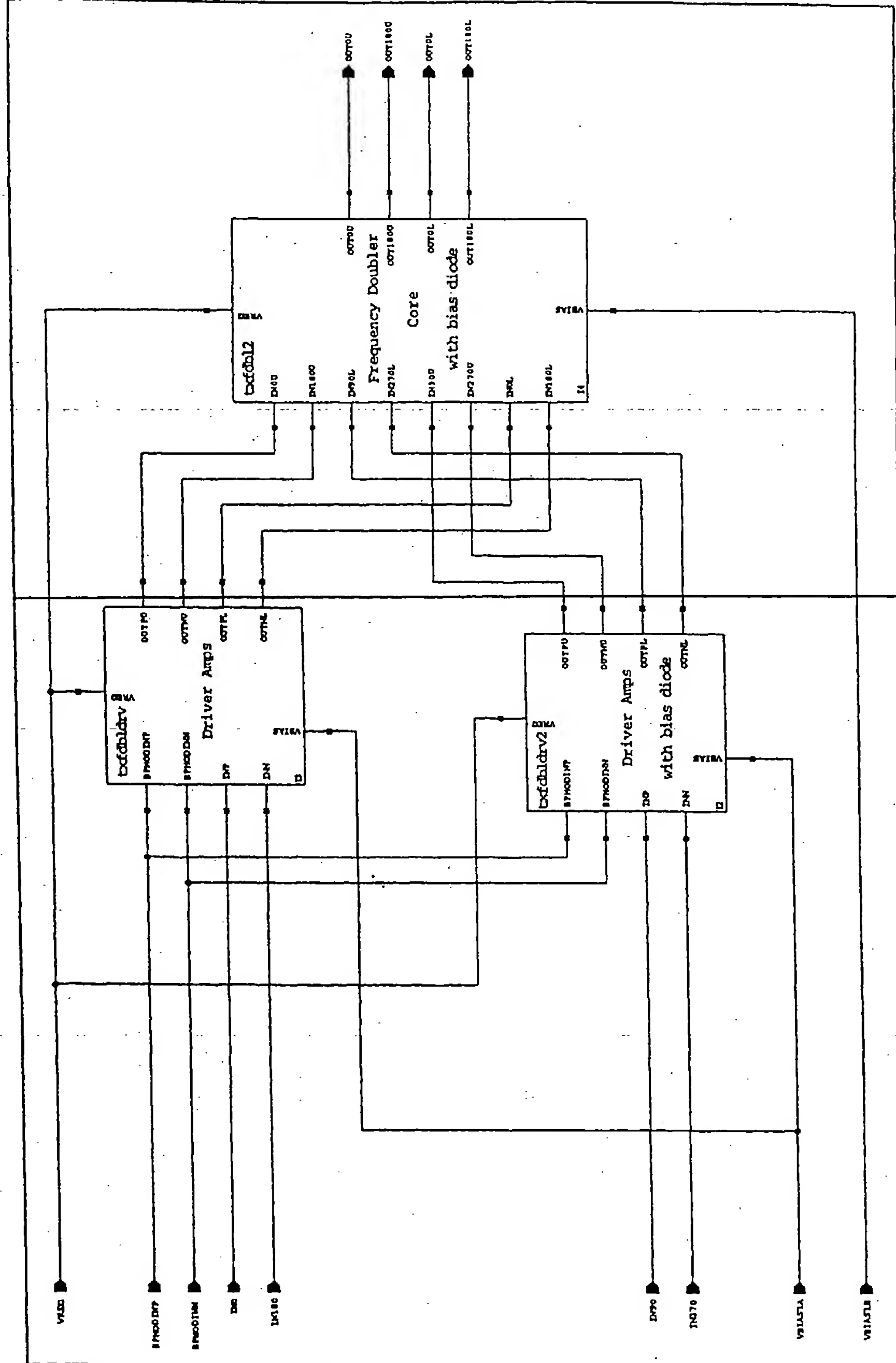
FIG. 8.060901

8.0605AB

8.0605AA

EX 88.00605





# Zoom

COMMUNICATIONS, INC.

# INTEGRATED CIRCUIT DESIGN

**CONFIDENTIAL INFORMATION**

PROJECT: 1.03	DELIVERABLE:	TOTAL: 310000
---------------	--------------	---------------

**TOTAL**  
**178,217.00**

**Frequency Doubler**

BIAS=4mA

103reva/bdoubler2

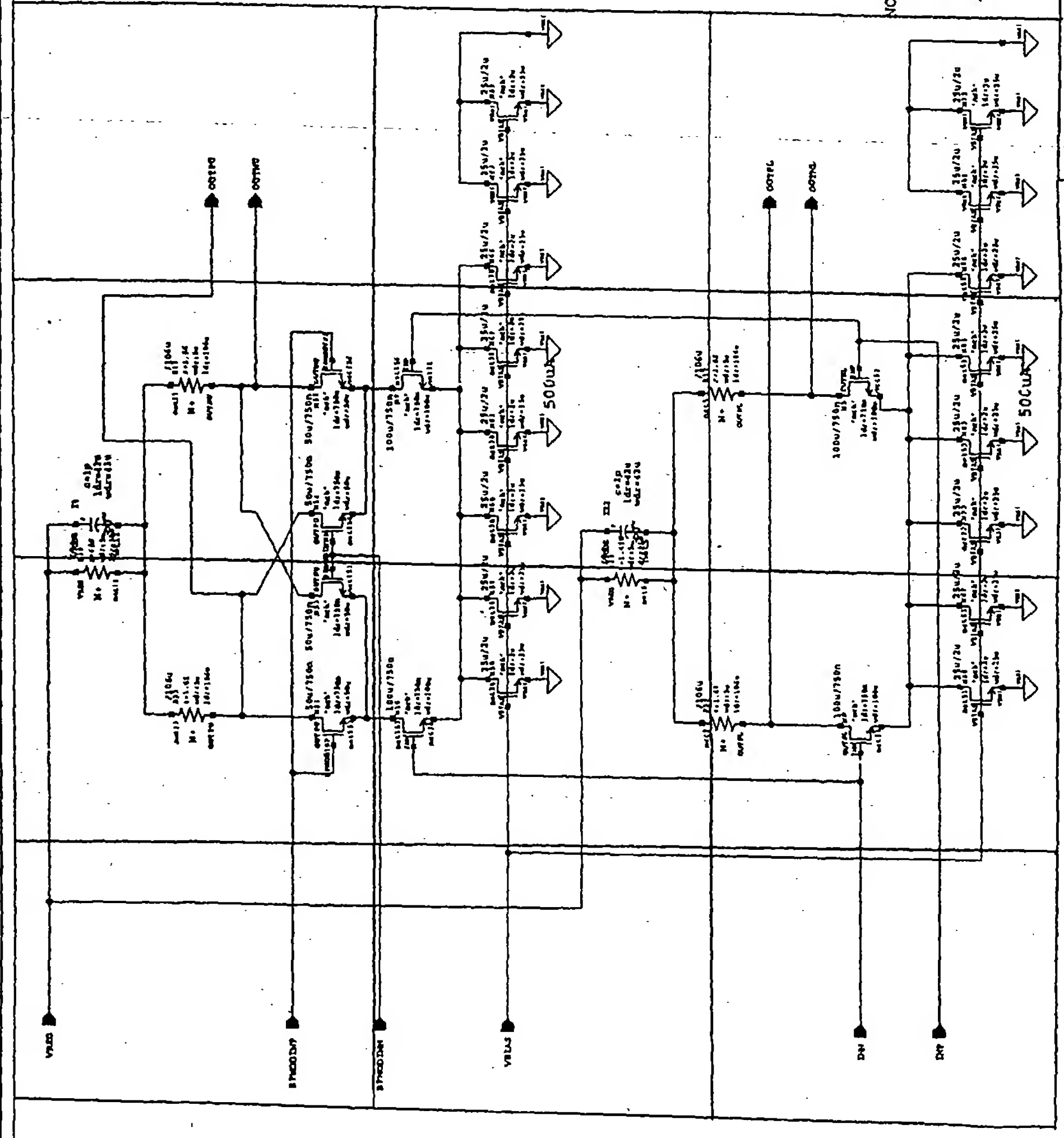
Jan 12 17:22:51 195

100-443887-100

**B8: current sources modified**

8.060501AA	8.060501AB	8.060501AC	8.060501AD
8.060501BA	8.060501BB	8.060501BC	8.060501BD
8.060501CA	8.060501CB	8.060501CC	8.060501CD

II II II 8.060501 II



NOTES  
Minimize capacitance on output nodes.  
Share all source/drain nodes.  
Allow +/- 20% adjustment on resistors  
at supply end.

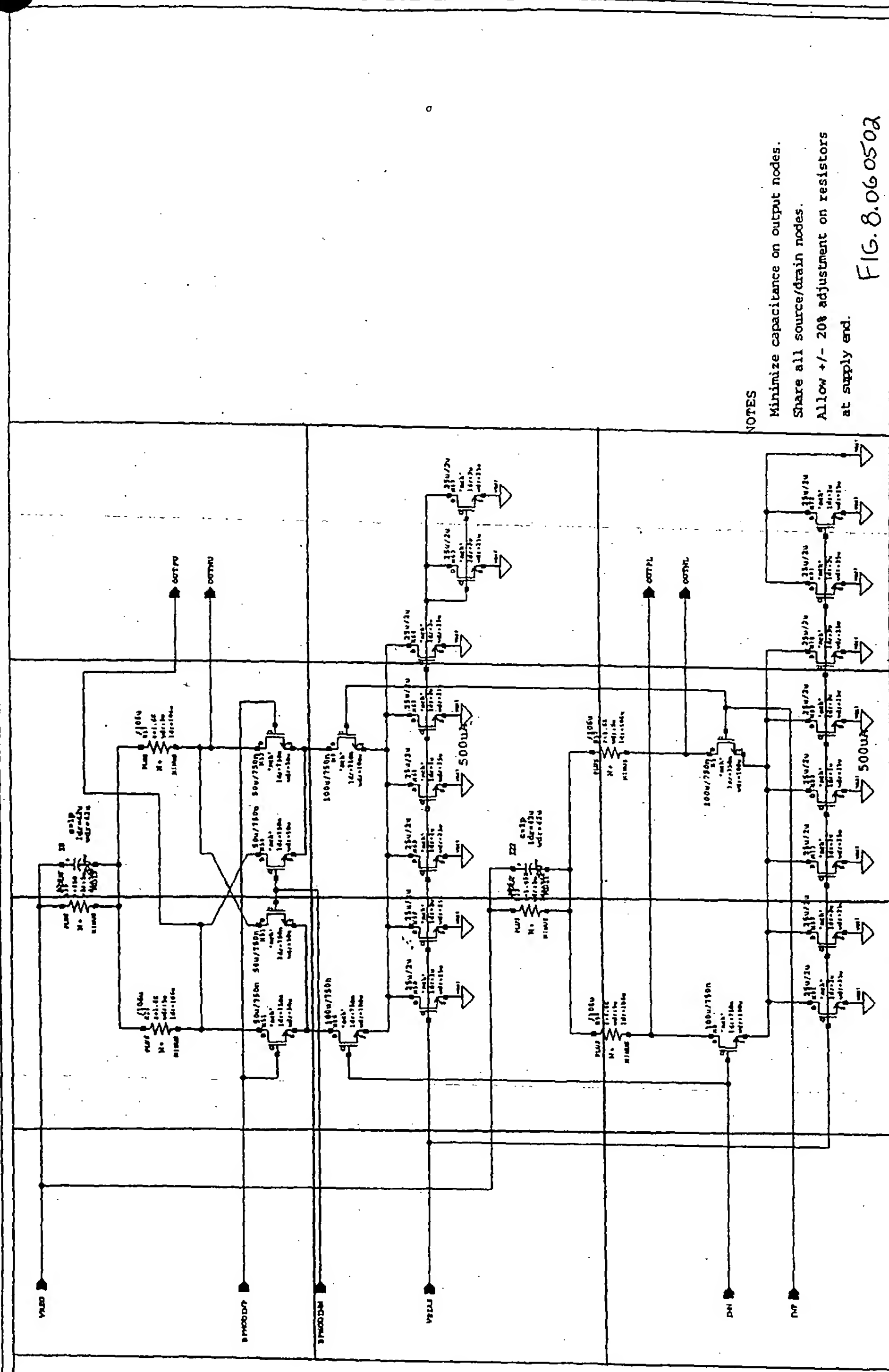
FIG. 8.060501

MICRON		PROJECT	L03	REVISION	J0700LE
COMMUNICATIONS, INC.		TYPE	Driver Amps		
INTEGRATED CIRCUIT DESIGN		IBIAS	1mA		
CONFIDENTIAL INFORMATION		DATE	10/19/96	BY	B8
		DATE	Jan 12 15:37:26 1996	BY	ml

B8: modified current sources

8.060502AA	8.060502AB	8.060502AC	8.060502AD
8.060502BA	8.060502BB	8.060502BC	8.060502BD
8.060502CA	8.060502CB	8.060502CC	8.060502CD

Итого 8.060502



NOTES  
Minimize capacitance on output nodes.  
Share all source/drain nodes.  
Allow +/- 20% adjustment on resistors  
at supply end.

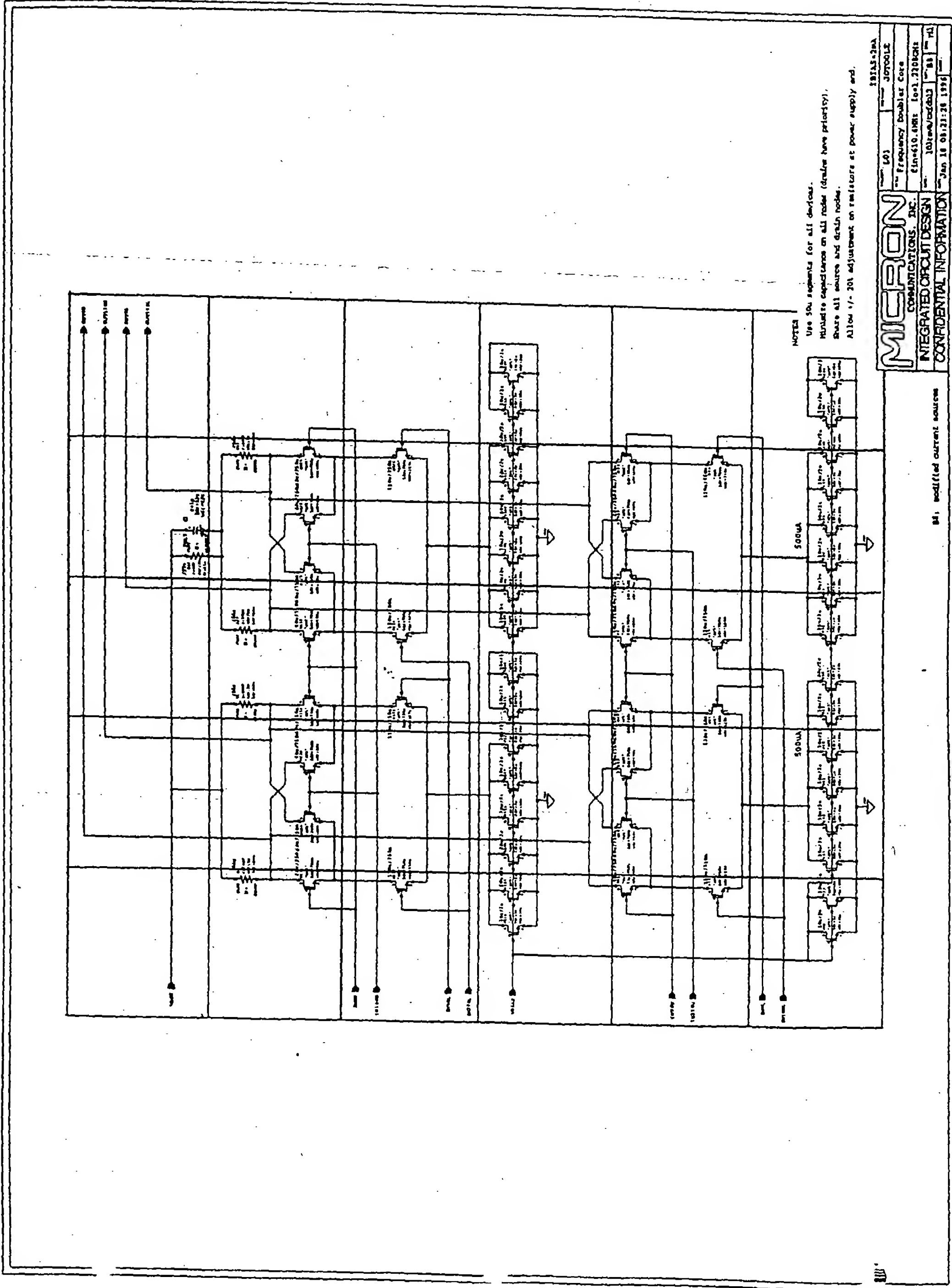
FIG. 8.060502

MICRON		PRODUCT: L03	PROJECT: J0700LE
COMMUNICATIONS, INC.		TYPE: Doubler Driver Amps	
INTEGRATED CIRCUIT DESIGN		IBIAS=1mA	
CONFIDENTIAL INFORMATION		DATE: 103revA/Exfabldrv2	REV: B8
		DATE: Jan 18 08:22:12 1996	FILE: ml

B8: modified current sources

8.060503AA	8.060503AB	8.060503AC	8.060503AD	8.060503AE
8.060503BA	8.060503BB	8.060503BC	8.060503BD	8.060503BE
8.060503CA	8.060503CB	8.060503CC	8.060503CD	8.060503CE
8.060503DA	8.060503DB	8.060503DC	8.060503DD	8.060503DE
8.060503EA	8.060503EB	8.060503EC	8.060503ED	8.060503EE
8.060503FA	8.060503FB	8.060503FC	8.060503FD	8.060503FE

8.060503



NOTES

- Use 50k ohms for all devices.
- Minimize capacitance on all nodes (drives have priority).
- Share all source and drain nodes.
- Allow +/- 20% adjustment on transistors at power supply end.

MICRON		30700L2
COMMUNICATIONS	30700L2	Frequency Doubler Core
INTEGRATED CIRCUIT DESIGN	41m410.48MT	101.270000
CONFIDENTIAL INFORMATION	101m410.48MT	101.270000
	Jan 18 08:21:28 1995	

81, modified current source

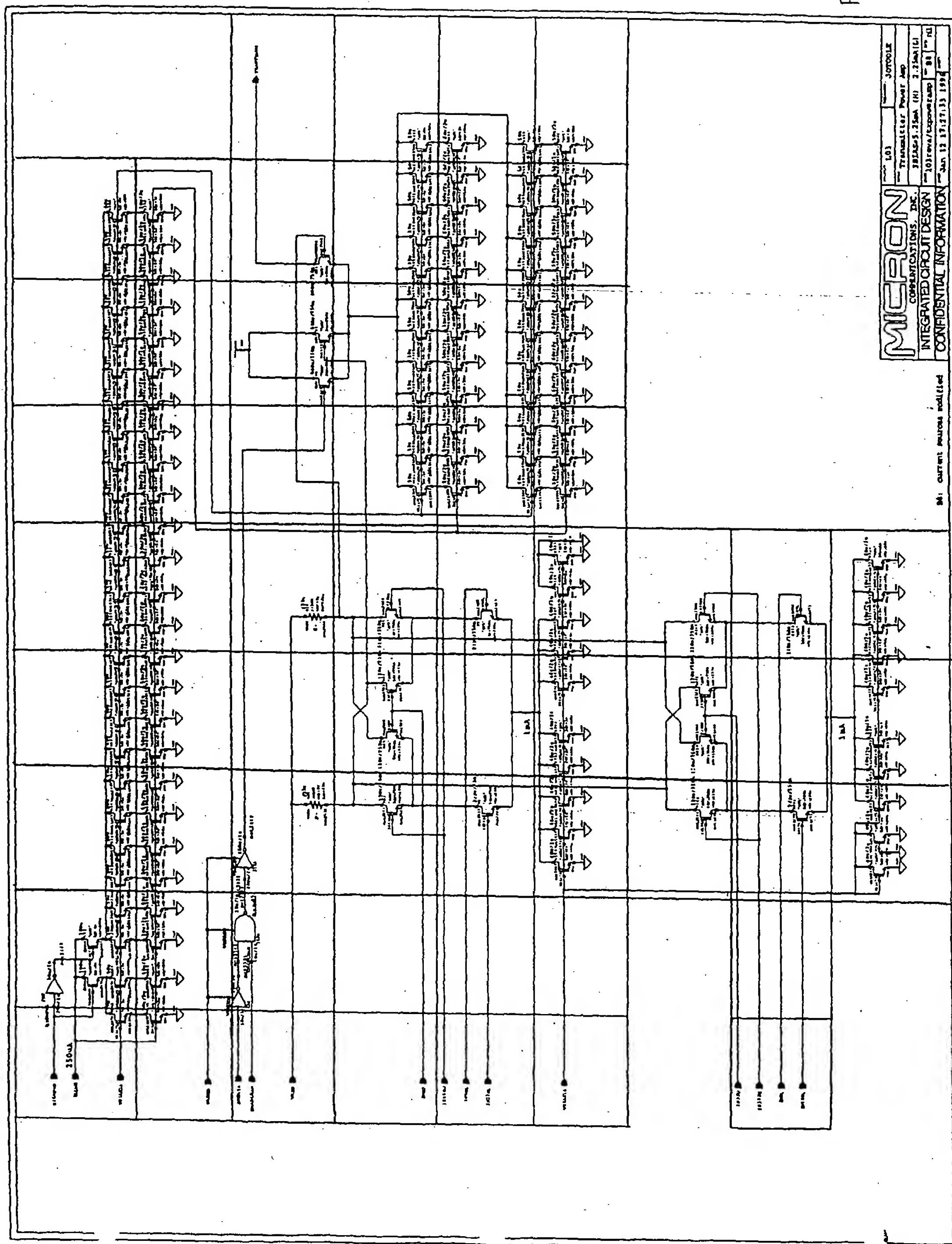
FIG. 8.060503

8.0606AA	8.0606AB	8.0606AC	8.0606AD	8.0606AE	8.0606AF	8.0606AG	8.0606AH
8.0606BA	8.0606BB	8.0606BC	8.0606BD	8.0606BE	8.0606BF	8.0606BG	8.0606BH
8.0606CA	8.0606CB	8.0606CC	8.0606CD	8.0606CE	8.0606CF	8.0606CG	8.0606CH
8.0606DA	8.0606DB	8.0606DC	8.0606DD	8.0606DE	8.0606DF	8.0606DG	8.0606DH
8.0606EA	8.0606EB	8.0606EC	8.0606ED	8.0606EE	8.0606EF	8.0606EG	8.0606EH
8.0606FA	8.0606FB	8.0606FC	8.0606FD	8.0606FE	8.0606FF	8.0606FG	8.0606FH
8.0606HA	8.0606HB	8.0606HC	8.0606HD	8.0606HE			
		8.0606IB	8.0606IC	8.0606ID	8.0606IE		

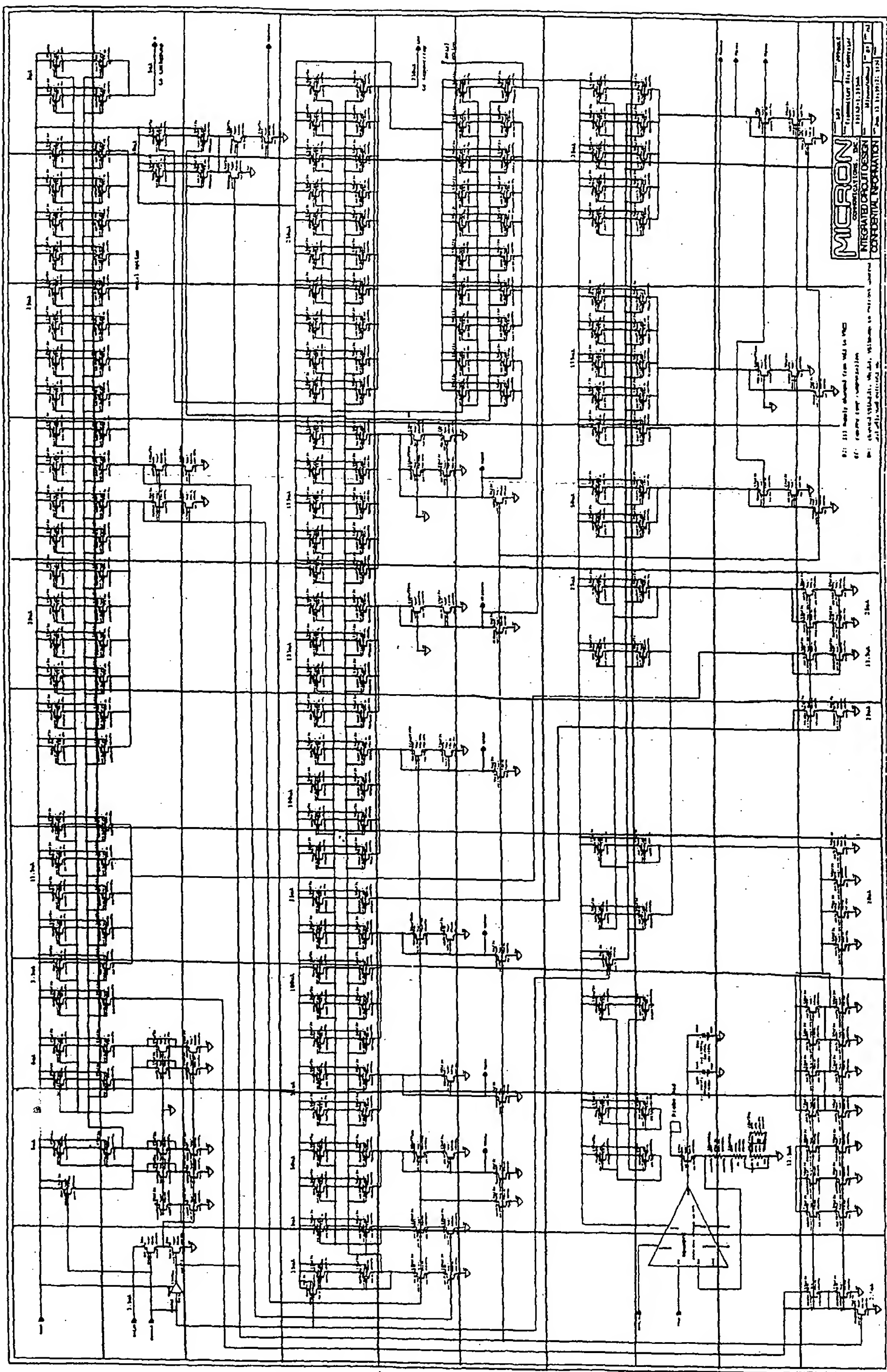
И.П.С. Б.М.Б.М.Б.



FIG. 8.0606







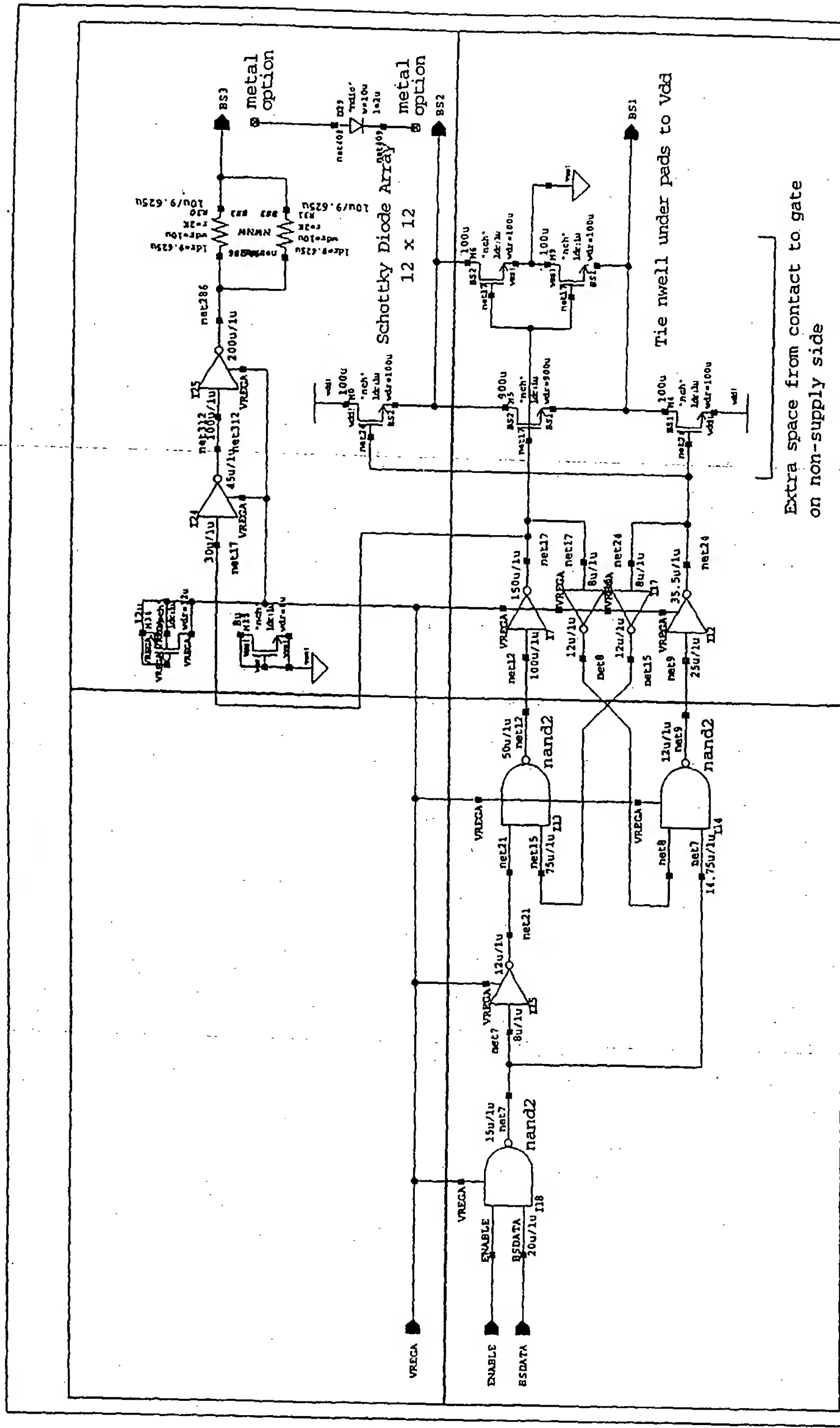
8.0608AB

8.0608BB

8.0608AA

8.0608BA

BB. 0606 II



**MICRON**  
COMMUNICATIONS, INC.

INTEGRATED CIRCUIT DESIGN

CONFIDENTIAL INFORMATION

PROJECT: L03 DESTROY: JOTOOLE

Modulated Backscatter

Transmitter

NAME: 103reva/tombs A2: B10 SIZE: A

DATE: Mar 26 11:07:42 1996 SHEET: 1

Fig. 8.0608

8.07AB	8.07BB
8.07AA	8.07BA

II II III III

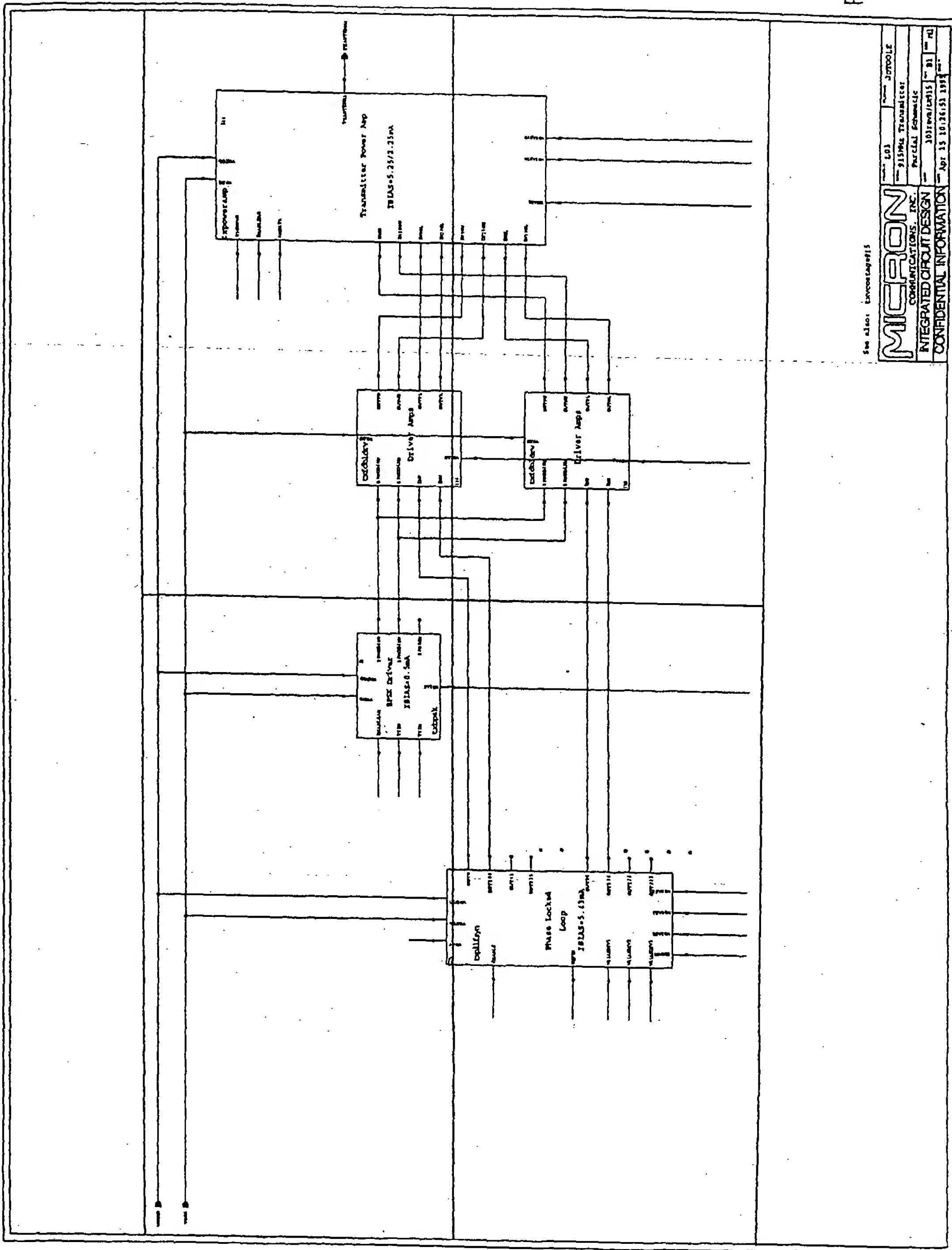


FIG. 8.07

See also: Unconstrained

**MICRON**

COMMUNICATIONS, INC.  
INTEGRATED CIRCUIT DESIGN

CONFIDENTIAL INFORMATION

Part: 1812AS-5.13MA  
Rev: 1.0  
Date: Apr 15 10:26:53 1994

8.0701AA	8.0701AB
8.0701BA	8.0701BB
8.0701CA	8.0701CB

II II III III III III

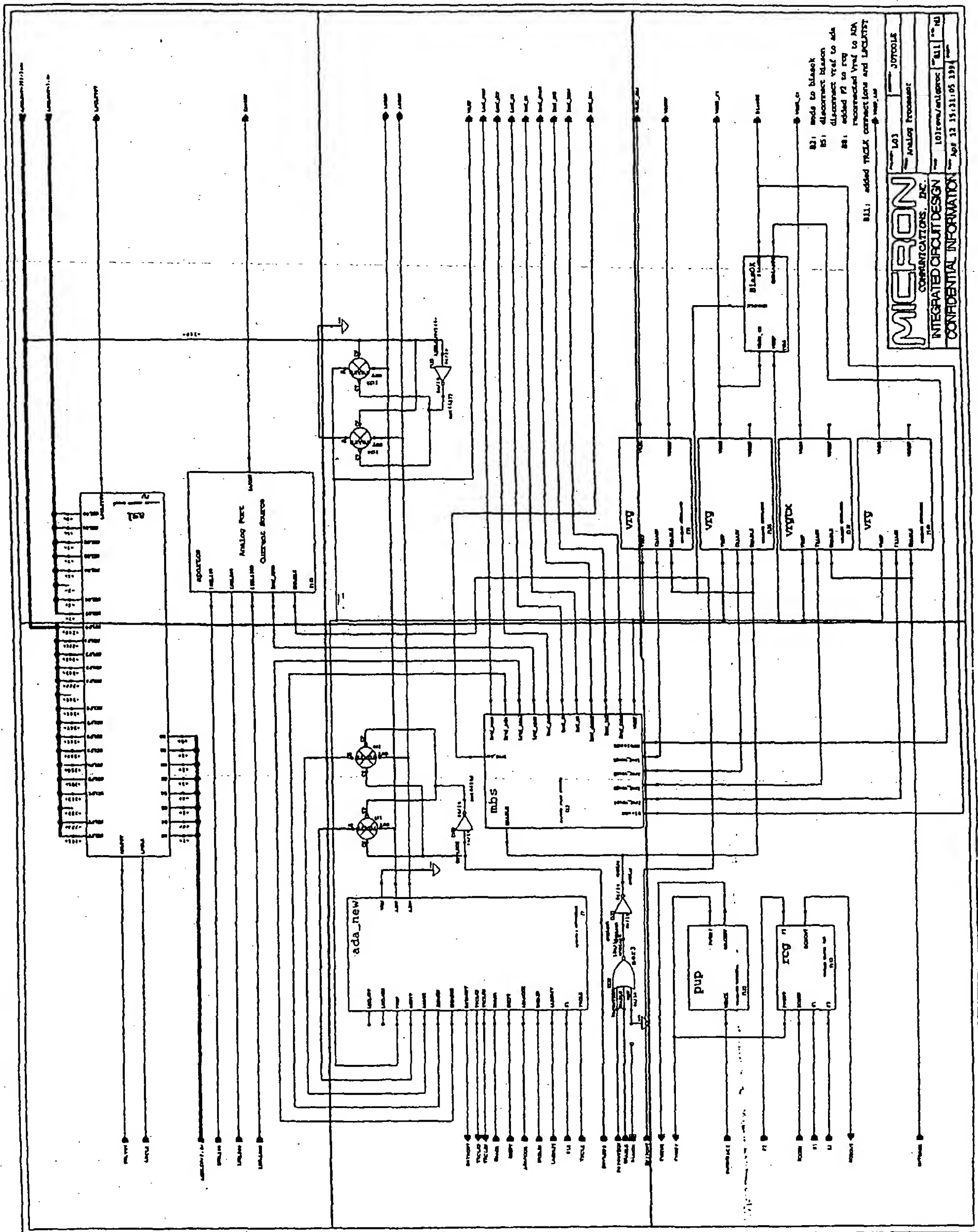




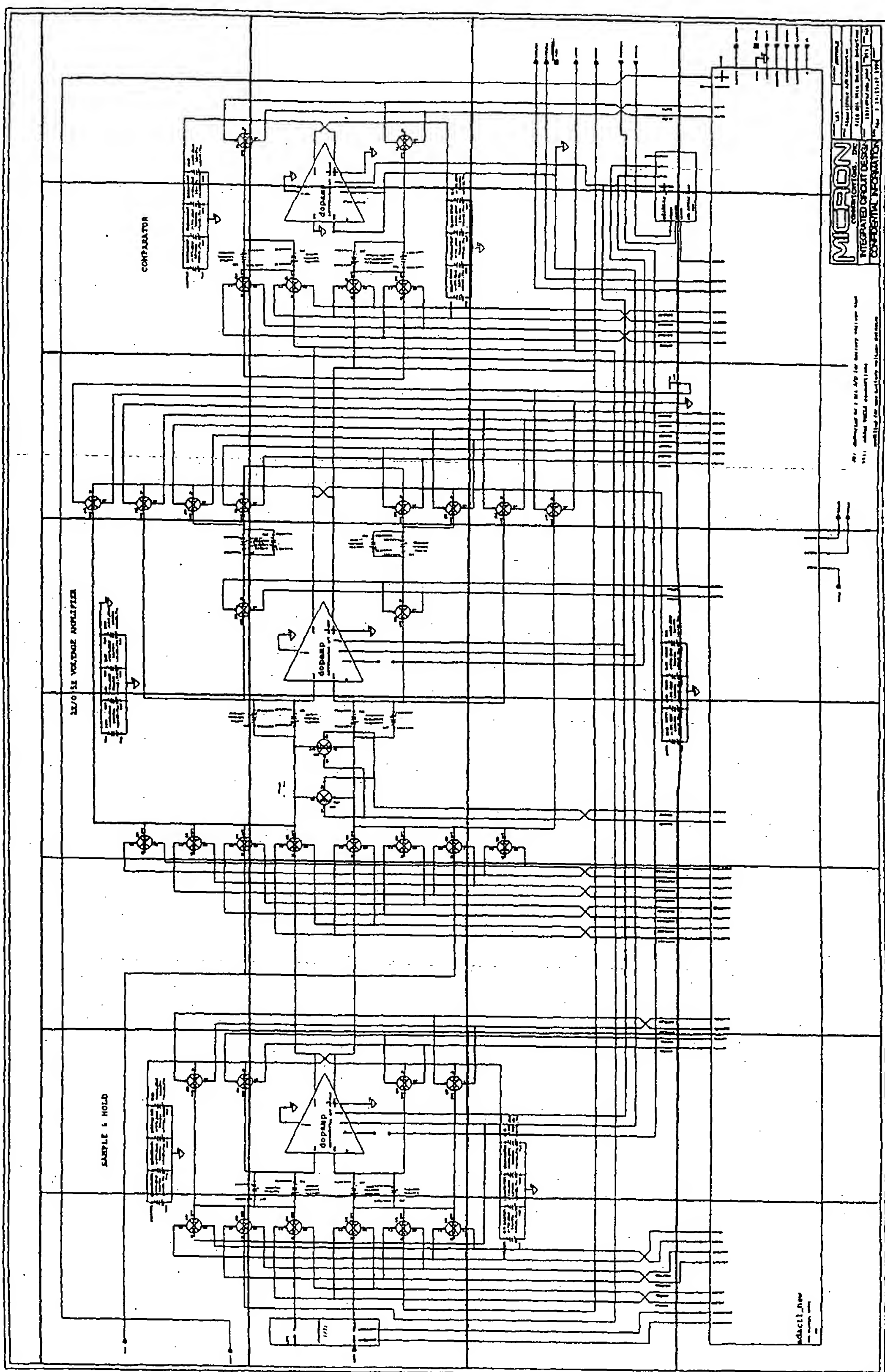
9AA	9AB
9BA	9BB
9CA	9CB

SECRET

Fig. 9



9.01AA	9.01AB	9.01AC	9.01AD	9.01AE	9.01AF	9.01AG	9.01AH
9.01BA	9.01BB	9.01BC	9.01BD	9.01BE	9.01BF	9.01BG	9.01BH
9.01CA	9.01CB	9.01CC	9.01CD	9.01CE	9.01CF	9.01CG	9.01CH
9.01DA	9.01DB	9.01DC	9.01DD	9.01DE	9.01DF	9.01DG	9.01DH



516,901

9.0101AA	9.0101AB	9.0101AC	9.0101AD	9.0101AE	9.0101AF	9.0101AG	9.0101AH	9.0101AI	9.0101AJ	9.0101AK
9.0101BA	9.0101BB	9.0101BC	9.0101BD	9.0101BE	9.0101BF	9.0101BG	9.0101BH	9.0101BI	9.0101BJ	9.0101BK
9.0101CA	9.0101CB	9.0101CC	9.0101CD	9.0101CE	9.0101CF	9.0101CG	9.0101CH	9.0101CI	9.0101CJ	9.0101CK

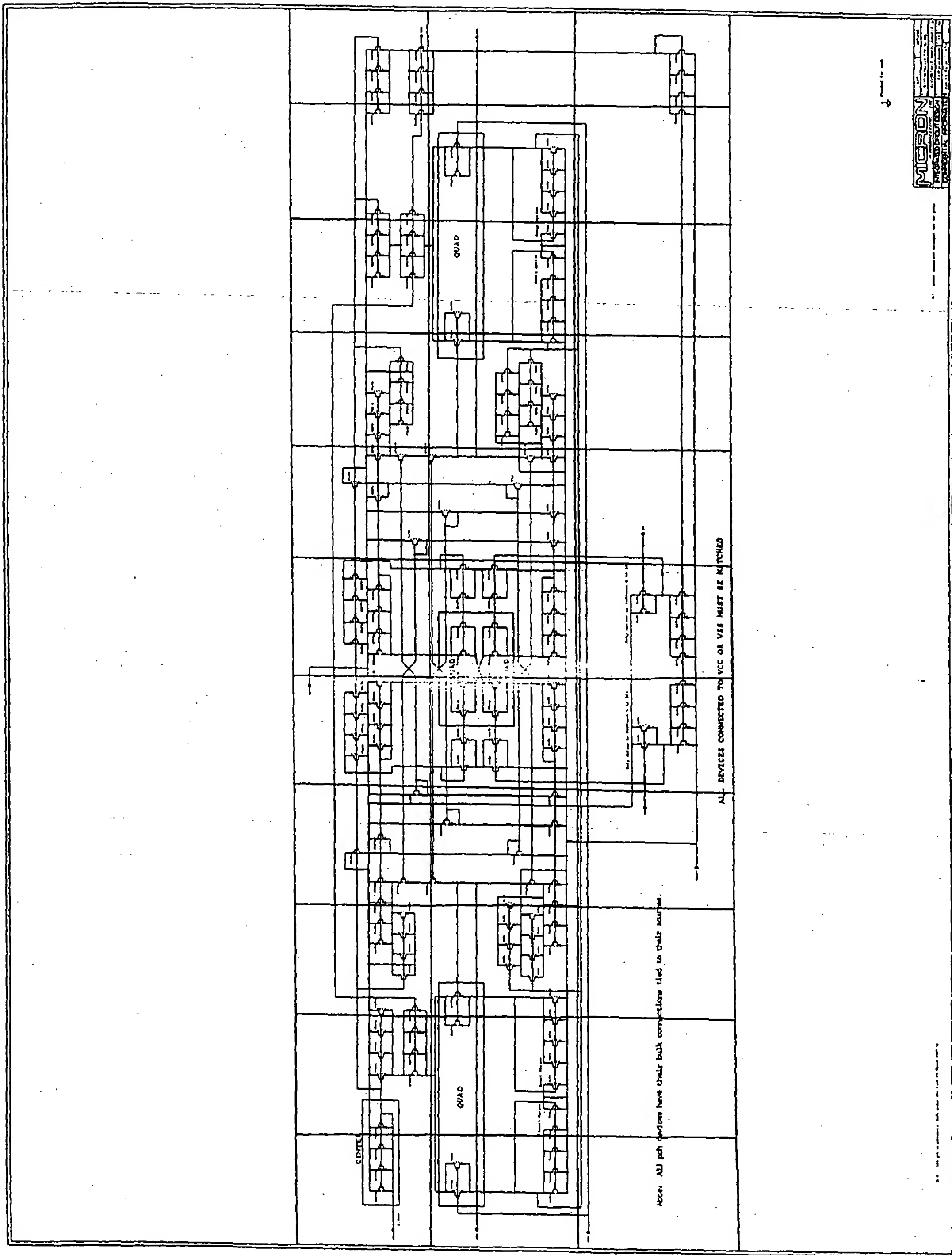


FIG. 9.0101



TIME, Analog Divide by 2

DATE May 19 16:34:53 1995

COMMUNICATIONS, INC.

# INTEGRATED CIRCUIT DESIGN

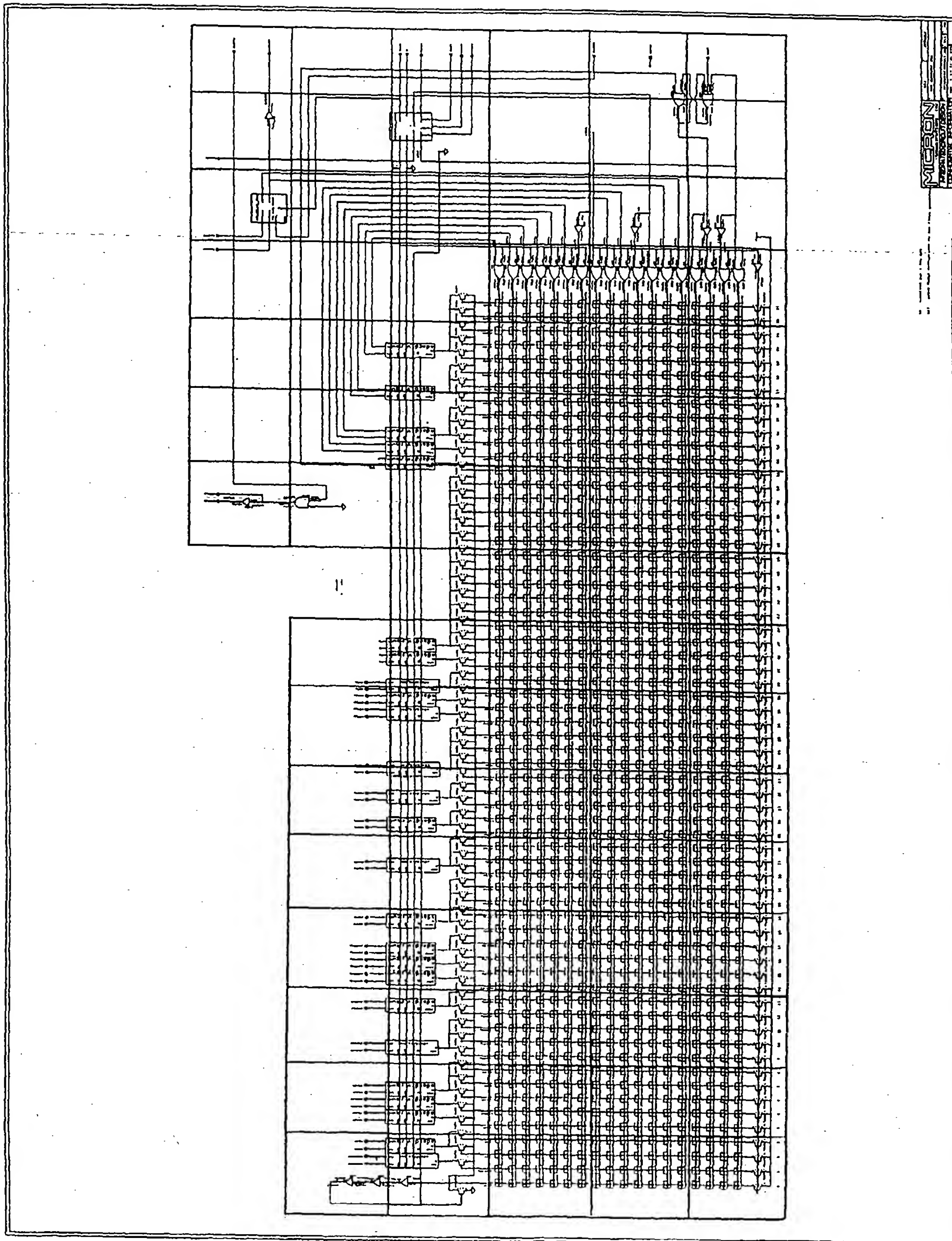
**CONFIDENTIAL INFORMATION**

Fig. 9.0102



9.0103BA	9.0103BB	9.0103BC	9.0103BD	9.0103BE	9.0103BF	9.0103BG	9.0103BH		9.0103AJ	9.0103AK	9.0103AL	9.0103AM	9.0103AN	9.0103AO	9.0103AP
9.0103CA	9.0103CB	9.0103CC	9.0103CD	9.0103CE	9.0103CF	9.0103CG	9.0103CH		9.0103BJ	9.0103BK	9.0103BL	9.0103BM	9.0103BN	9.0103BO	9.0103BP
9.0103DA	9.0103DB	9.0103DC	9.0103DD	9.0103DE	9.0103DF	9.0103DG	9.0103DH	9.0103CI	9.0103CJ	9.0103CK	9.0103CL	9.0103CM	9.0103CN	9.0103CO	9.0103CP
9.0103EA	9.0103EB	9.0103EC	9.0103ED	9.0103EE	9.0103EF	9.0103EG	9.0103EH	9.0103EI	9.0103EJ	9.0103EK	9.0103EL	9.0103EM	9.0103EN	9.0103EO	9.0103EP
9.0103FA	9.0103FB	9.0103FC	9.0103FD	9.0103FE	9.0103FF	9.0103FG	9.0103FH	9.0103FI	9.0103FJ	9.0103FK	9.0103FL	9.0103FM	9.0103FN	9.0103FO	9.0103FP

MI 40-030

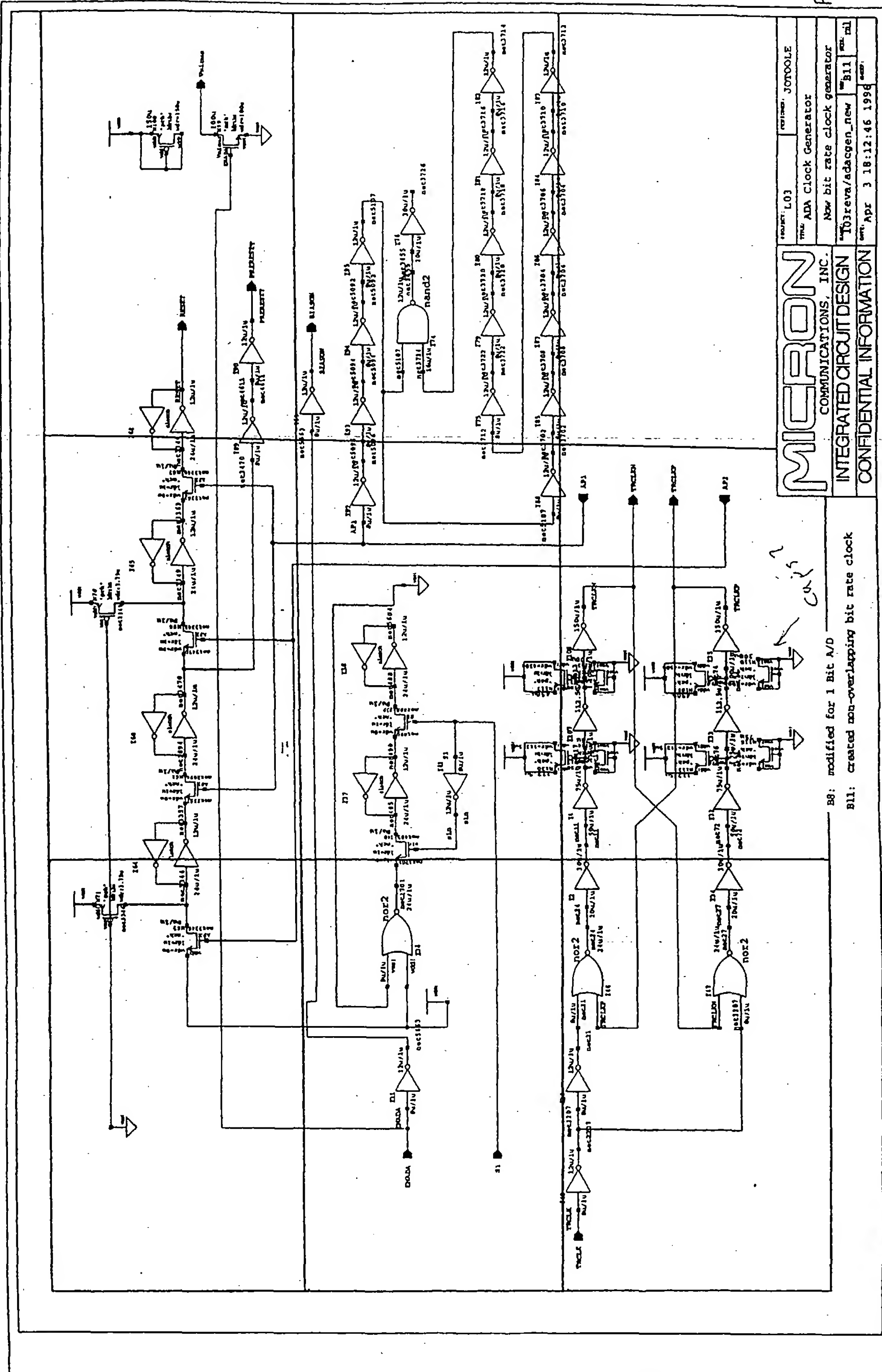


MICRON  
TECHNOLOGY CORPORATION  
1800 N. MILPITAS AVENUE  
SANTA CLARA, CALIF. 95050

FIG. 9.0103

9.010301AA	9.010301AB	9.010301AC
9.010301BA	9.010301BB	9.010301BC
9.010301CA	9.010301CB	9.010301CC

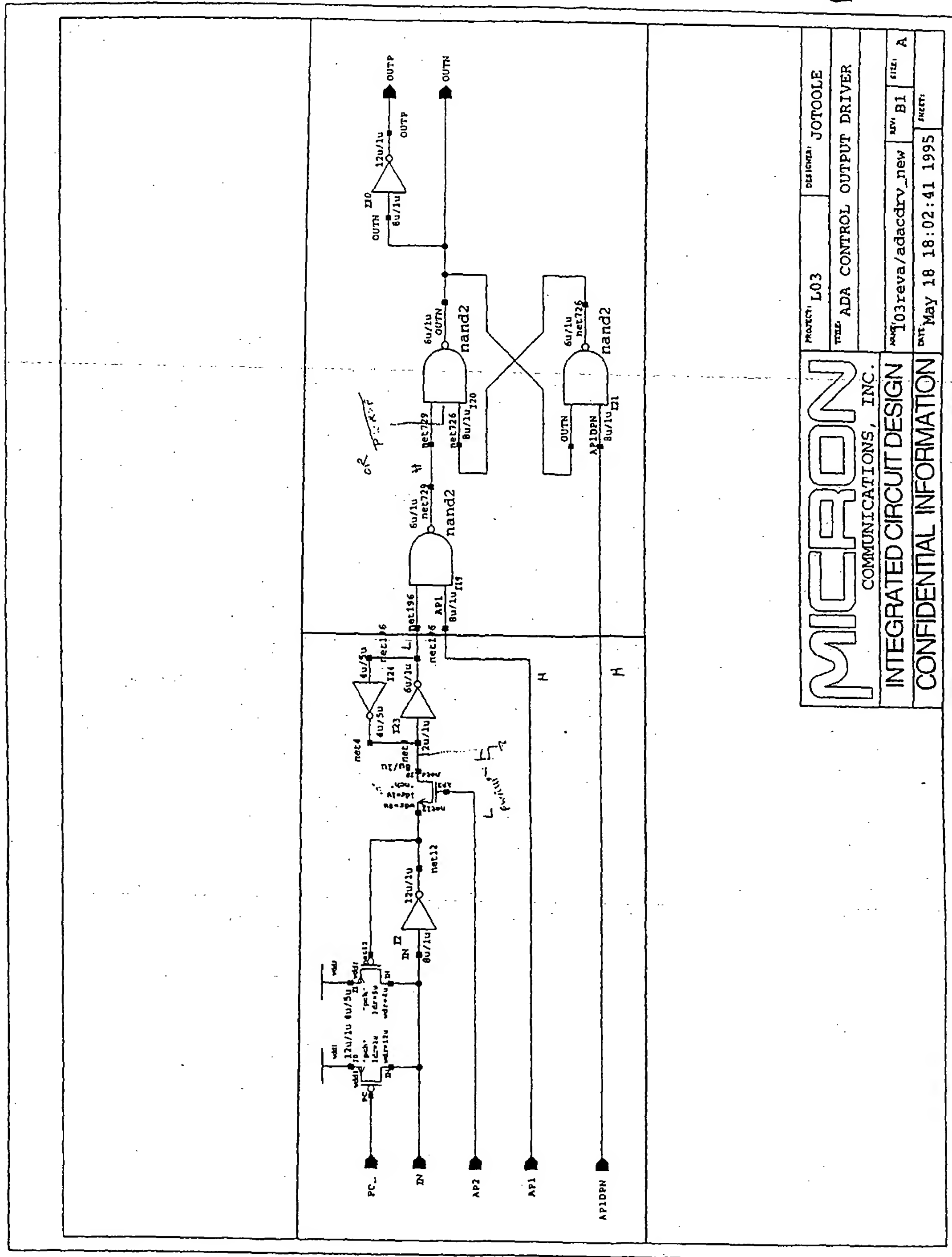
II II II II II II II II



9.010302AB

9.010302AA

MI 40-030



9.010303AA	9.010303AB
------------	------------

9.010303AA

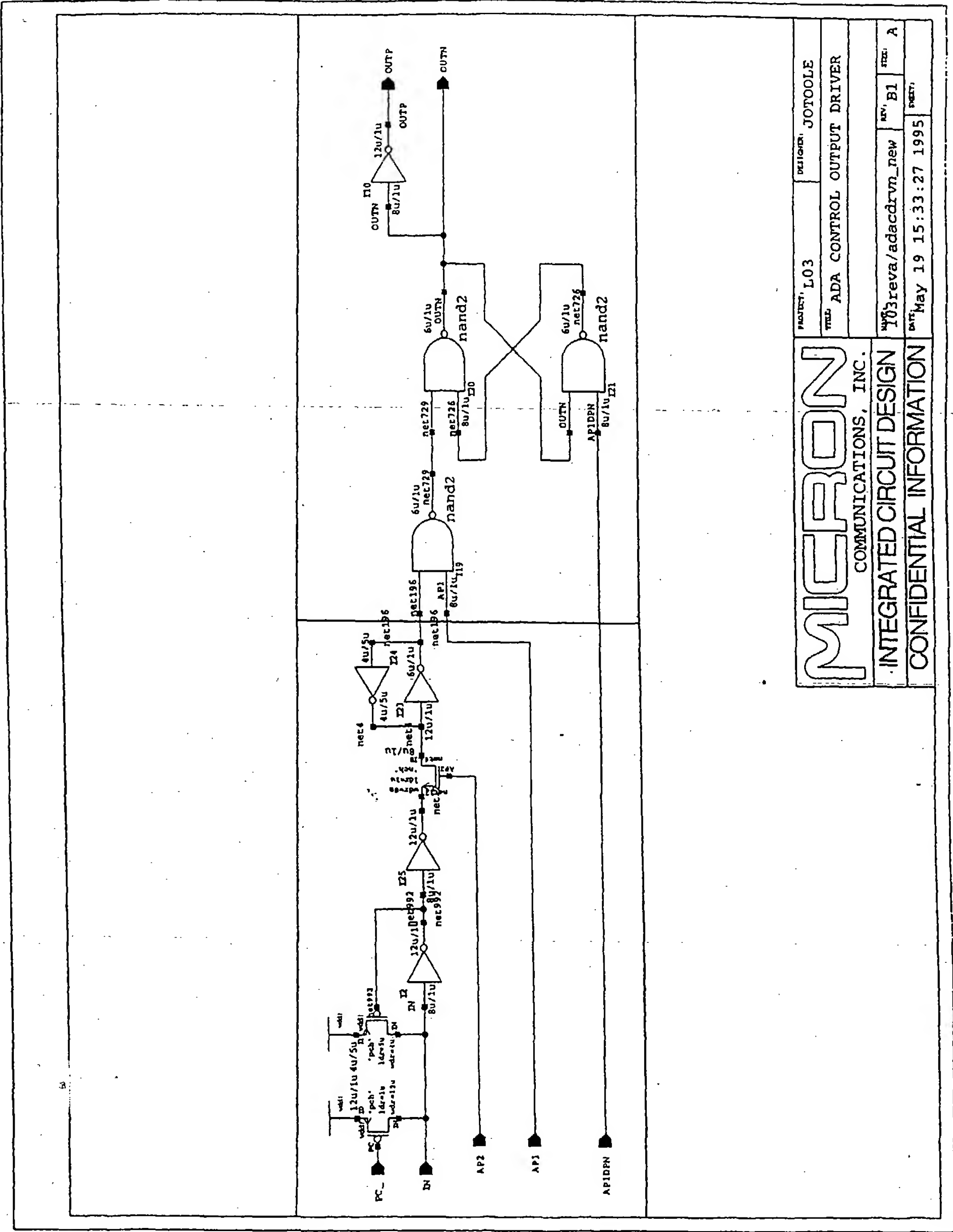


FIG. 9.010303

MICRON		PROJECT: L03	DESIGNER: JOTOOLE
COMMUNICATIONS, INC.		TITLE: ADA CONTROL OUTPUT DRIVER	
INTEGRATED CIRCUIT DESIGN		REV: B1	REV: A
CONFIDENTIAL INFORMATION		DATE: May 19 15:33:27 1995	







9.0104AA	9.0104AB	9.0104AC	9.0104AD	9.0104AE
9.0104BA	9.0104BB	9.0104BC	9.0104BD	9.0104BE
9.0104CA	9.0104CB	9.0104CC	9.0104CD	
9.0104DA	9.0104DB	9.0104DC	9.0104DD	

9.0104

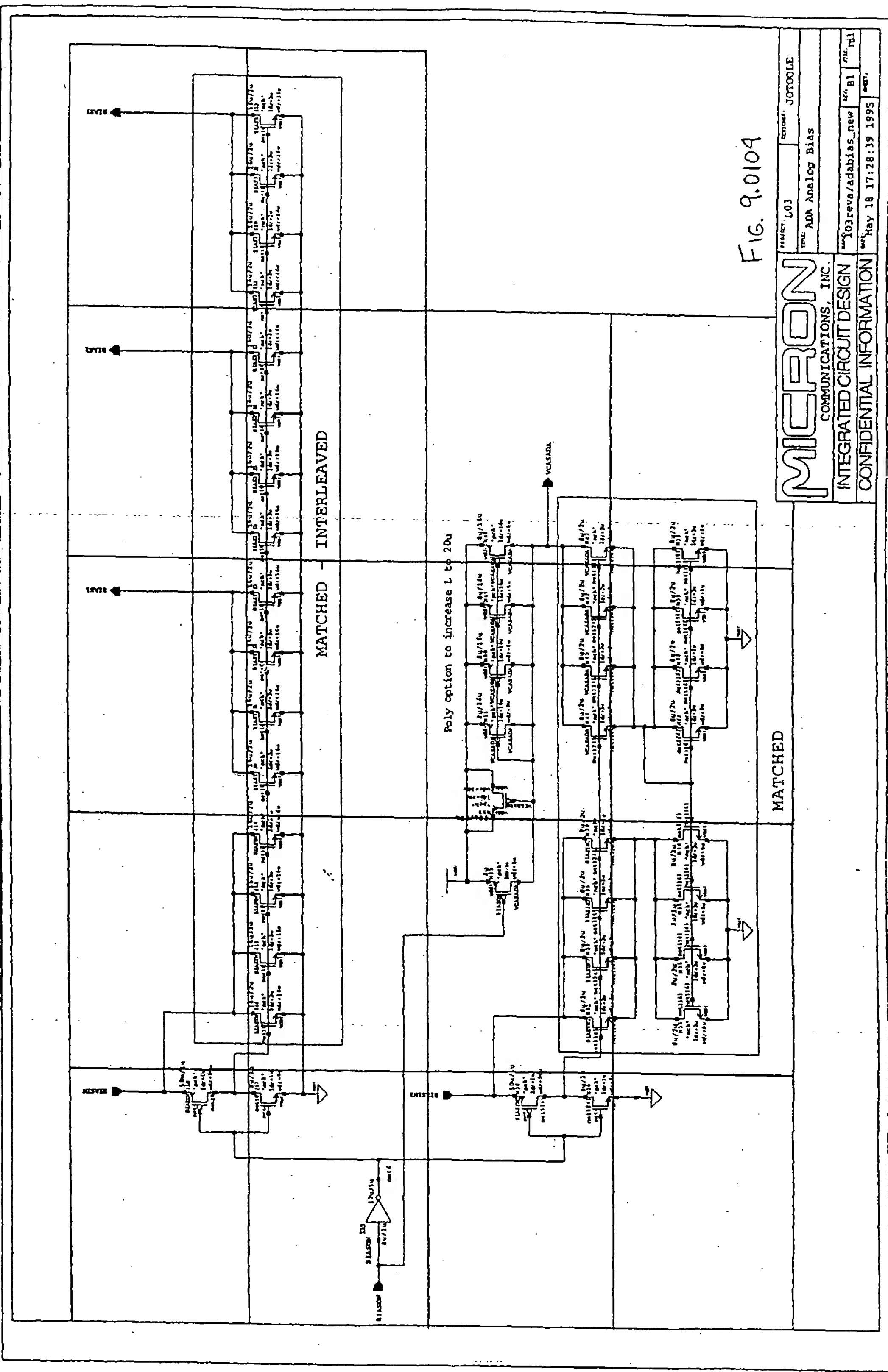
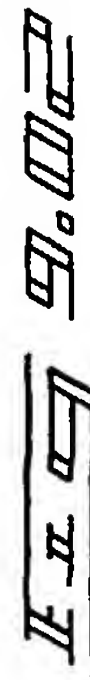
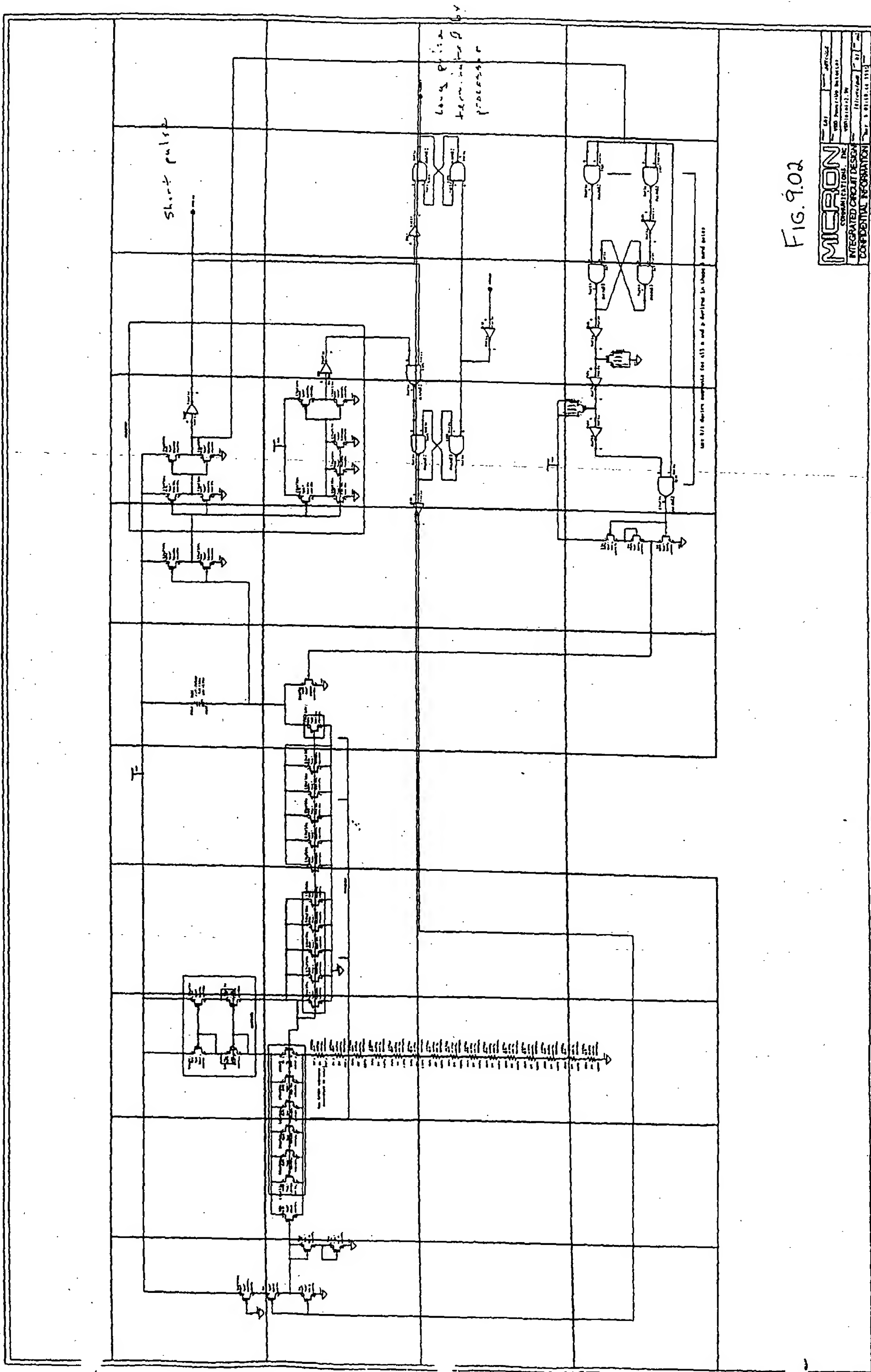


FIG. 9.0104

MICRON		REVISION	DATE
COMMUNICATIONS, INC.		L03	JOTOOLE
INTEGRATED CIRCUIT DESIGN		TITLE ADA Analog Bias	
CONFIDENTIAL INFORMATION		DESIGNER	DATE
		103revs/adabias_new	81
		May 18 17:28:39 1995	0001

9.02AA	9.02AB	9.02AC	9.02AD	9.02AE	9.02AF	9.02AG	9.02AH	9.02AI	9.02AJ	9.02AK
9.02BA	9.02BB	9.02BC	9.02BD	9.02BE	9.02BF	9.02BG	9.02BH	9.02BI	9.02BJ	9.02BK
9.02CA		9.02CC	9.02CD	9.02CE	9.02CF	9.02CG	9.02CH	9.02CI	9.02CJ	9.02CK
9.02DA	9.02DB	9.02DC	9.02DD		9.02DF	9.02DG	9.02DH	9.02DI	9.02DJ	9.02DK

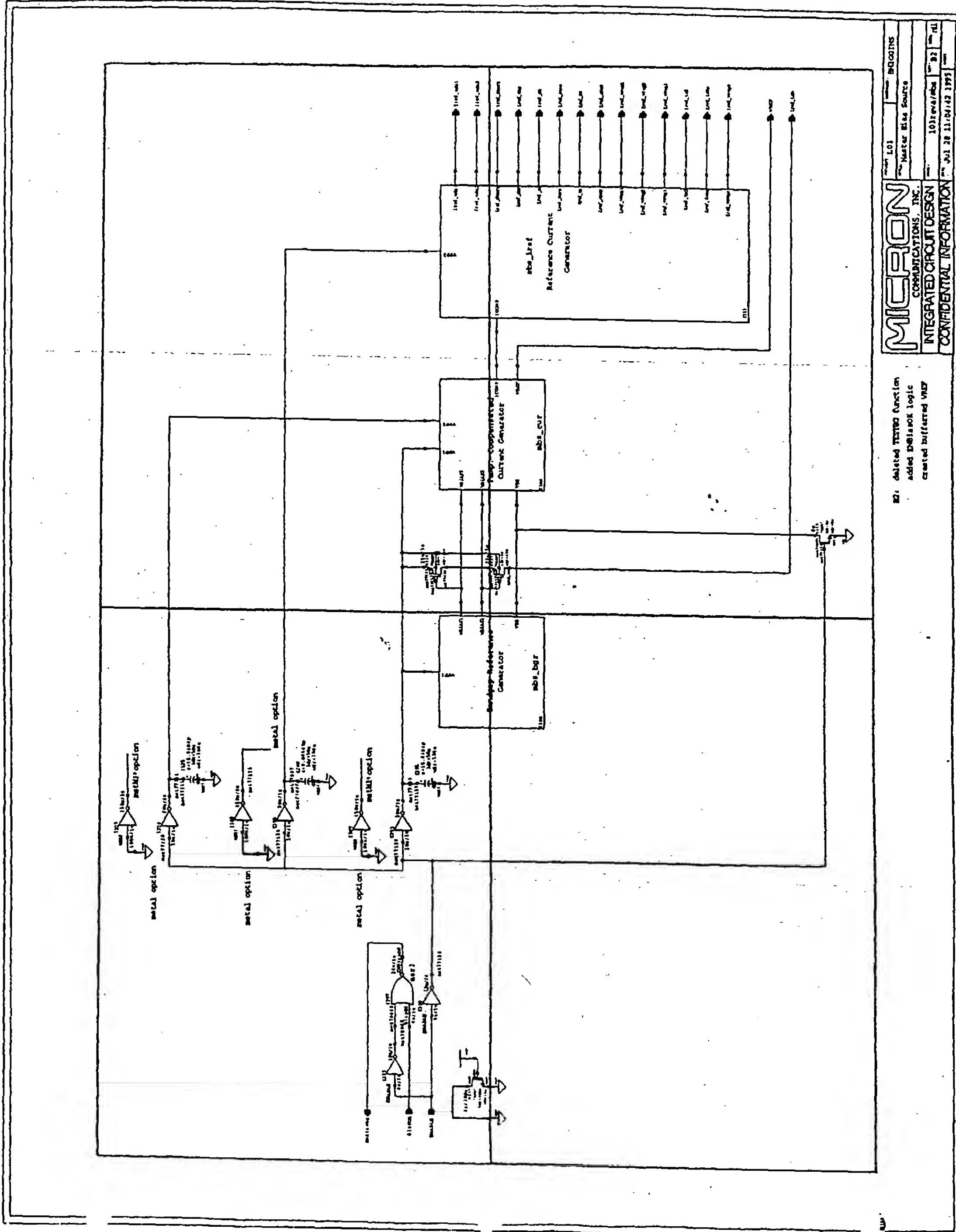




9.03AA	9.03AB
9.03BA	9.03BB

SEP 90

FIG. 9.03



82: Added TESTED function  
 added DELAY logic  
 created buffered VDD

**MICRON**  
 COMMUNICATIONS, INC.  
 INTEGRATED CIRCUIT DESIGN  
 CONFIDENTIAL INFORMATION

101  
 Master Blue Source  
 101:rev/rev  
 9-1 28 11:04:43 1995



9.0301AA	9.0301AB	9.0301AC	9.0301AD	9.0301AE	9.0301AF	9.0301AG	9.0301AH	9.0301AI	9.0301AJ
9.0301BA	9.0301BB	9.0301BC	9.0301BD	9.0301BE	9.0301BF	9.0301BG	9.0301BH	9.0301BI	9.0301BJ
9.0301CB	9.0301CC	9.0301CD	9.0301CE	9.0301CF	9.0301CG	9.0301CH	9.0301CI	9.0301CJ	
9.0301DB	9.0301DC	9.0301DD	9.0301DE	9.0301DF	9.0301DG	9.0301DH	9.0301DI	9.0301DJ	

II II III III III II

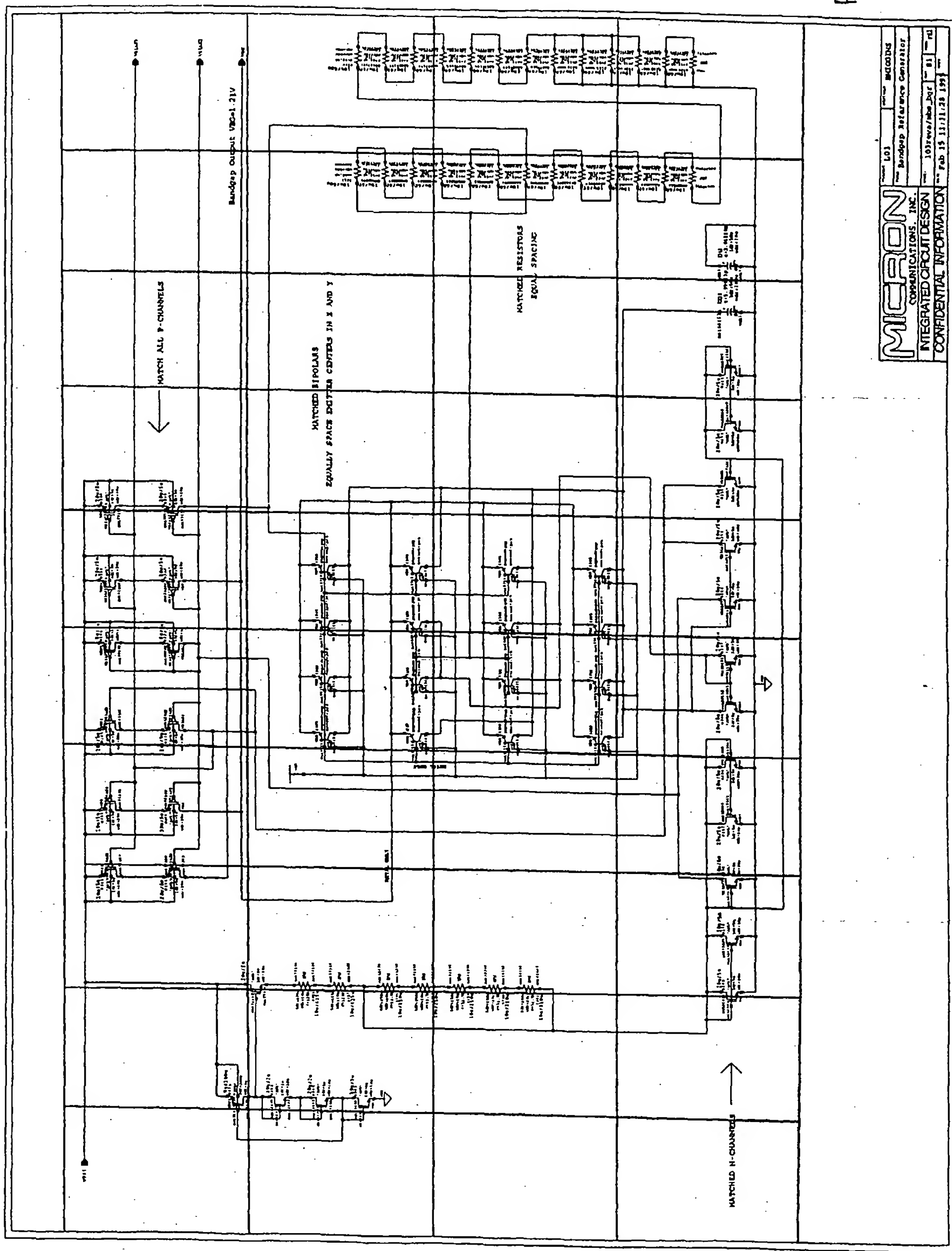


FIG. 9.0301

MICRON		L01	ENCLOSURE
COMMUNICATIONS, INC.		Bandgap Reference Generator	
INTEGRATED CIRCUIT DESIGN		103 Rev 0/Rev 0.01	81
CONFIDENTIAL INFORMATION		Feb 15 11:11:28 1991	

9.0302AA	9.0302AB	9.0302AC	9.0302AD	9.0302AE	9.0302AF	9.0302AG	9.0302AH	9.0302AI	9.0302AJ
9.0302BA	9.0302BB	9.0302BC	9.0302BD	9.0302BE	9.0302BF	9.0302BG	9.0302BH	9.0302BI	9.0302BJ
		9.0302CC	9.0302CD	9.0302CE	9.0302CF	9.0302CG	9.0302CH	9.0302CI	9.0302CJ
						9.0302DG	9.0302DH	9.0302DI	

9.0302

FIG. 9.030a

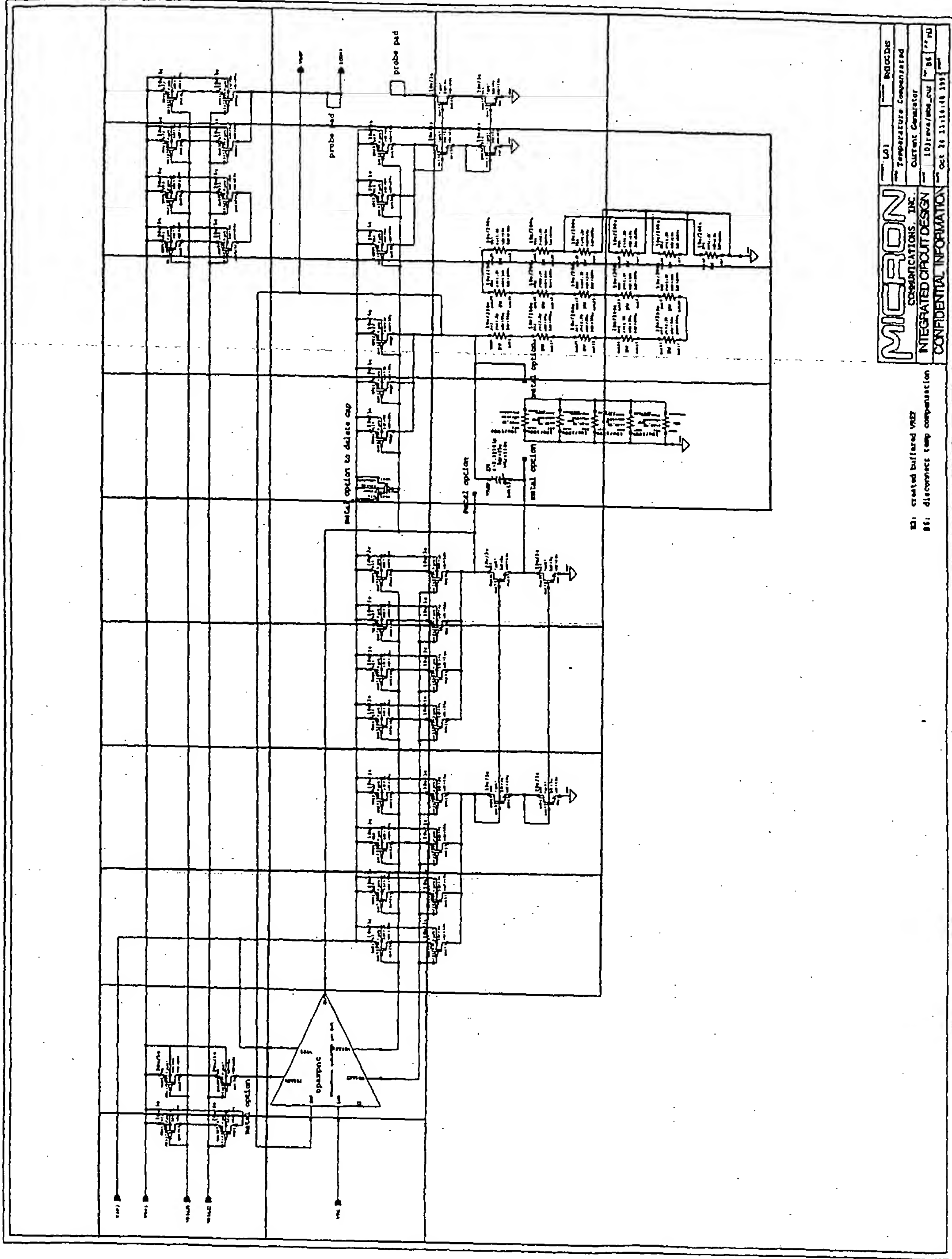
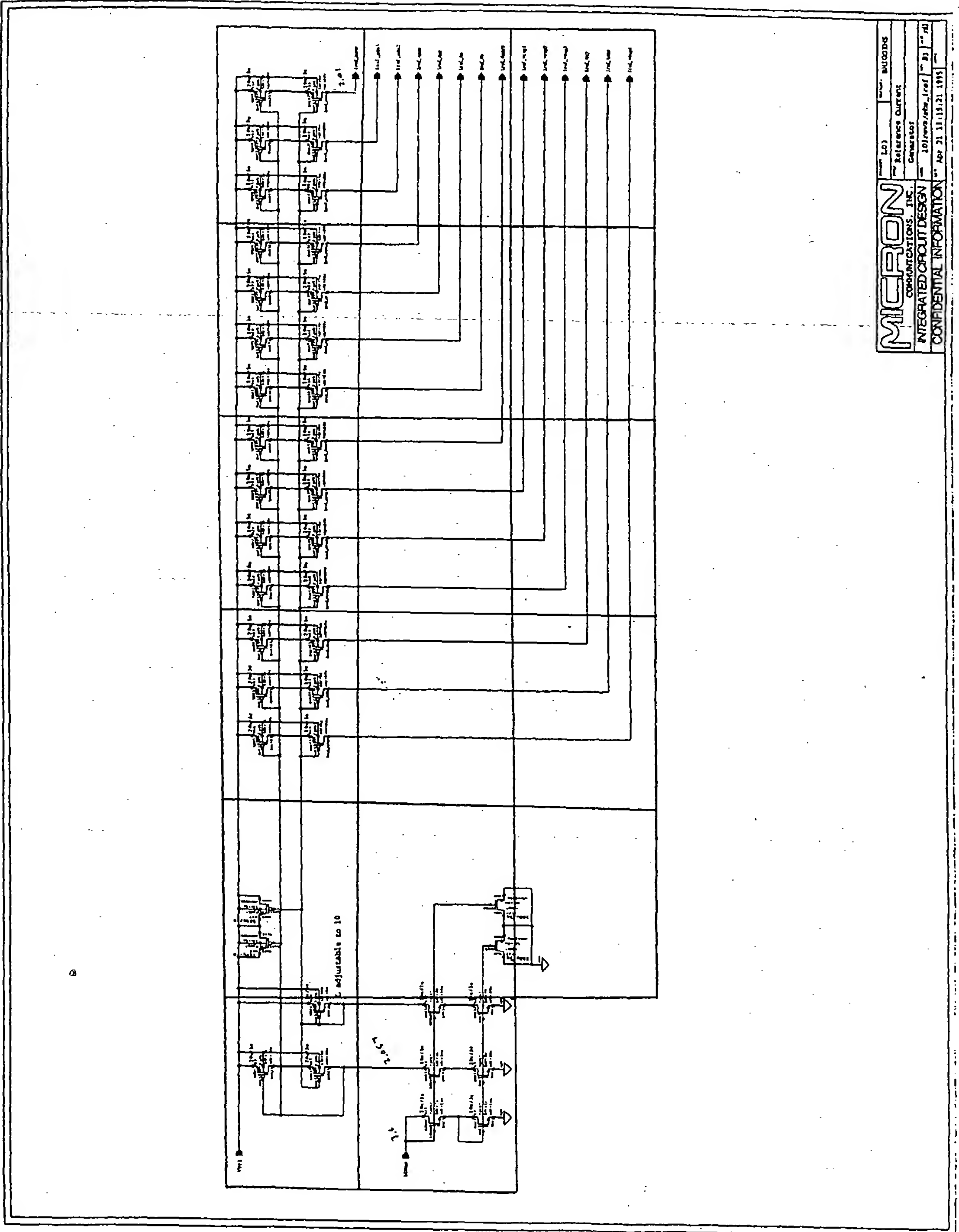




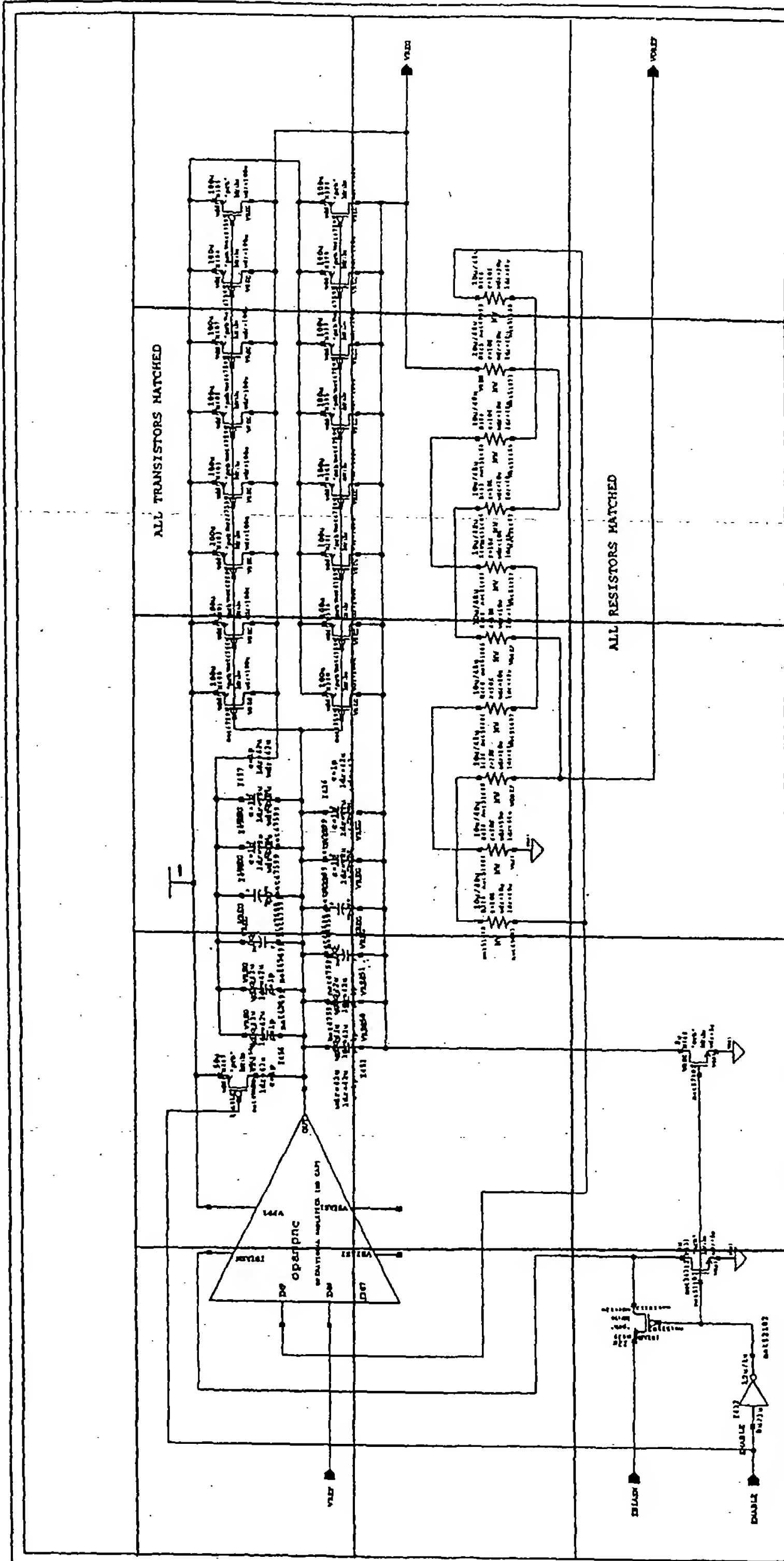
FIG. 9.0303



MICRON		101	BUDDS
COMMUNICATIONS, INC.		Reference Current	
INTEGRATED CIRCUIT DESIGN		Comparator	
CONFIDENTIAL INFORMATION		101/rev/8/8/1/rel	3
		Apr 21 11:15:21 1995	70

9.04AA	9.04AB	9.04AC	9.04AD	9.04AE
9.04BA	9.04BB	9.04BC	9.04BD	9.04BE
9.04CA	9.04CB	9.04CC	9.04CD	9.04CE

SECRET



70 20 24

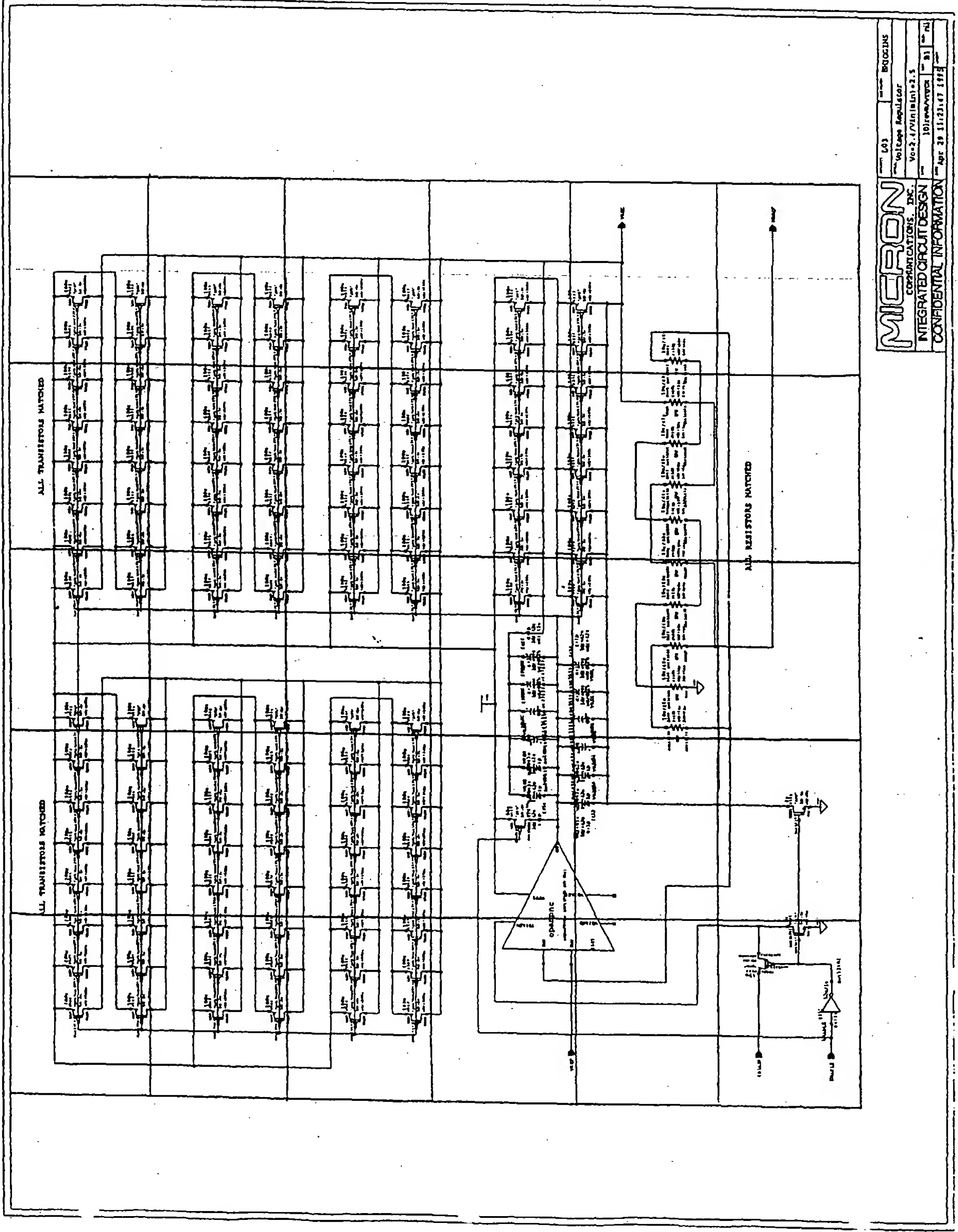
FIG. 9.04

MICRON		DESIGN: L03	DESIGNER: BHIGGINS
COMMUNICATIONS, INC.		Voltage Regulator	
INTEGRATED CIRCUIT DESIGN		V <sub>OS</sub> = 2.4/V <sub>IN</sub> (min) = 2.5	
CONFIDENTIAL INFORMATION		DATE: 10/28/94	REV: 91
		APR 29 13:22:24 1995	

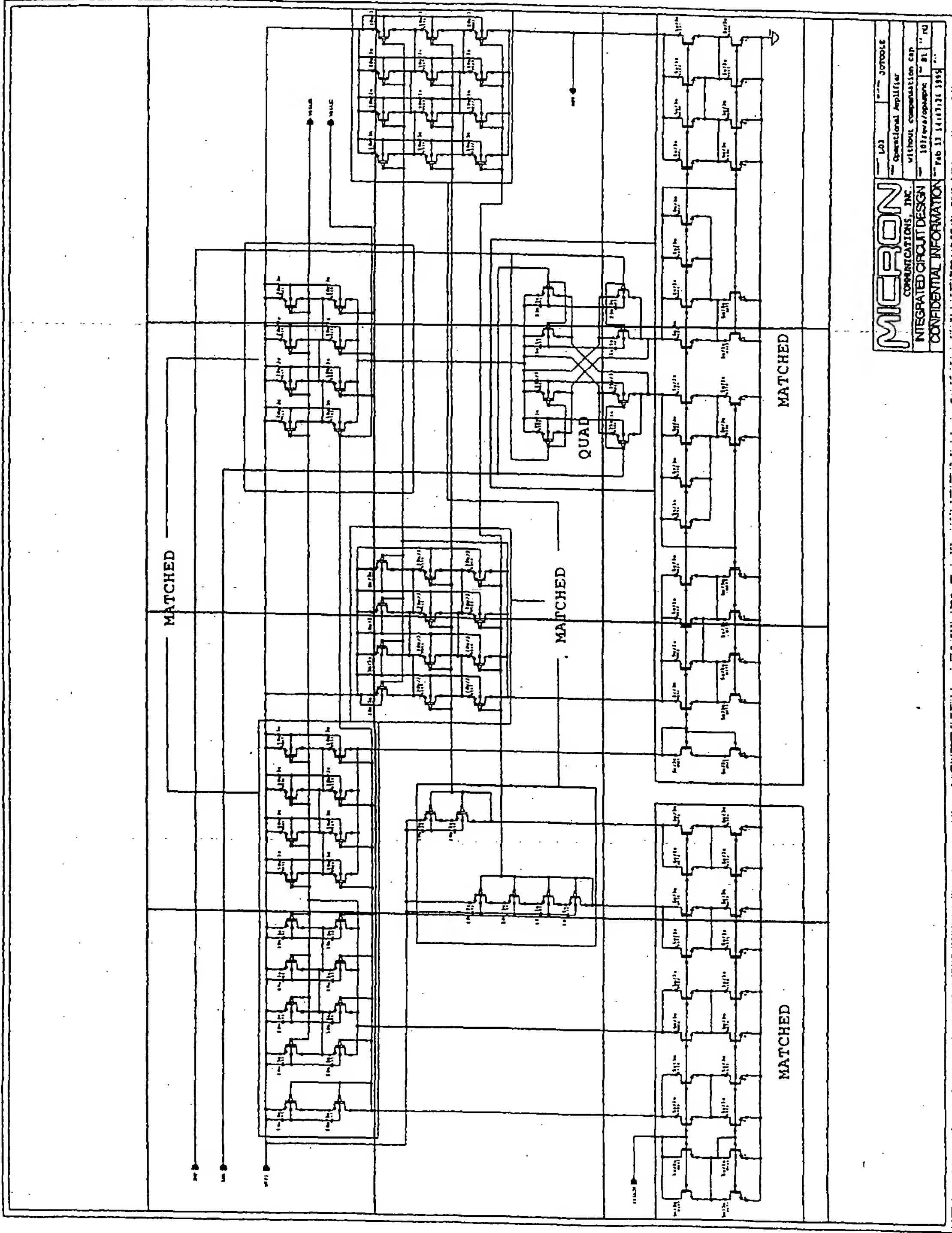


9.05AA	9.05AB	9.05AC	9.05AD	9.05AE
9.05BA	9.05BB	9.05BC	9.05BD	9.05BE
9.05CA	9.05CB	9.05CC	9.05CD	9.05CE
9.05DA	9.05DB	9.05DC	9.05DD	9.05DE
9.05EA	9.05EB	9.05EC	9.05ED	9.05EE
9.05FA	9.05FB	9.05FC	9.05FD	9.05FE

FIG. 9.05







**MICRON**  
 COMMUNICATIONS, INC.  
 INTEGRATED CIRCUIT DESIGN  
 CONFIDENTIAL INFORMATION

101  
 Operational Amplifier  
 without compensation cap  
 101Teva/Opamp  
 81  
 Feb 11 14:15:31 1984

Fig. 9.0501

9.06AA	9.06AB	9.06AC	9.06AD	9.06AE
9.06BA	9.06BB	9.06BC	9.06BD	9.06BE
9.06CA	9.06CB	9.06CC	9.06CD	
9.06DA	9.06DB	9.06DC	9.06DD	

SECRET

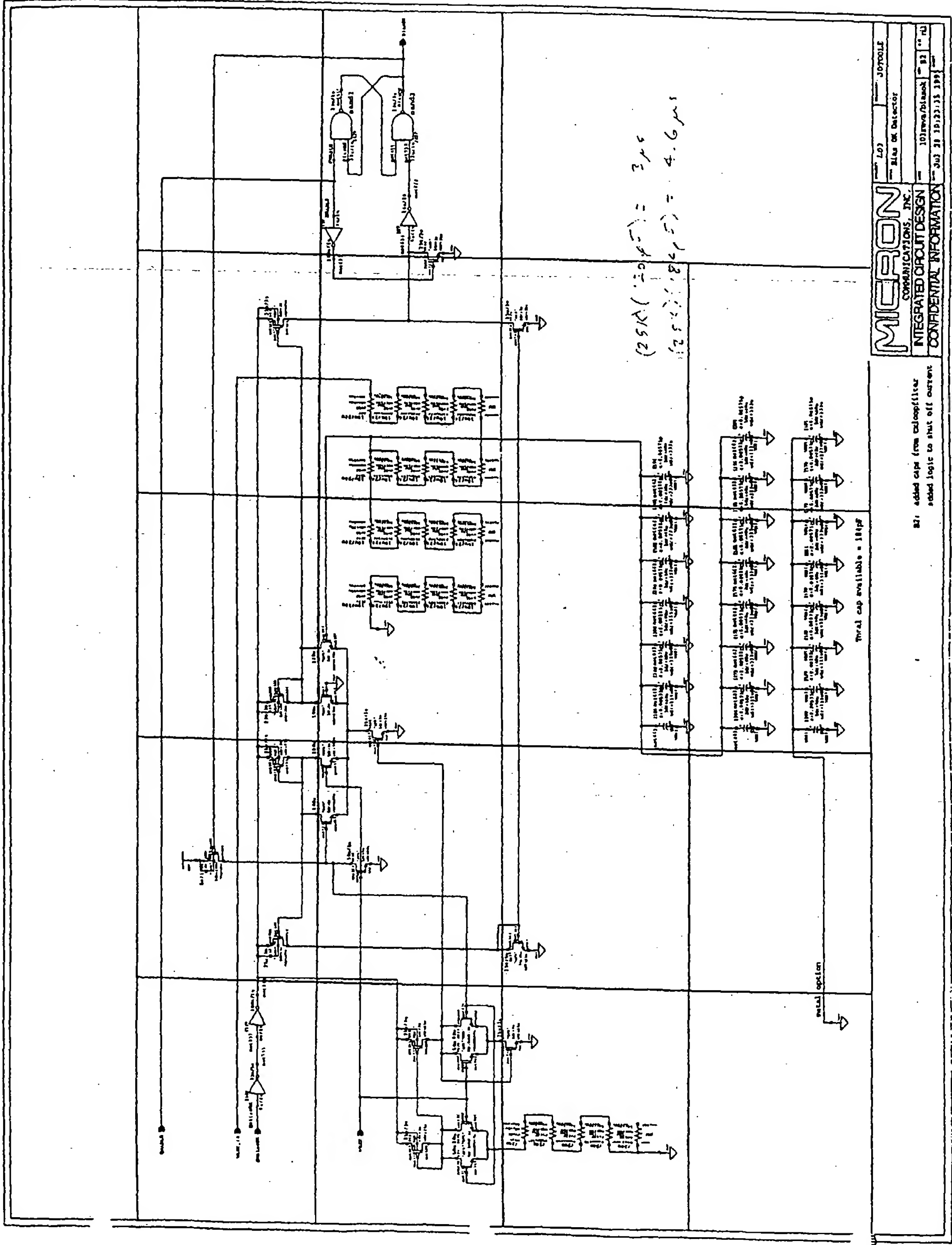


Fig. 9.06

9.07AA	9.07AB	9.07AC	9.07AD	9.07AE	9.07AF	9.07AG	9.07AH	9.07AI
9.07BA	9.07BB	9.07BC	9.07BD	9.07BE	9.07BF	9.07BG	9.07BH	9.07BI
9.07CA	9.07CB	9.07CC	9.07CD	9.07CE	9.07CF	9.07CG	9.07CH	
9.07DA	9.07DB	9.07DC	9.07DD	9.07DE	9.07DF	9.07DG		
9.07EA	9.07EB	9.07EC	9.07ED	9.07EE	9.07EF	9.07EG		

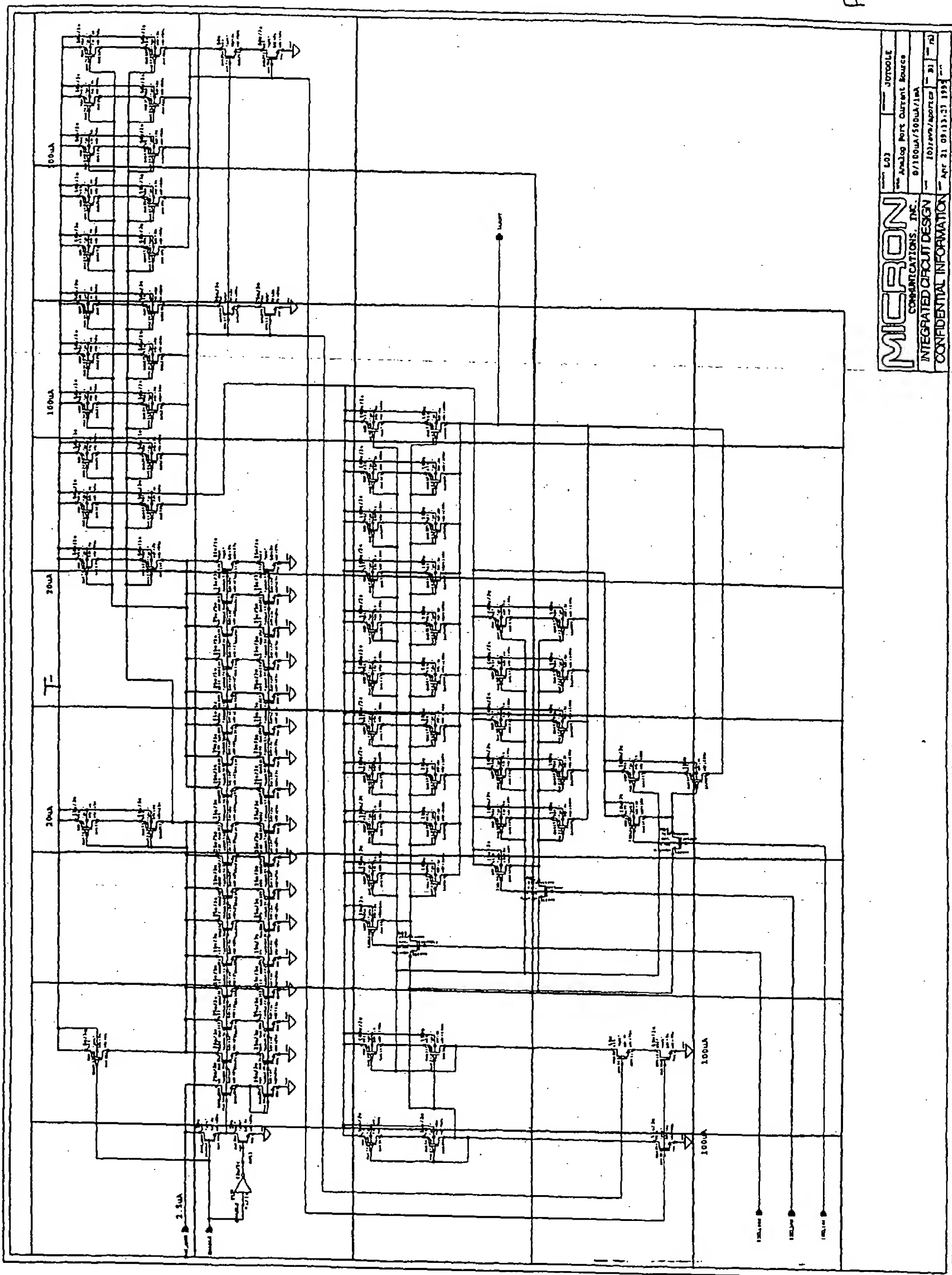
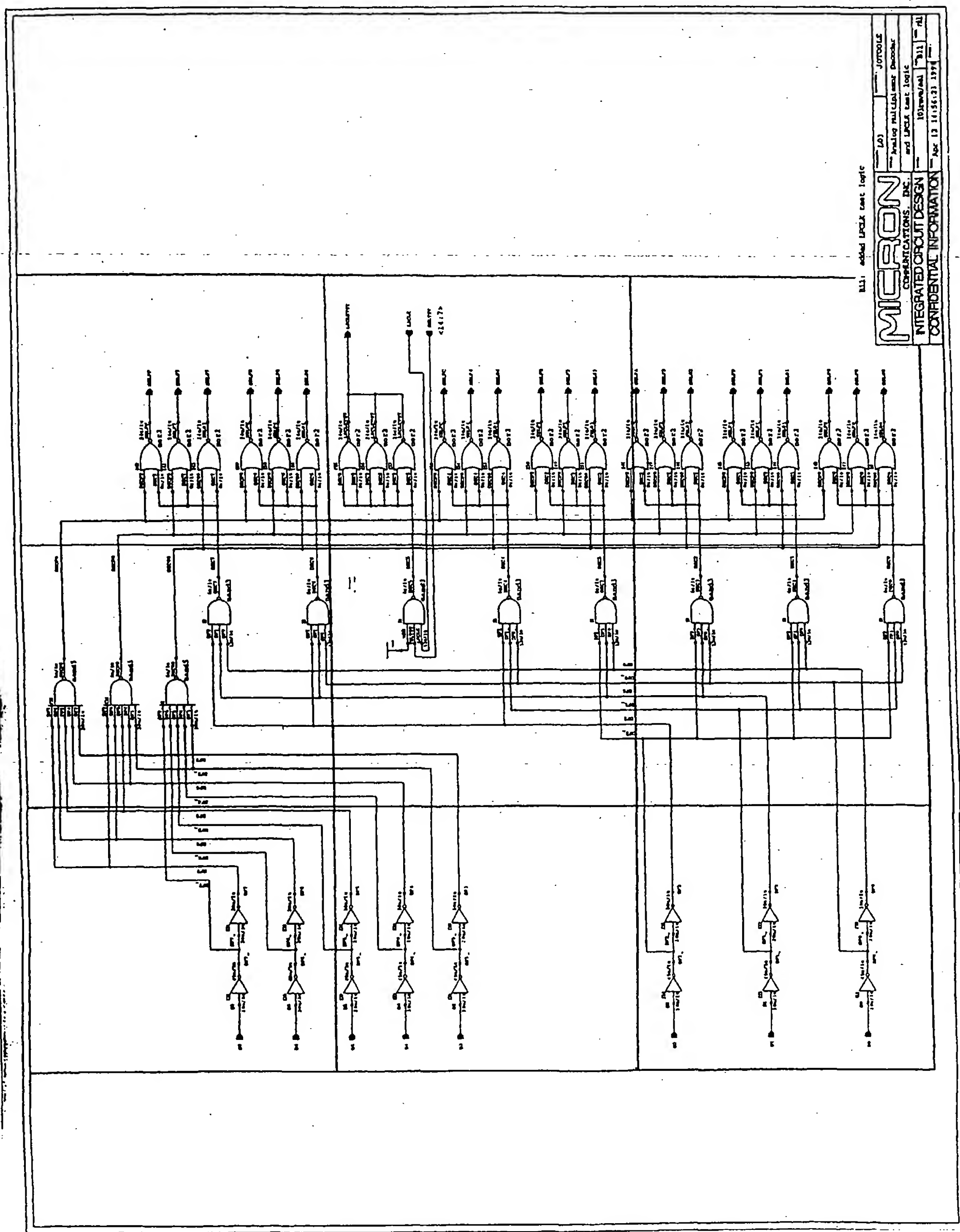


Fig. 9.07



9.08AA	9.08AB	9.08AC
9.08BA	9.08BB	9.08BC
9.08CA	9.08CB	9.08CC



9.09AA	9.09AB
9.09BA	9.09BB

EX-99

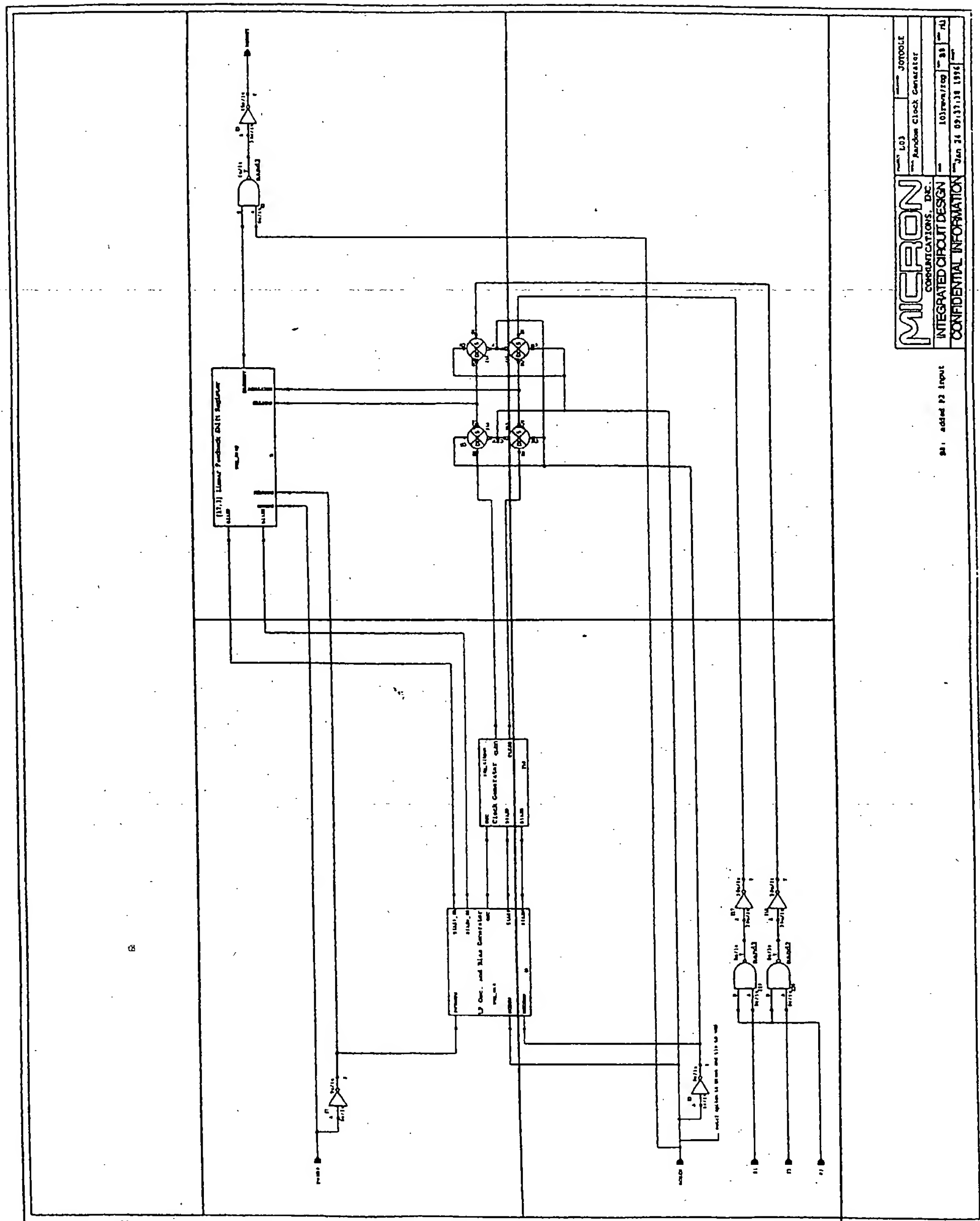


Fig. 9.09

9.0901AA	9.0901AB	9.0901AC	9.0901AD	9.0901AE	9.0901AF	9.0901AG	9.0901AH
9.0901BA	9.0901BB	9.0901BC	9.0901BD	9.0901BE	9.0901BF	9.0901BG	9.0901BH
9.0901CA	9.0901CB	9.0901CC	9.0901CD	9.0901CE	9.0901CF	9.0901CG	9.0901CH

II II III III III III

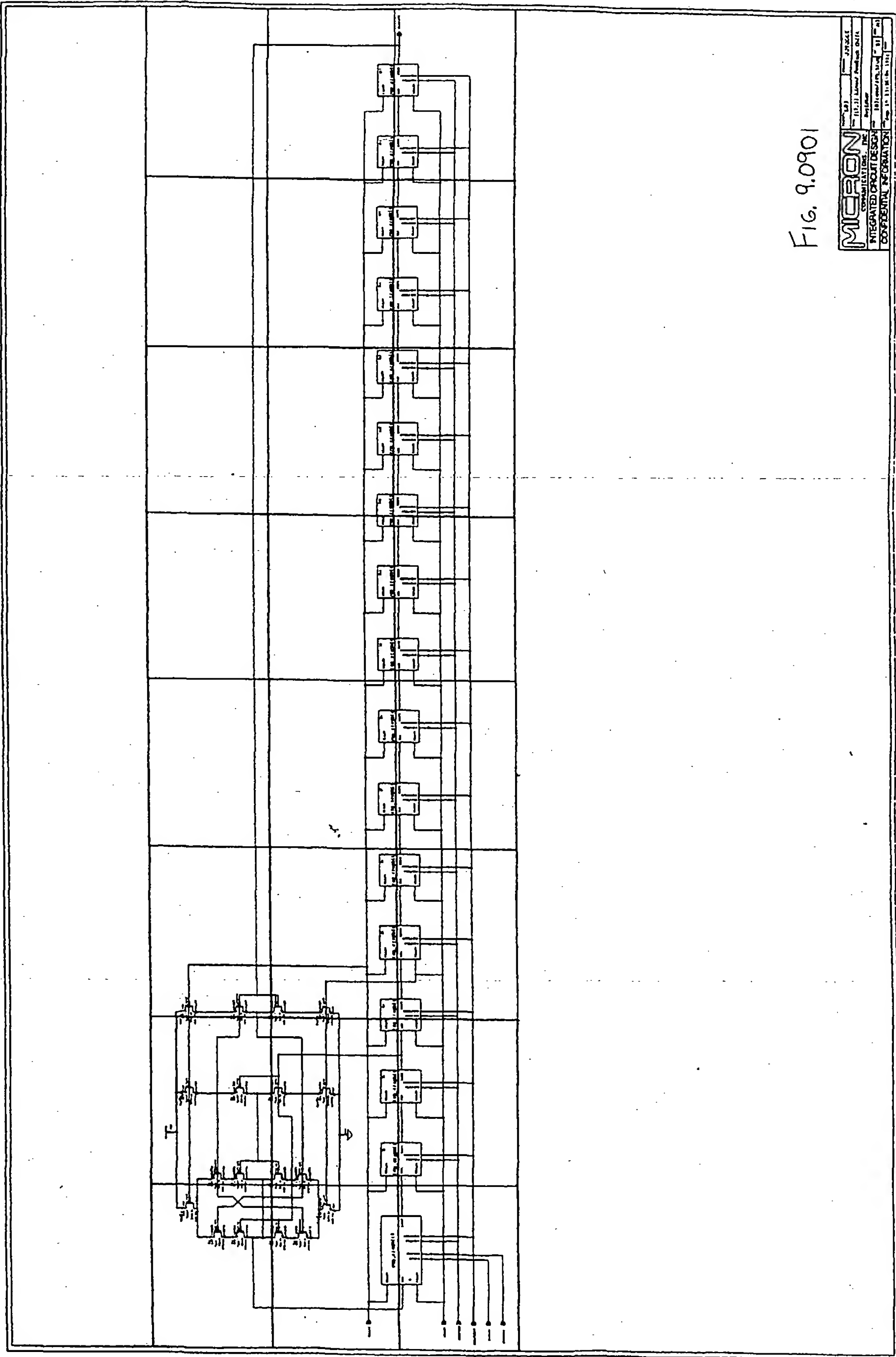
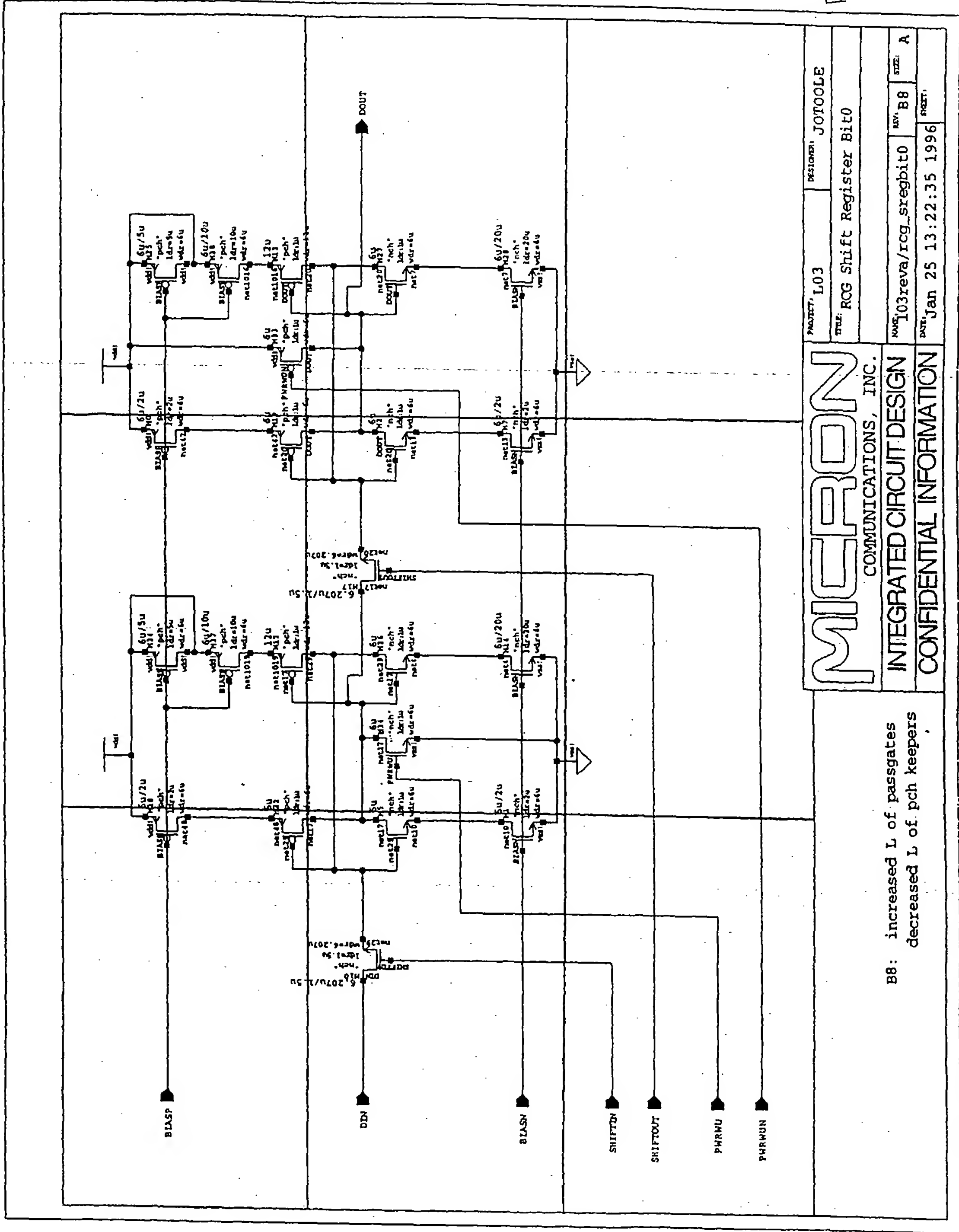


Fig. 9.0901

9.090101AA	9.090101AB	9.090101AC
9.090101BA	9.090101BB	9.090101BC
9.090101CA	9.090101CB	9.090101CC

II II III III III III III III



**MICRON**  
COMMUNICATIONS, INC.

PROJECT: L03 DESIGNER: JOTOOLE  
TITLE: RCG Shift Register Bit0  
NAME: j03reva/rcg\_sregbit0 REV: B8 SIZE: A  
DATE: Jan 25 13:22:35 1996 SHEET: 1

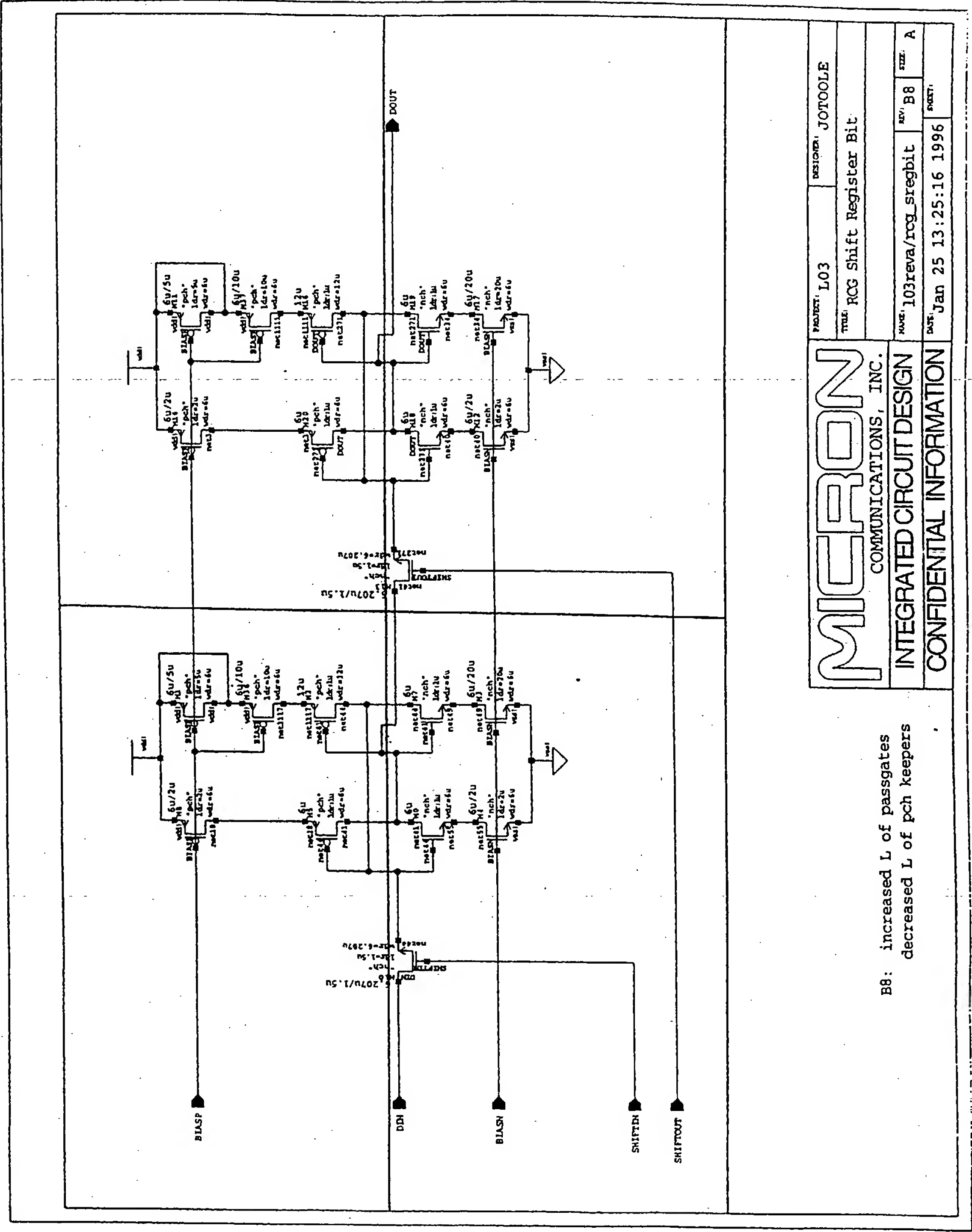
B8: increased L of passgates  
decreased L of pch keepers

FIG. 9.090101



9.090102AA	9.090102AB
9.090102BA	9.090102BB

9.090102



B8: increased L of passgates  
decreased L of pch keepers

**MICRON**  
COMMUNICATIONS, INC.

INTEGRATED CIRCUIT DESIGN  
CONFIDENTIAL INFORMATION

PROJECT: L03	DESIGNER: JOTOOLE
TITLE: RCG Shift Register Bit	
NAME: 103reva/rcg_sregbit	REV: B8
DATE: Jan 25 13:25:16 1996	SIZE: A

9.0902AA	9.0902AB	9.0902AC	9.0902AD	9.0902AE	9.0902F	9.0902AG	9.0902AH	9.0902AI	9.0902AJ	9.0902AK	9.0902AL
9.0902BA	9.0902BB	9.0902BC	9.0902BD	9.0902BE	9.0902F	9.0902BG	9.0902BH	9.0902BI	9.0902BJ	9.0902BK	9.0902BL
		9.0902CC	9.0902CD	9.0902CE	9.0902F	9.0902CG	9.0902CH	9.0902CI	9.0902CJ	9.0902CK	9.0902CL
		9.0902DC	9.0902DD	9.0902DE	9.0902F						9.0902DL
9.0902EA	9.0902EB	9.0902EC	9.0902ED	9.0902EE	9.0902F	9.0902EG	9.0902EH	9.0902EI	9.0902EJ	9.0902EK	9.0902EL
			9.0902FD	9.0902FE	9.0902F	9.0902FG	9.0902FH	9.0902FI	9.0902FJ	9.0902FK	9.0902FL

9.0902



9.0903AA	9.0903AB	9.0903AC
9.0903BA	9.0903BB	9.0903BC
9.0903CA	9.0903CB	9.0903CC

LEWIS & CLARK

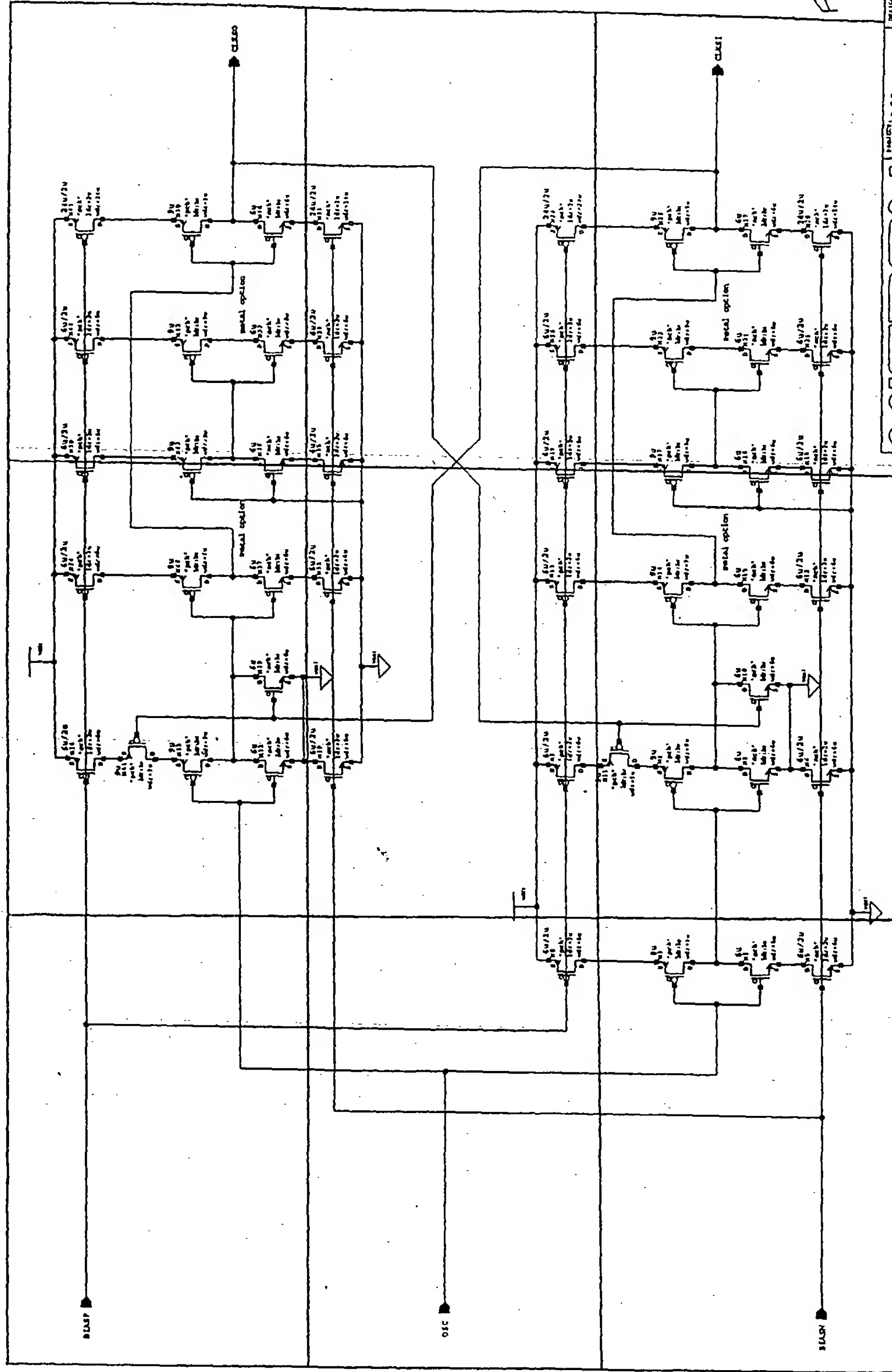


FIG. 9.0903

**MICRON**  
COMMUNICATIONS, INC.

INTEGRATED CIRCUIT DESIGN  
CONFIDENTIAL INFORMATION

DESIGN: L03  
MIL Clock Generator

DATE: 103revA/rcg\_clkgen  
REV: B8  
JAN 24 09:56:43 1996

B8: wired cross-couples to ground

10AA	10AB	10AC	10AD
10BA	10BB	10BC	10BD
10CA	10CB	10CC	10CD
10DA	10DB	10DC	10DD

II II II II

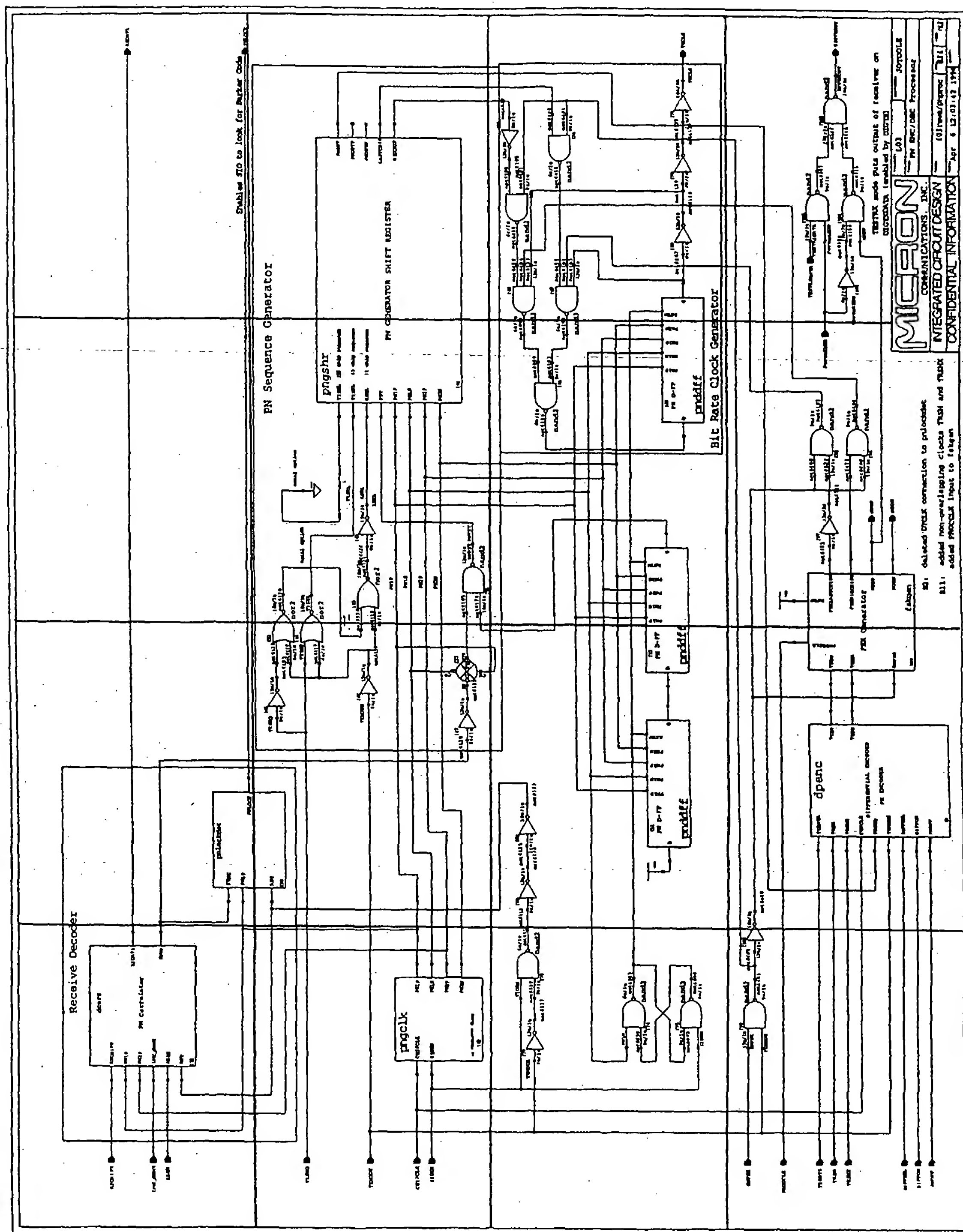


Fig. 10



10.01AA	10.01AB	10.01AC	10.01AD	10.01AE	10.01AF	10.01AG			
10.01BA	10.01BB	10.01BC	10.01BD	10.01BE	10.01BF	10.01BG	10.01BH	10.01BI	10.01BJ
10.01CA	10.01CB	10.01CC	10.01CD	10.01CE	10.01CF	10.01CG	10.01CH	10.01CI	10.01CJ
	10.01DB	10.01DC	10.01DD	10.01DE	10.01DF	10.01DG	10.01DH	10.01DI	10.01DJ

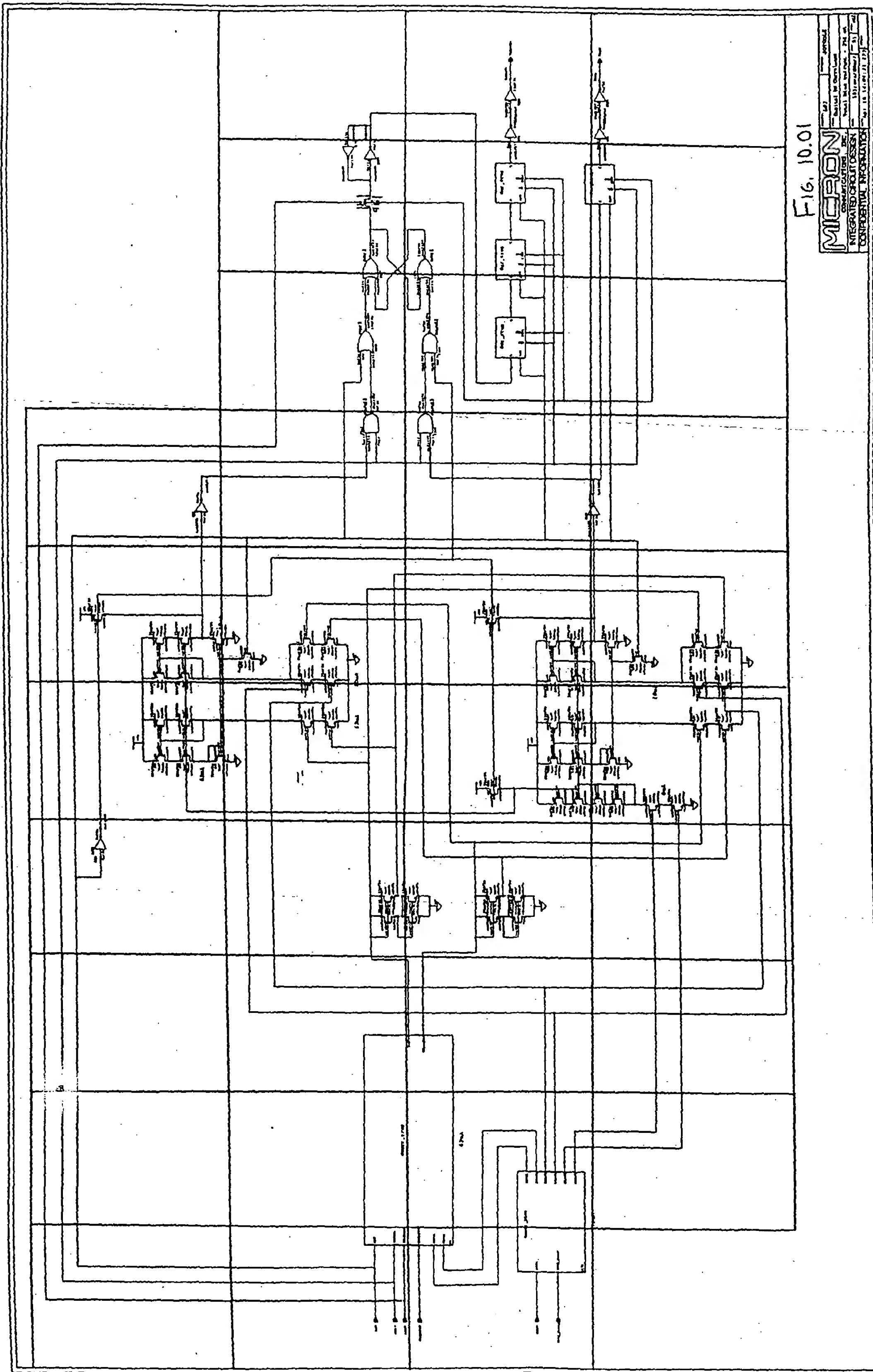


Fig. 10.01

**MICRON**  
INTEGRATED CIRCUIT DESIGN  
CONFIDENTIAL INFORMATION  
No. 10.01.01.01  
Rev. 10.01.01.01  
Date 10.01.01.01  
By 10.01.01.01  
Checked by 10.01.01.01  
Approved by 10.01.01.01

10.0101AA	10.0101AB	10.0101AC	10.0101AD	10.0101AE	10.0101AF	10.0101AG
10.0101BA	10.0101BB	10.0101BC	10.0101BD	10.0101BE	10.0101BF	10.0101BG

10.0101

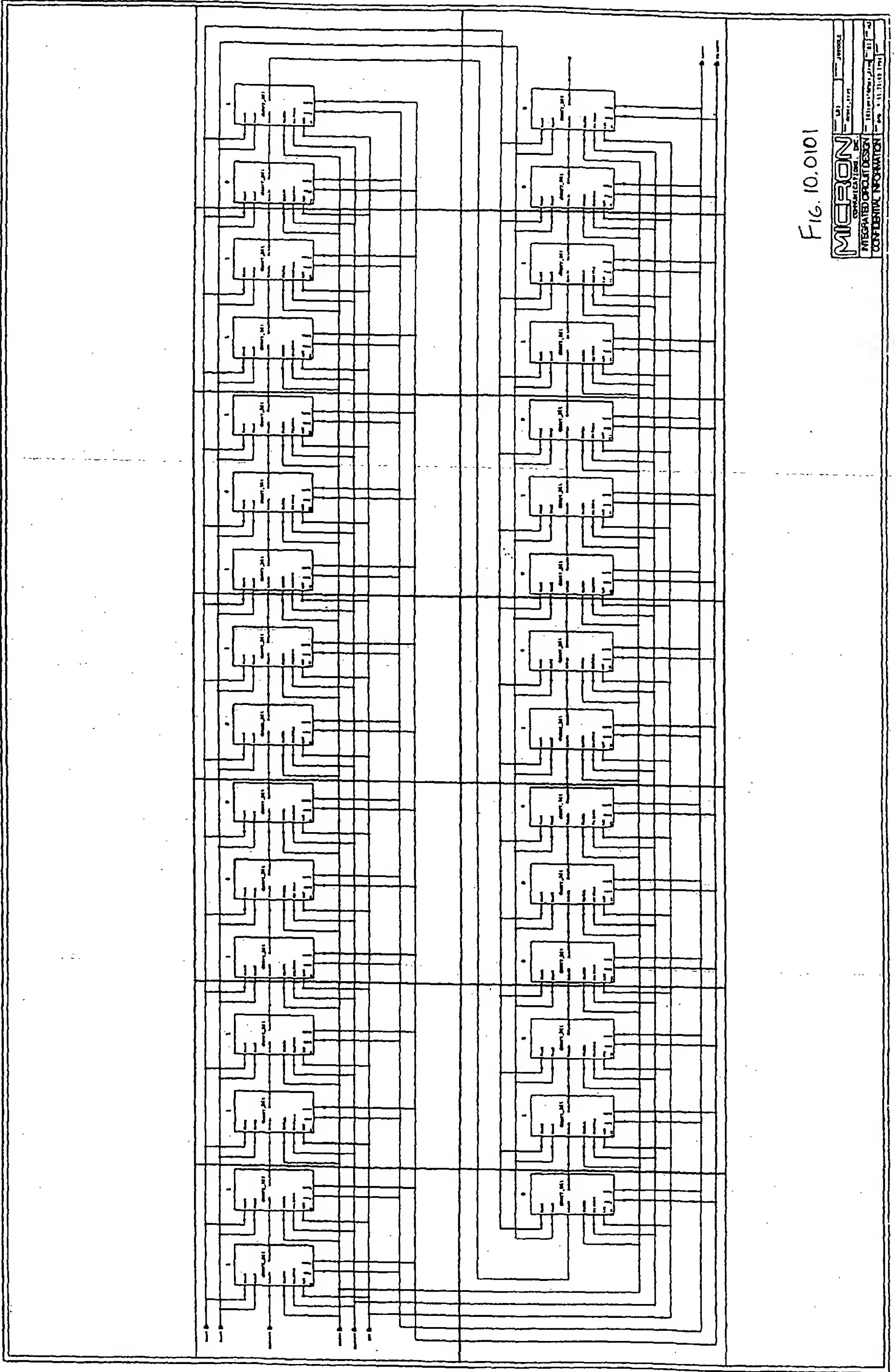


FIG. 10.0101

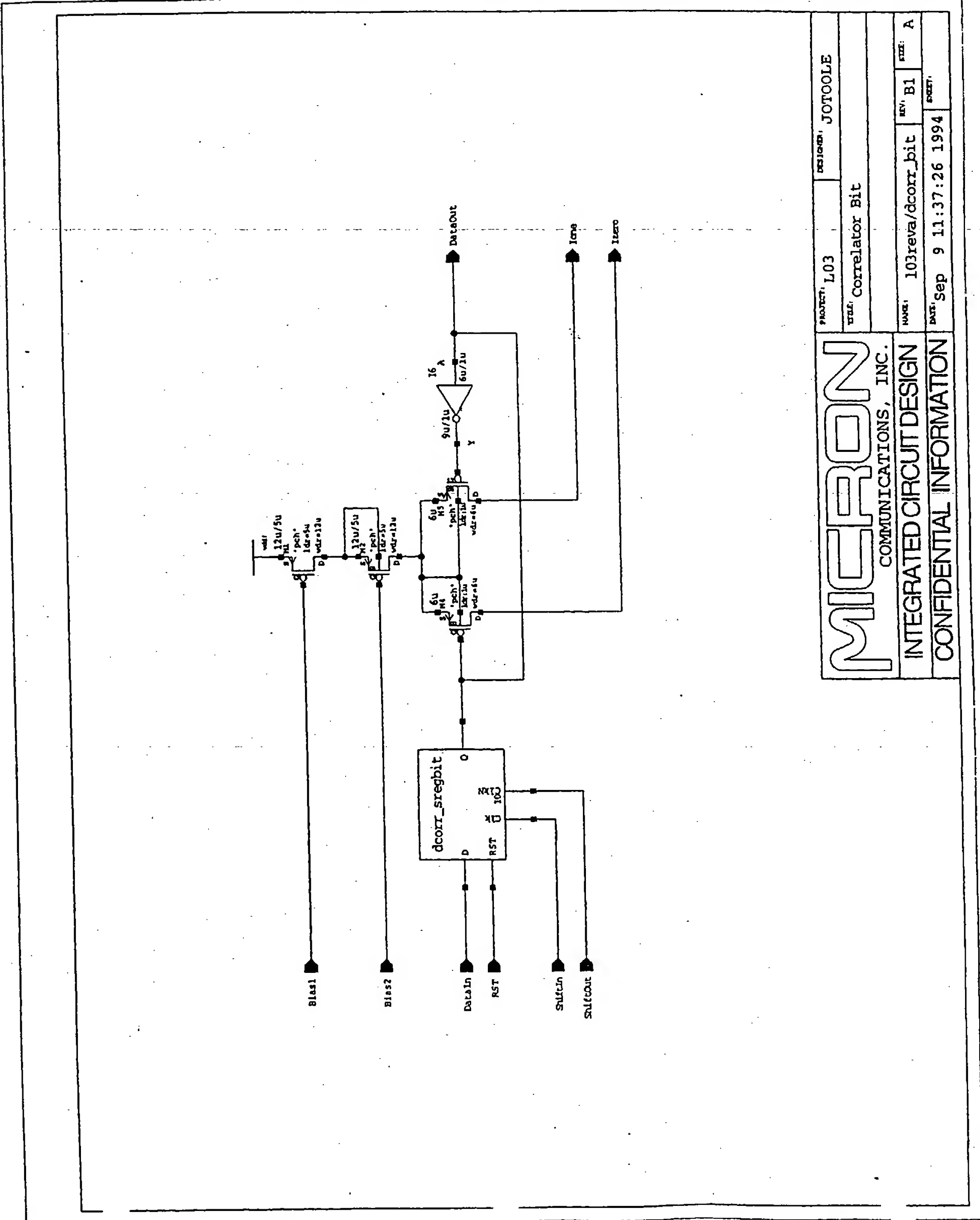


FIG. 10.010101

MICRON		PRODUCT: L03	DESIGN: J000LE
COMMUNICATIONS, INC.		TITLE: Correlator Bit	
INTEGRATED CIRCUIT DESIGN		NAME: 103reva/dcorr_bit	REV: B1
CONFIDENTIAL INFORMATION		DATE: Sep 9 11:37:26 1994	SIZE: A

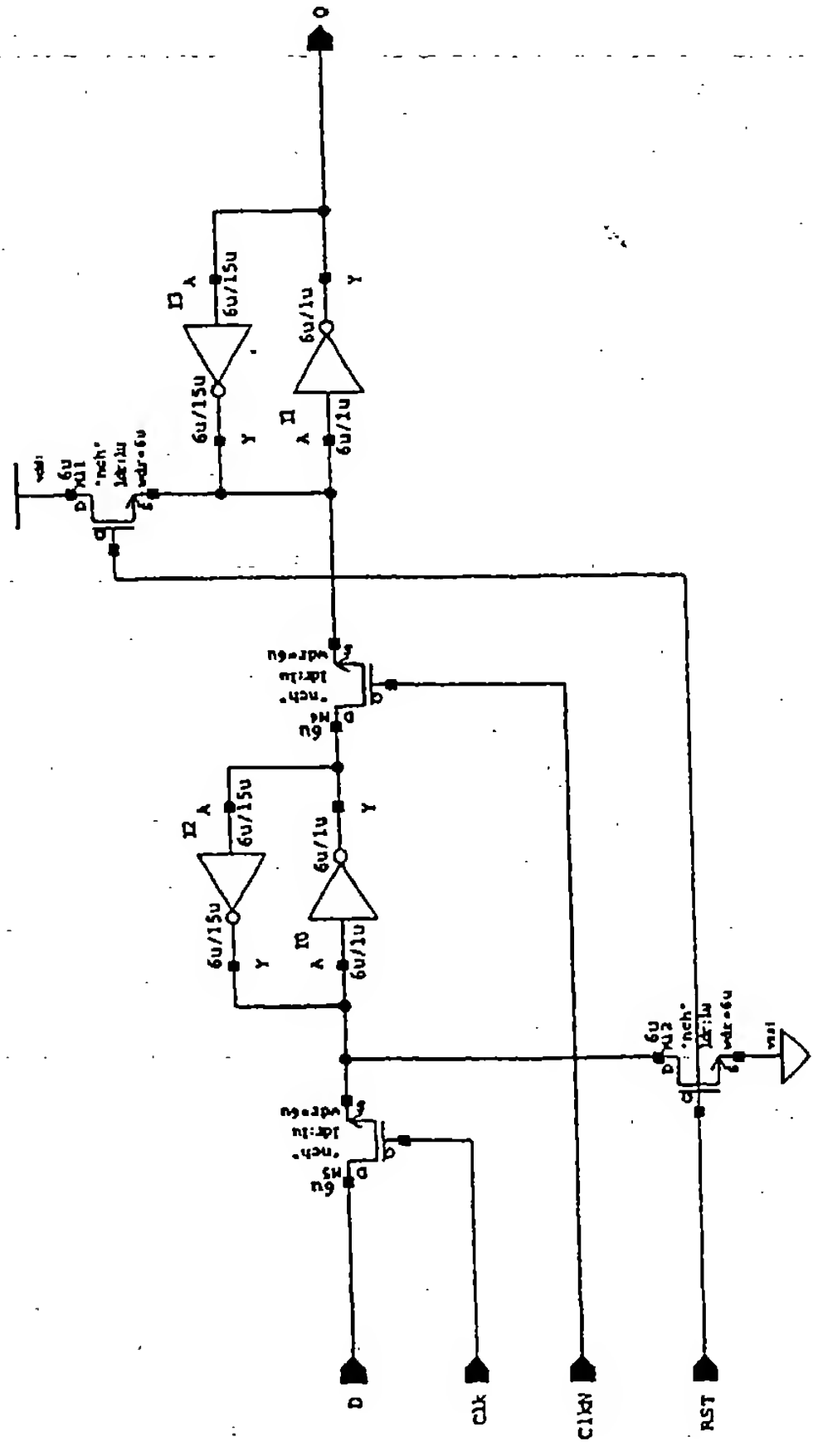


FIG. 10.01010101

PROJECT: L03		DESIGNER: JOTOOLE	
TITLE: Shift Register Cell			
W4103reva/dcorr_sregbit		REV: B1	SIZE: A
DATE: Sep 9 14:08:50 1994		SHEET: 1	

**MICRON**  
 COMMUNICATIONS, INC.  
 INTEGRATED CIRCUIT DESIGN  
 CONFIDENTIAL INFORMATION

10.0102AA	10.0102AB	10.0102AC	10.0102AD	10.0102AE	10.0102AF	10.0102AG	10.0102AH	10.0101AI	10.0102AJ	10.0102AK	10.0102AL	10.0102AM	10.0102AN
10.0102BA	10.0102BB	10.0102BC	10.0102BD	10.0102BE	10.0102BF	10.0102BG	10.0102BH	10.0101AI	10.0102BJ	10.0102BK	10.0102BL	10.0102BM	10.0102BN
									10.0102CJ	10.0102CK	10.0102CL	10.0102CM	10.0102CN

10.0102





10.02AA	10.02AB	10.02AC	10.02AD	10.02AE
10.02BA	10.02BB	10.02BC	10.02BD	10.02BE

II II II II II II II II

Figure 1 is a schematic diagram of a 4-bit ripple-carry adder circuit. The circuit is composed of four full-adder blocks (74181) and four half-adder blocks (74181). The inputs are labeled A, B, and C. The outputs are labeled S (Sum) and C (Carry). The circuit is divided into two sections by a vertical dashed line. The left section contains the first two full-adder blocks and the first half-adder block. The right section contains the remaining two full-adder blocks and the second half-adder block. The circuit is powered by a 5V supply and ground. The output S is connected to a 5V supply and ground. The output C is connected to a 5V supply and ground.

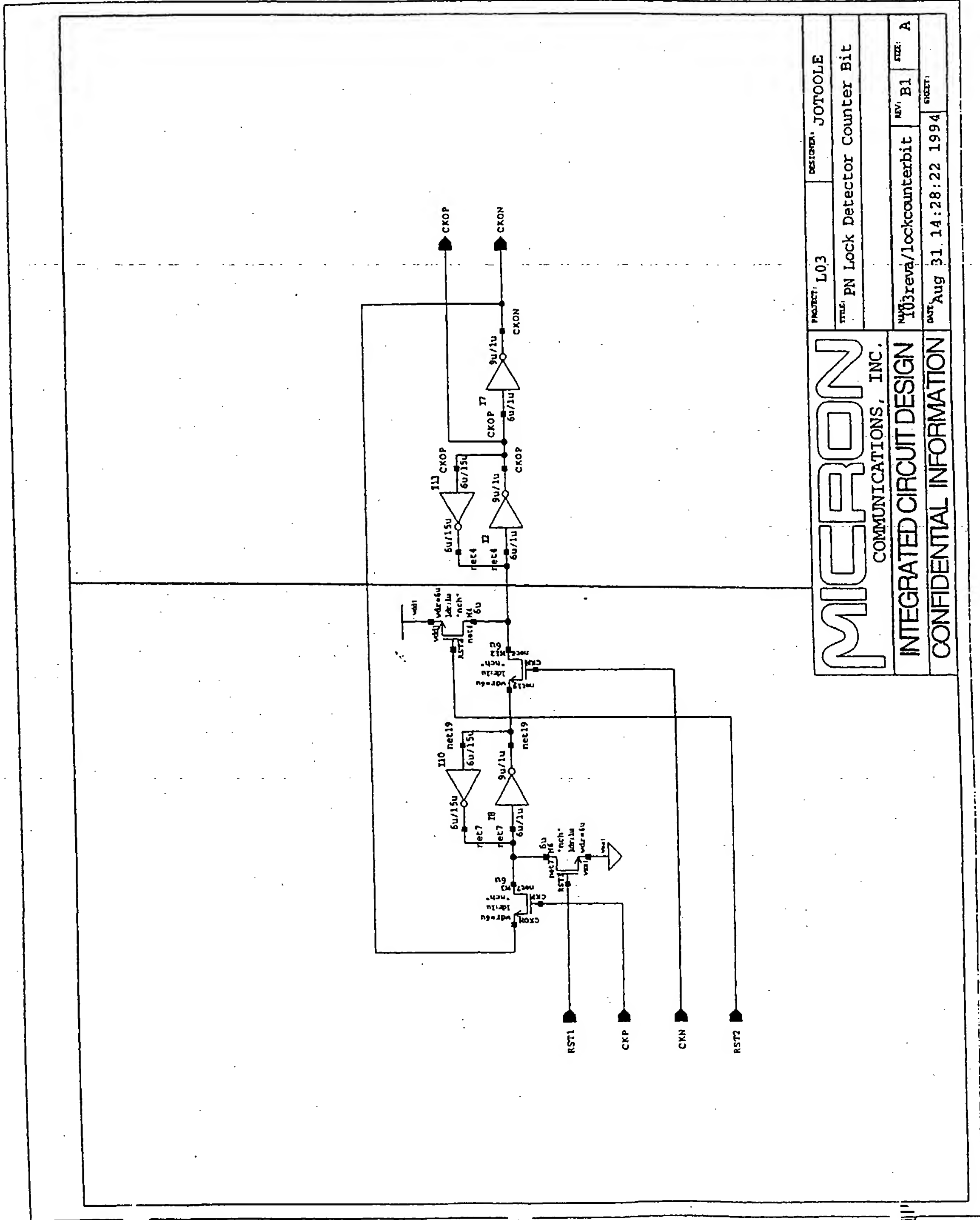
MICRON	
CORPORATIONS, INC.	
INTEGRATED CIRCUIT DESIGN	
CONFIDENTIAL INFORMATION	
DATE: 11/11/79	BY: [Signature]
TIME: 10:00 AM	LOCATION: [Signature]
PROJECT: [Signature]	DATE: 11/11/79

4114 09 JUL 68 0440Z  
FM JCRC TO DIA  
INFO DIA : 14 JUL 68 0440Z

10.0201AA	10.0201AB
-----------	-----------

10.0201

FIG. 10.0201

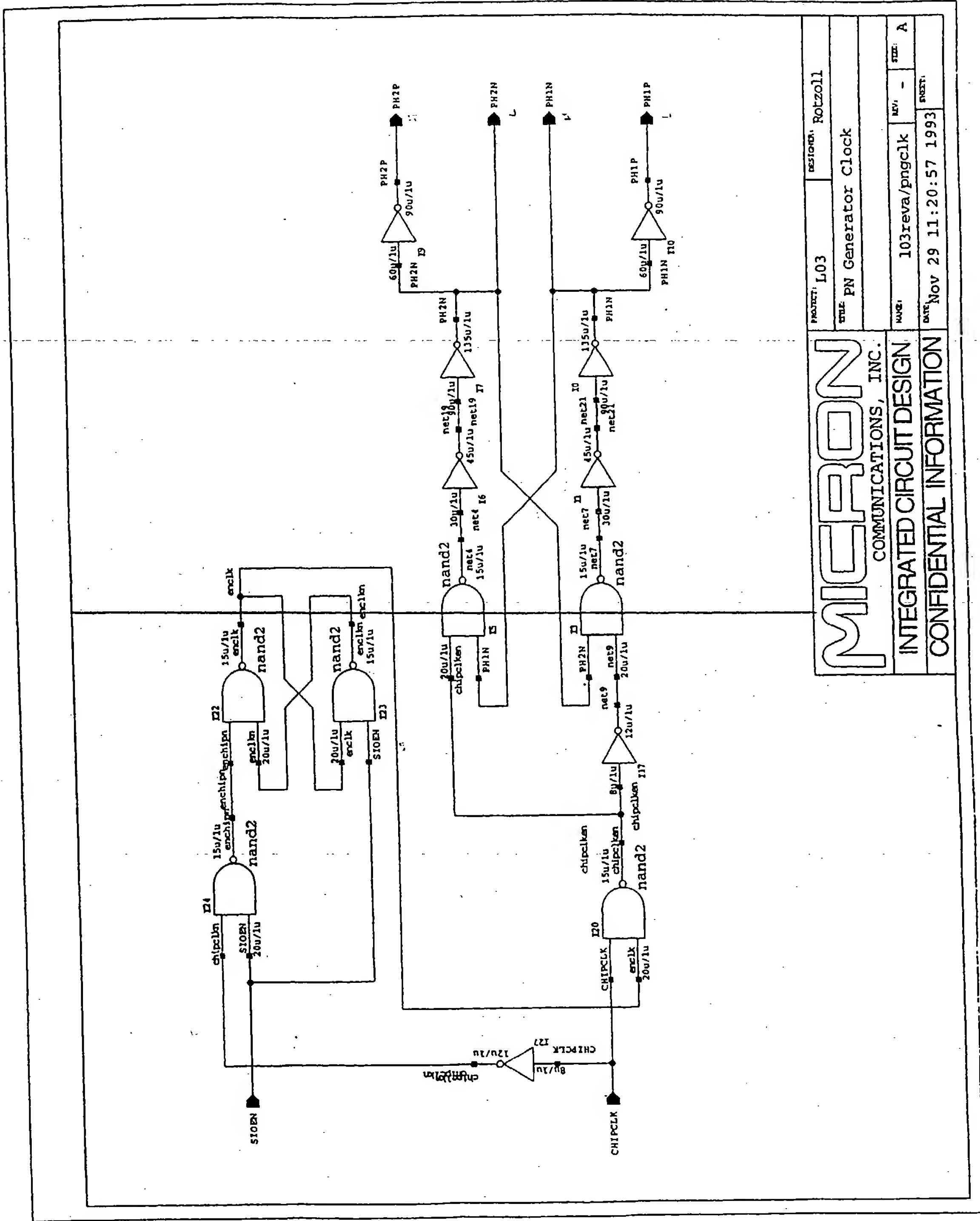


PROJECT: L03	DESIGNER: JOTOOLE
TITLE: PN Lock Detector Counter Bit	
PART: T03revA/lockcounterbit	
REV: B1	SIZE: A
DATE: Aug 31 14:28:22 1994	
SHEET: 1	

**MICRON**  
COMMUNICATIONS, INC.  
INTEGRATED CIRCUIT DESIGN  
CONFIDENTIAL INFORMATION

10.03AA	10.03AB
---------	---------

10.03



**MICRON**  
 COMMUNICATIONS, INC.  
 INTEGRATED CIRCUIT DESIGN  
 CONFIDENTIAL INFORMATION

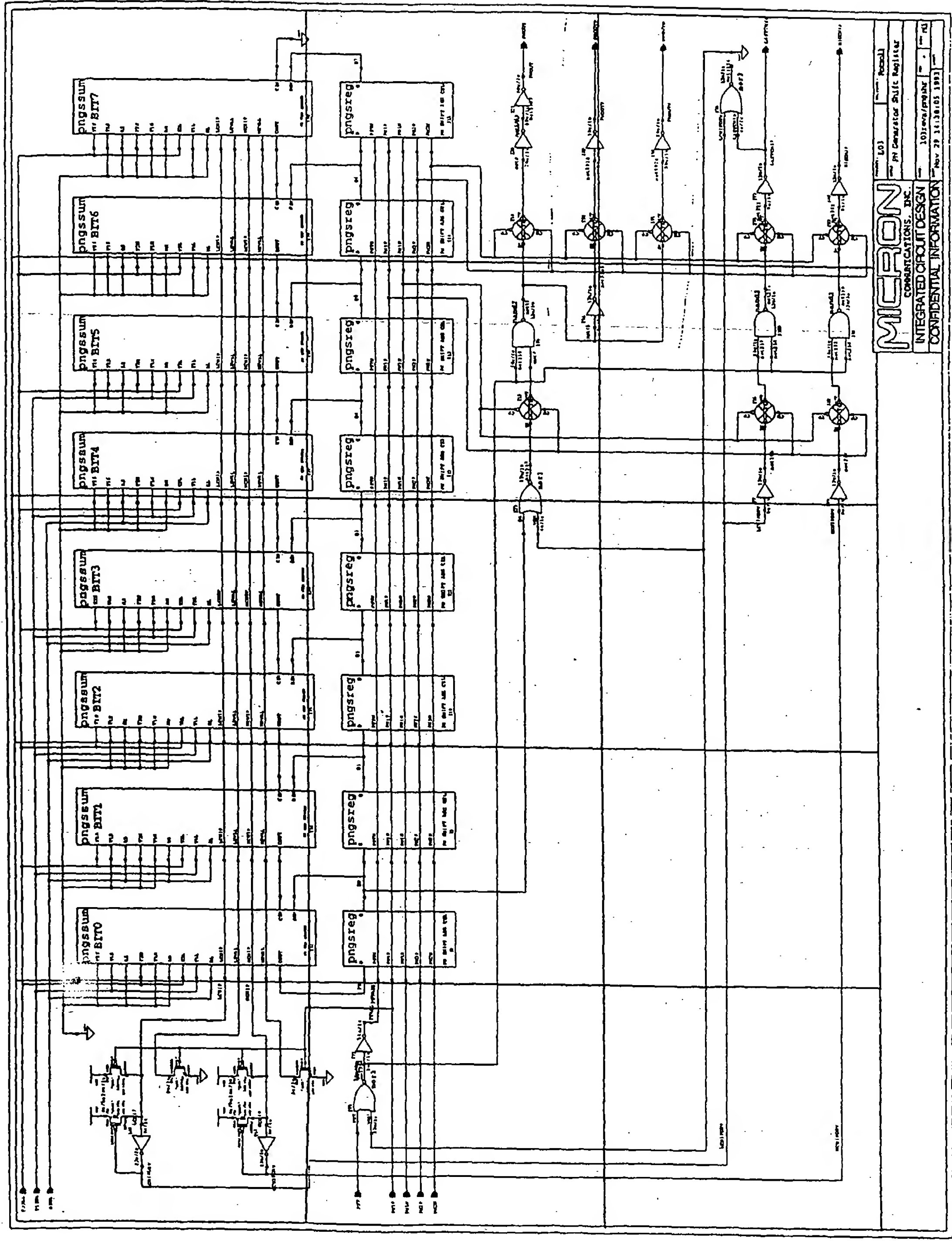
PROJECT: L03	DESIGNER: Rotzoll
FILE: PN Generator Clock	
NAME: 103reva/pngclk	REV: -
DATE: Nov 29 11:20:57 1993	SHEET: A

FIG. 10.03

10.04AA	10.04AB	10.04AC	10.04AD	10.04AE
10.04BA	10.04BB	10.04BC	10.04BD	10.04BE
10.04CA	10.04CB	10.04CC	10.04CD	10.04CE

II II II II II II II II

Fig. 10.04





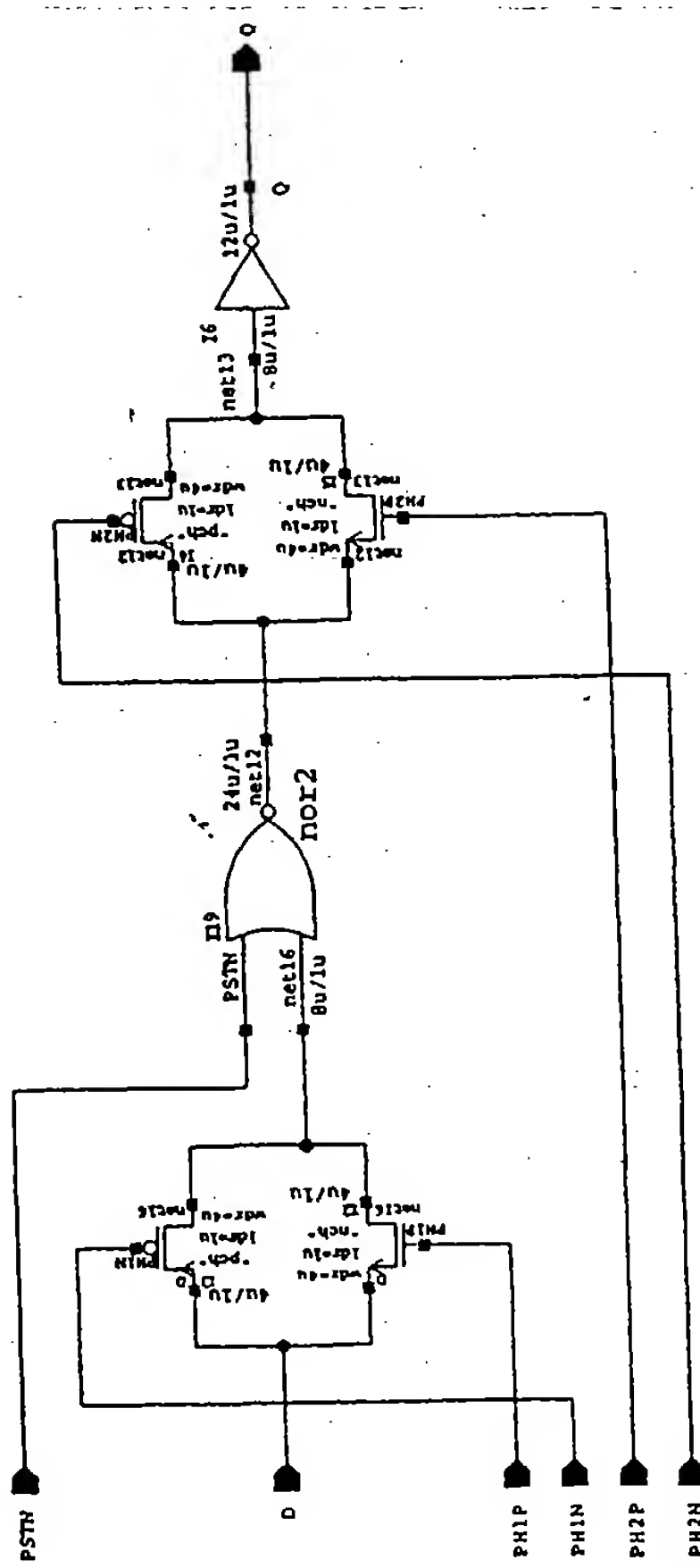
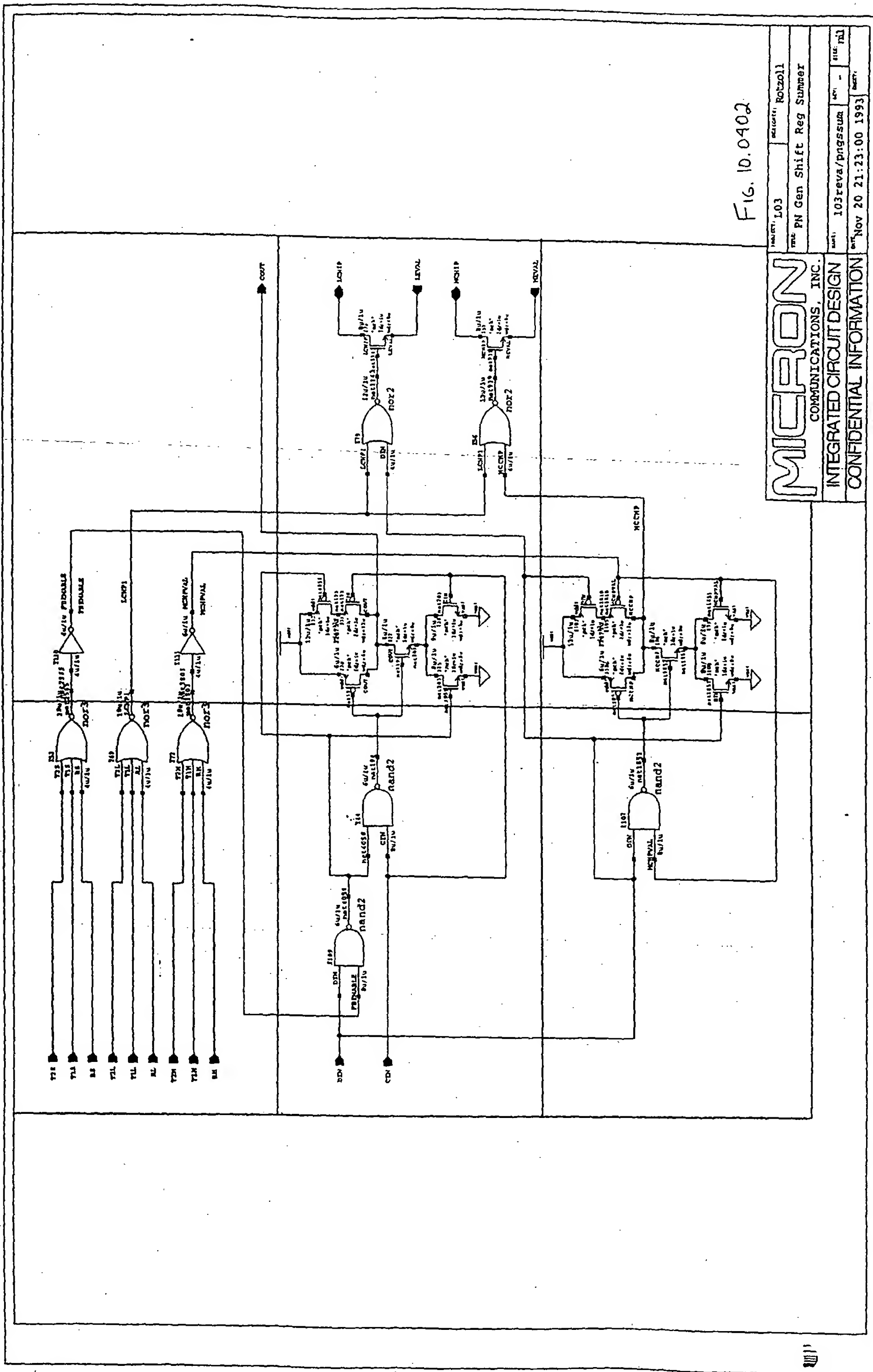


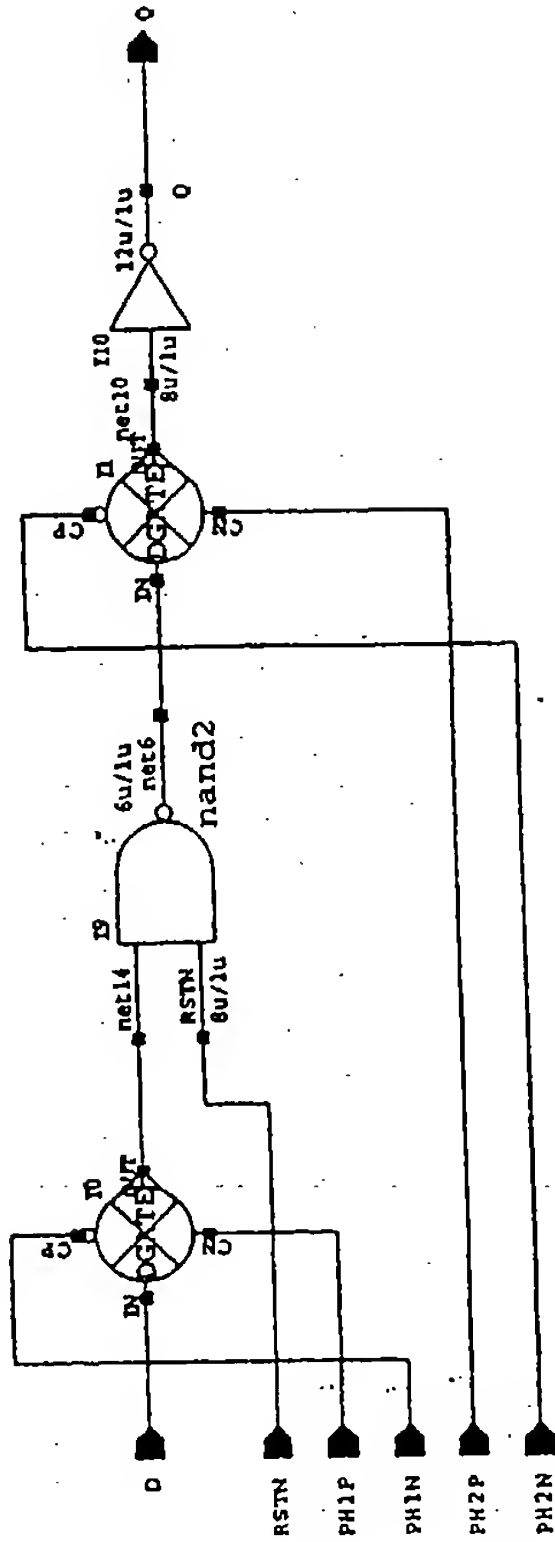
Fig. 10.0401

MICRON		DESIGNER: Rotzoll	
COMMUNICATIONS, INC.		TITLE: PN Generator Shift Register Cell	
INTEGRATED CIRCUIT DESIGN		NAME: 103reva/pngsreg	REV: -
CONFIDENTIAL INFORMATION		SIZE: A	
		DATE: Nov 20 21:22:37 1993	
		SHEET: 1	

**MICRON**  
 COMMUNICATIONS, INC.  
 INTEGRATED CIRCUIT DESIGN  
 CONFIDENTIAL INFORMATION







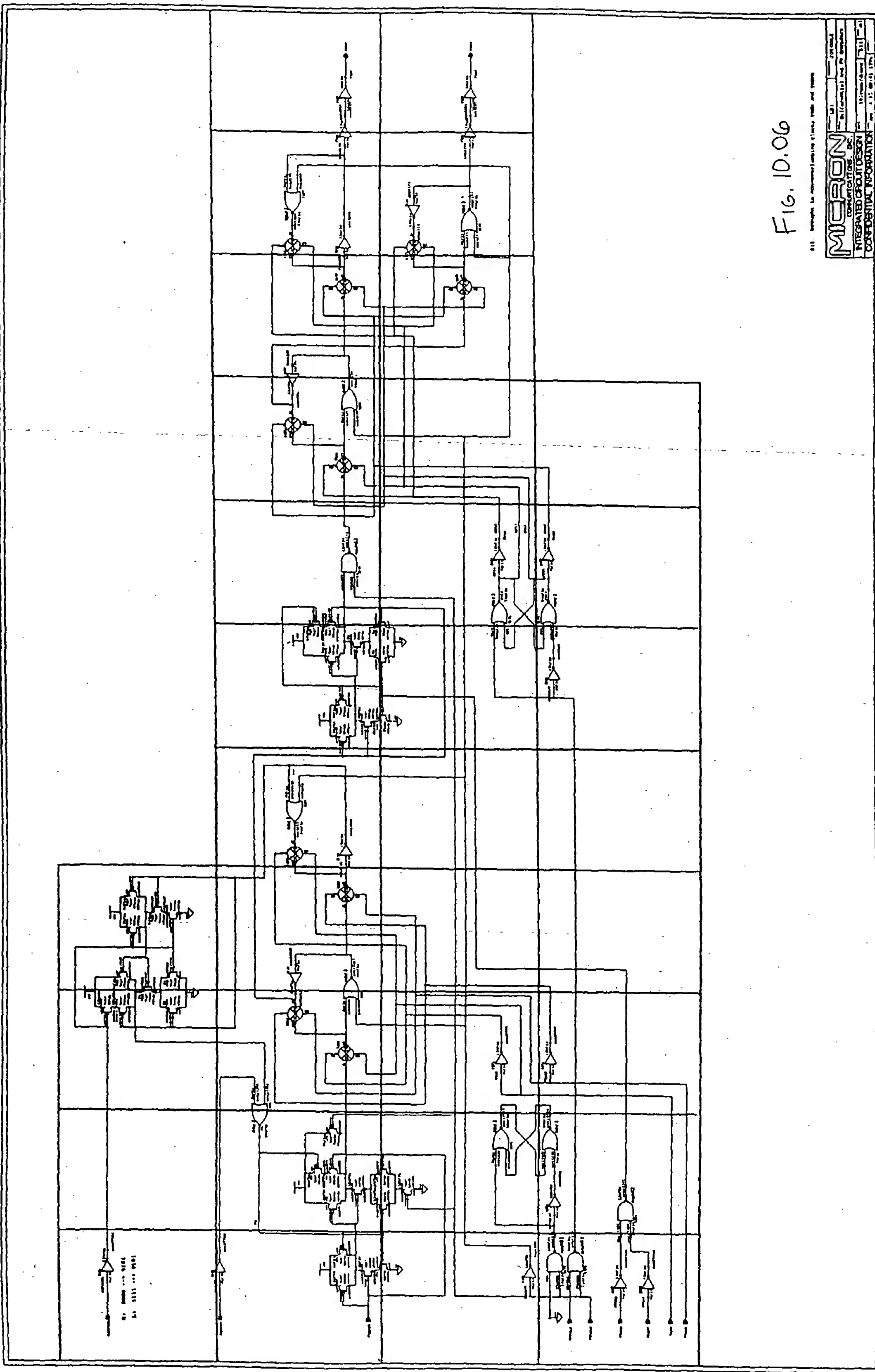
MICRON		PROJECT: L03		DESIGNER: Rotzoll	
COMMUNICATIONS, INC.		TITLE: PN Controller D Flip-Flop			
INTEGRATED CIRCUIT DESIGN		NAME: 103reva/pnddff		REV: -	SIZE: A
CONFIDENTIAL INFORMATION		DATE: Nov 26 18:12:59 1993		SHEET: 1	

**MICRON**  
 COMMUNICATIONS, INC.  
 INTEGRATED CIRCUIT DESIGN  
 CONFIDENTIAL INFORMATION

FIG. 10.05

10.06AA	10.06AB	10.06AC	10.06AD									
10.06BA	10.06BB	10.06BC	10.06BD	10.06BE	10.06BF	10.06BG	10.06BH	10.06BI	10.06BJ	10.06BK		
10.06CA	10.06CB	10.06CC	10.06CD	10.06CE	10.06CF	10.06CG	10.06CH	10.06CI	10.06CJ	10.06CK		
10.06DA	10.06DB	10.06DC	10.06DD	10.06DE	10.06DF	10.06DG	10.06DH					

II II III IIII



10.07AA	10.07AB	10.07AC	10.07AD
10.07BA	10.07BB	10.07BC	10.07BD
10.07CA	10.07CB	10.07CC	10.07CD

II II II II II

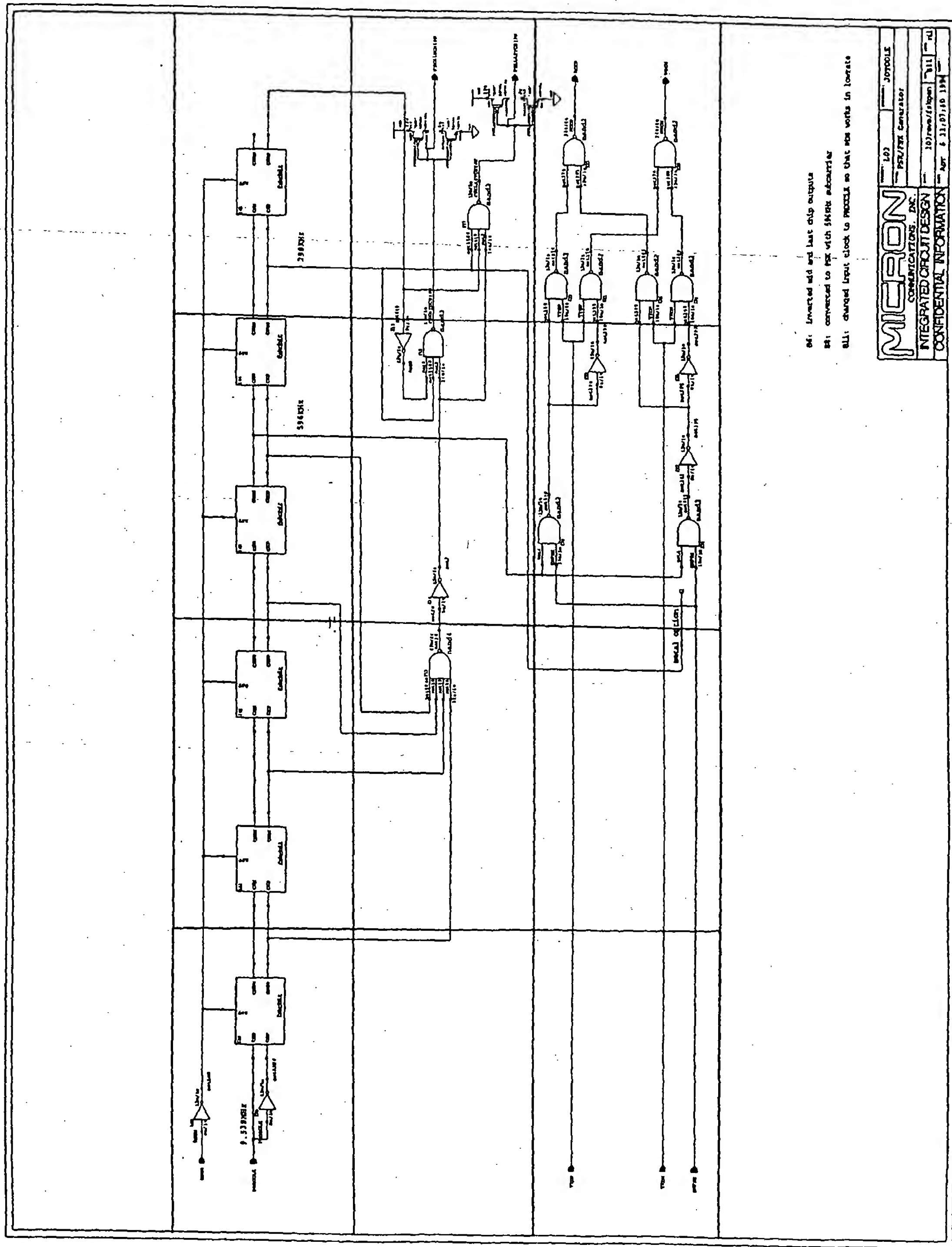
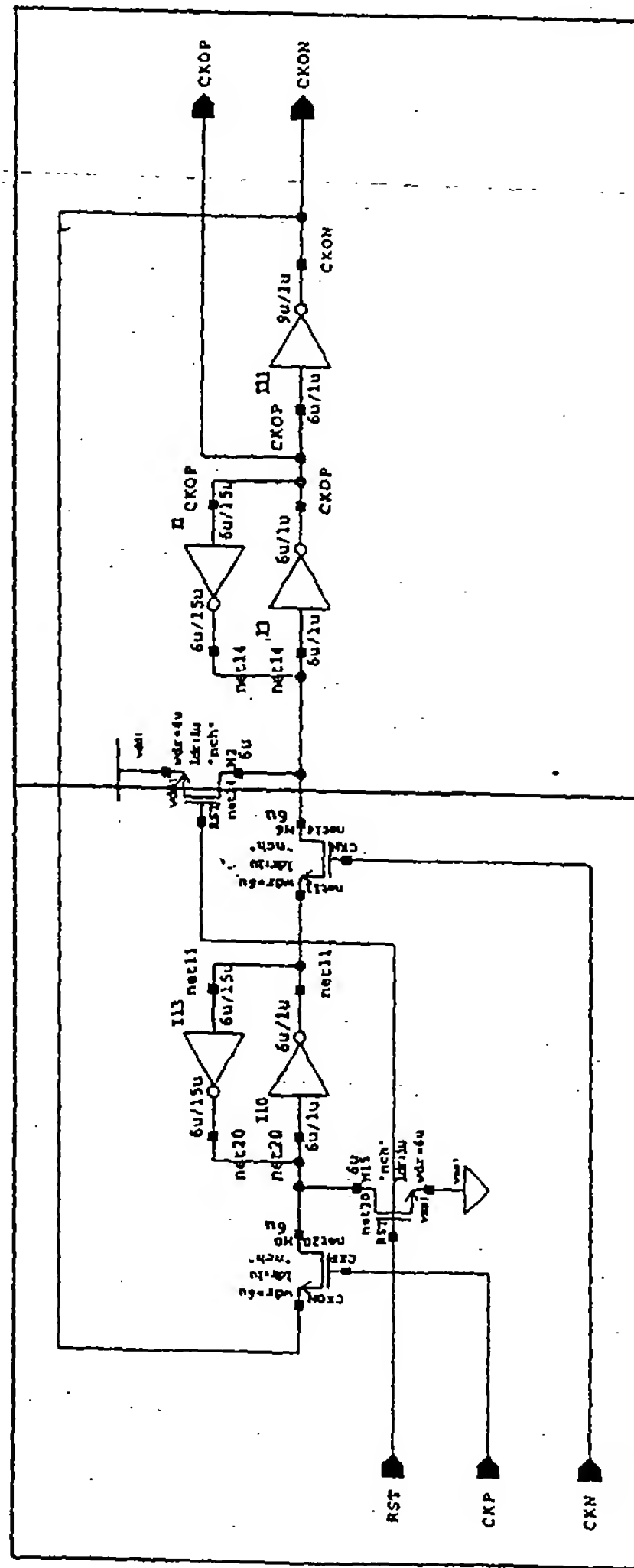


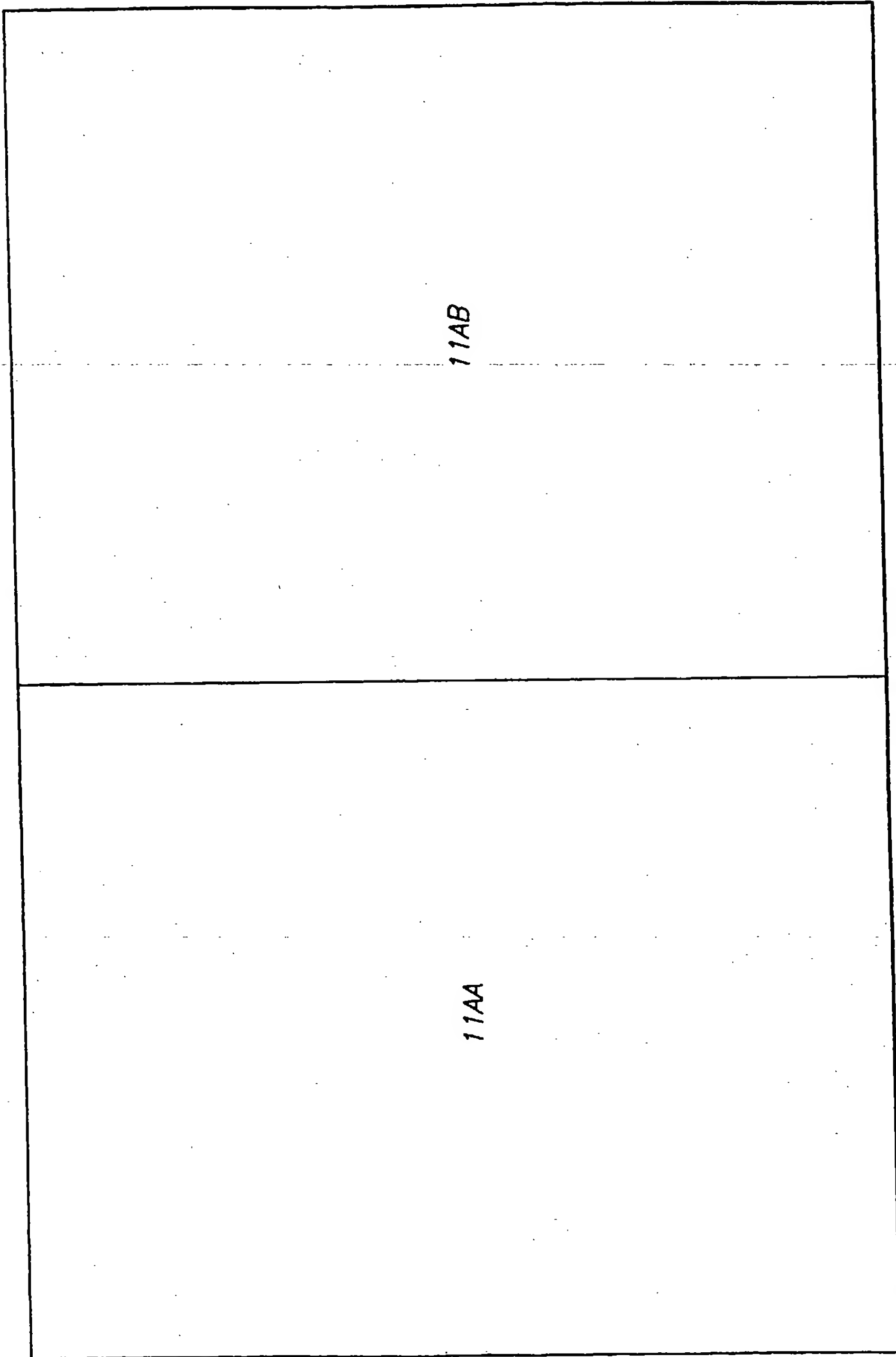




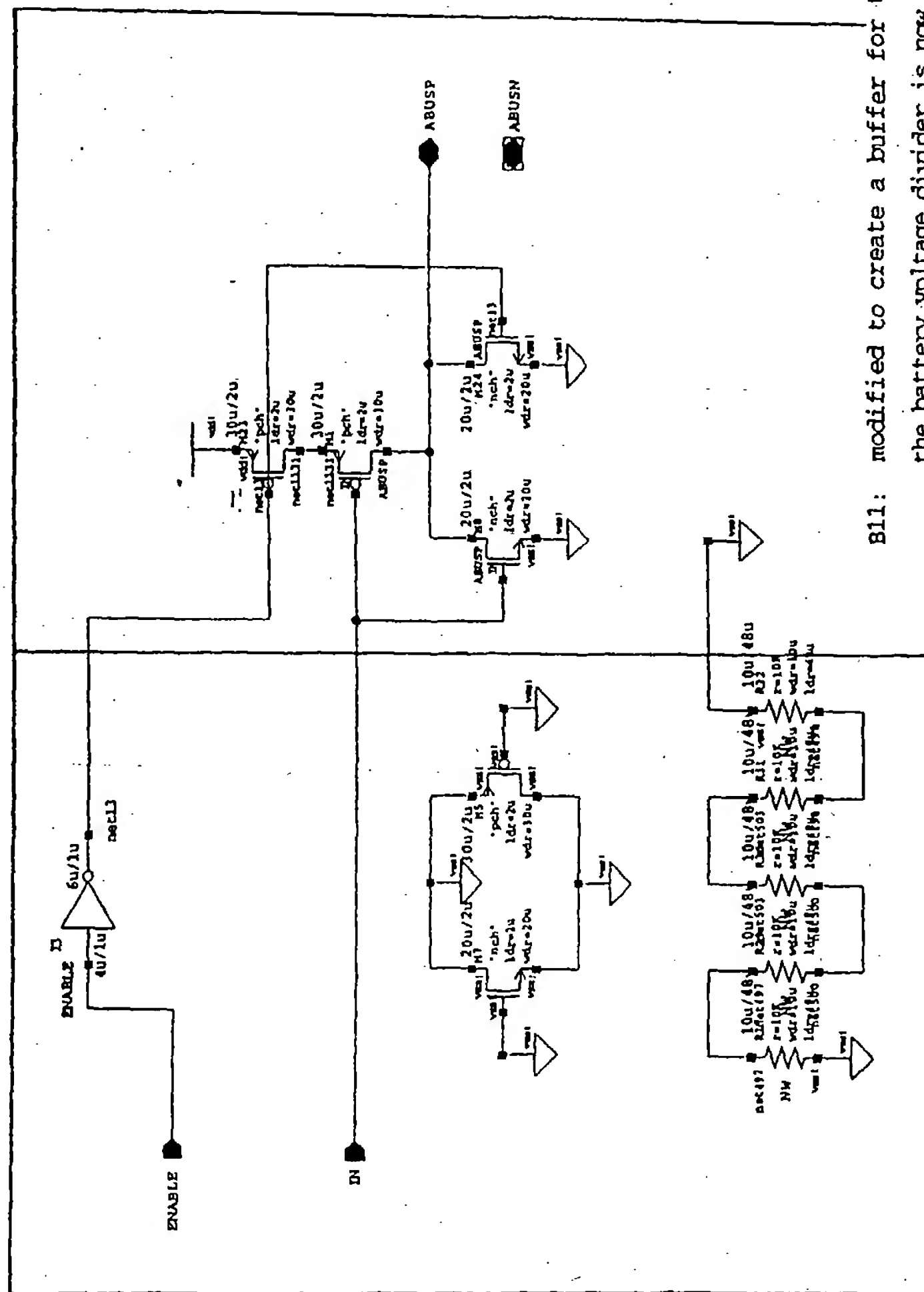
FIG. 10.0701



<b>MICROON</b>		PROJECT: L03	DESIGNER: JOTOOLE
COMMUNICATIONS, INC.		TITLE: FSK Counter Bit	
INTEGRATED CIRCUIT DESIGN		Same as wuabot_cbit	
CONFIDENTIAL INFORMATION		NAME: 103reva/fskcbit	REV: B1
		DATE: Apr 17 15:42:44 1995	SIZE: A



11 11



# NOFEL

COMMUNICATIONS, INC.

# INTEGRATED CIRCUIT DESIGN

**CONFIDENTIAL INFORMATION**

PROJECT: L03	DESIGNER: JOTOOLE
--------------	-------------------

DESIGNER: JOTOOLE

Battery Analog I/O Buffer

NUMERO:	103 reva/batalg	REV:	B11	SIZE:	A
---------	-----------------	------	-----	-------	---

B11	Ref: A
-----	--------

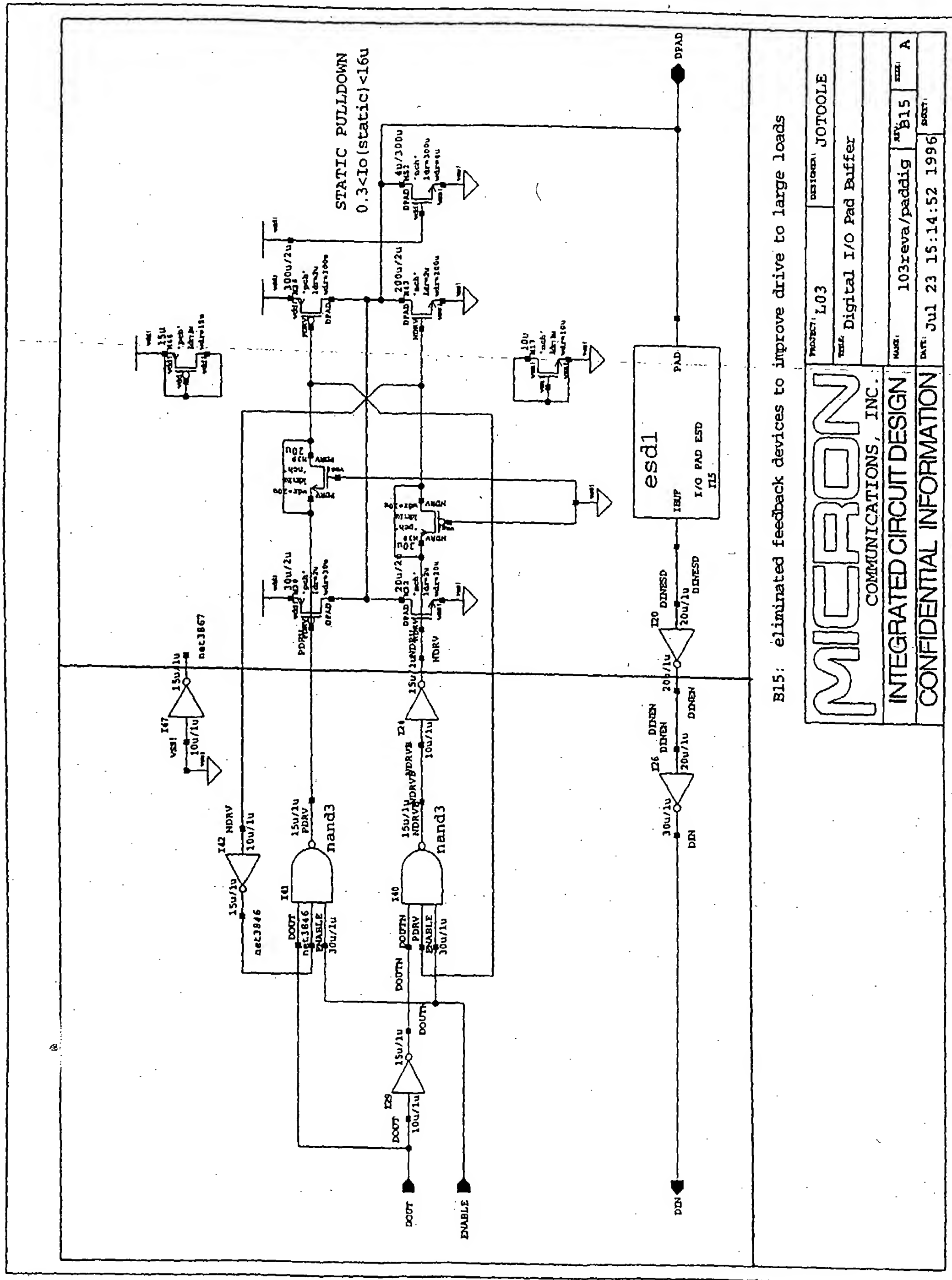
A	
---	--

DATE: APR 8 10:19:56 1996	SORT:
---------------------------	-------

1205

12AA	12AB
------	------

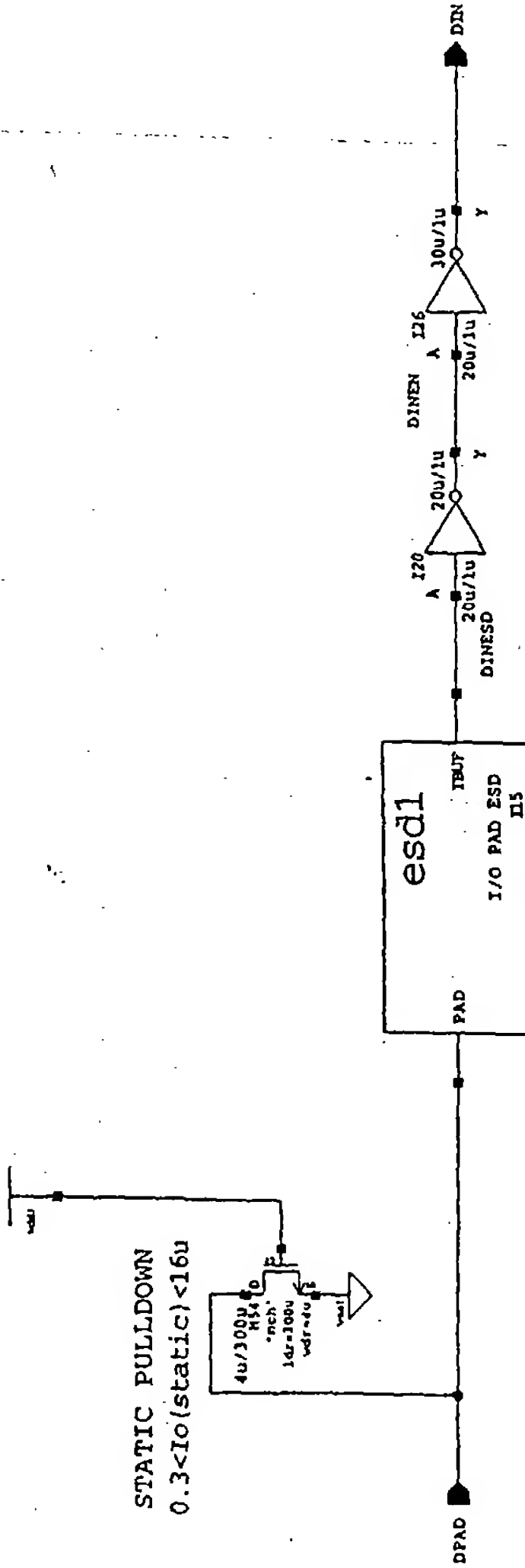
11-11-11



B15: eliminated feedback devices to improve drive to large loads

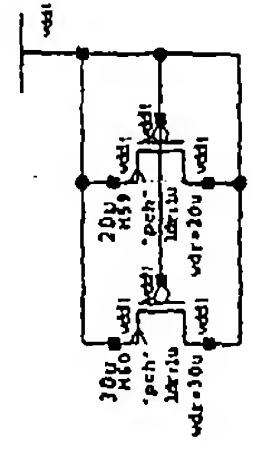
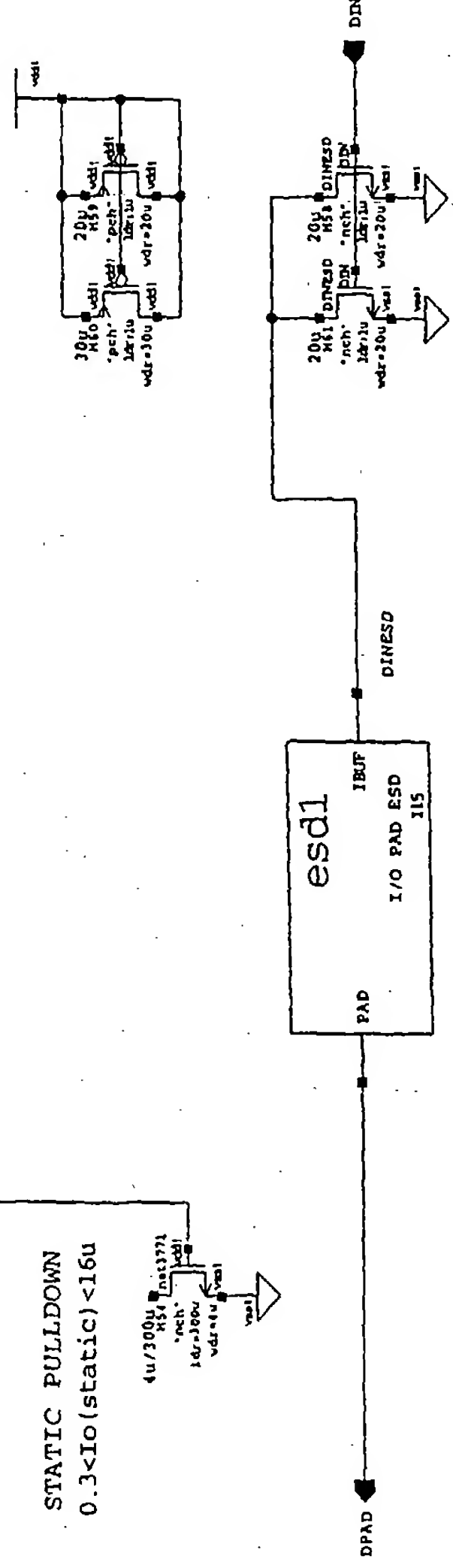
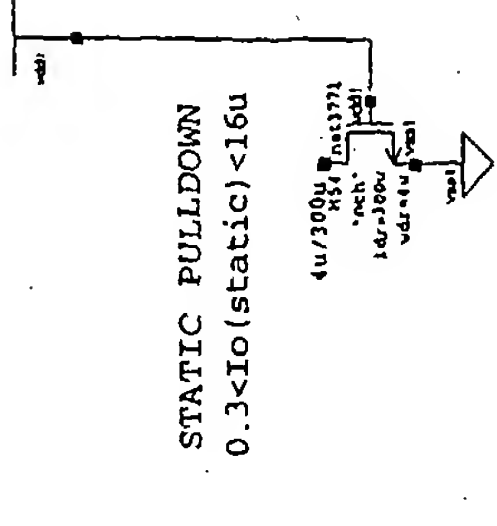
MICRON		PROJECT: L03	DESIGNER: JOTOOLE
COMMUNICATIONS, INC.		TITLE: Digital I/O Pad Buffer	
INTEGRATED CIRCUIT DESIGN		MADE: 103reva/paddig	REV: B15
CONFIDENTIAL INFORMATION		DATE: Jul 23 15:14:52 1996	PAGE: A

Fig 12AA-AB



<b>MICRON</b>		PROJECT: L03	DESIGNER: JOTOOLE
COMMUNICATIONS, INC.		TITLE: Digital Input Pad Buffer	
INTEGRATED CIRCUIT DESIGN		NAME: 103reva/paddigin	REV: B1
CONFIDENTIAL INFORMATION		DATE: Apr 11 11:10:35 1995	SIZE: A

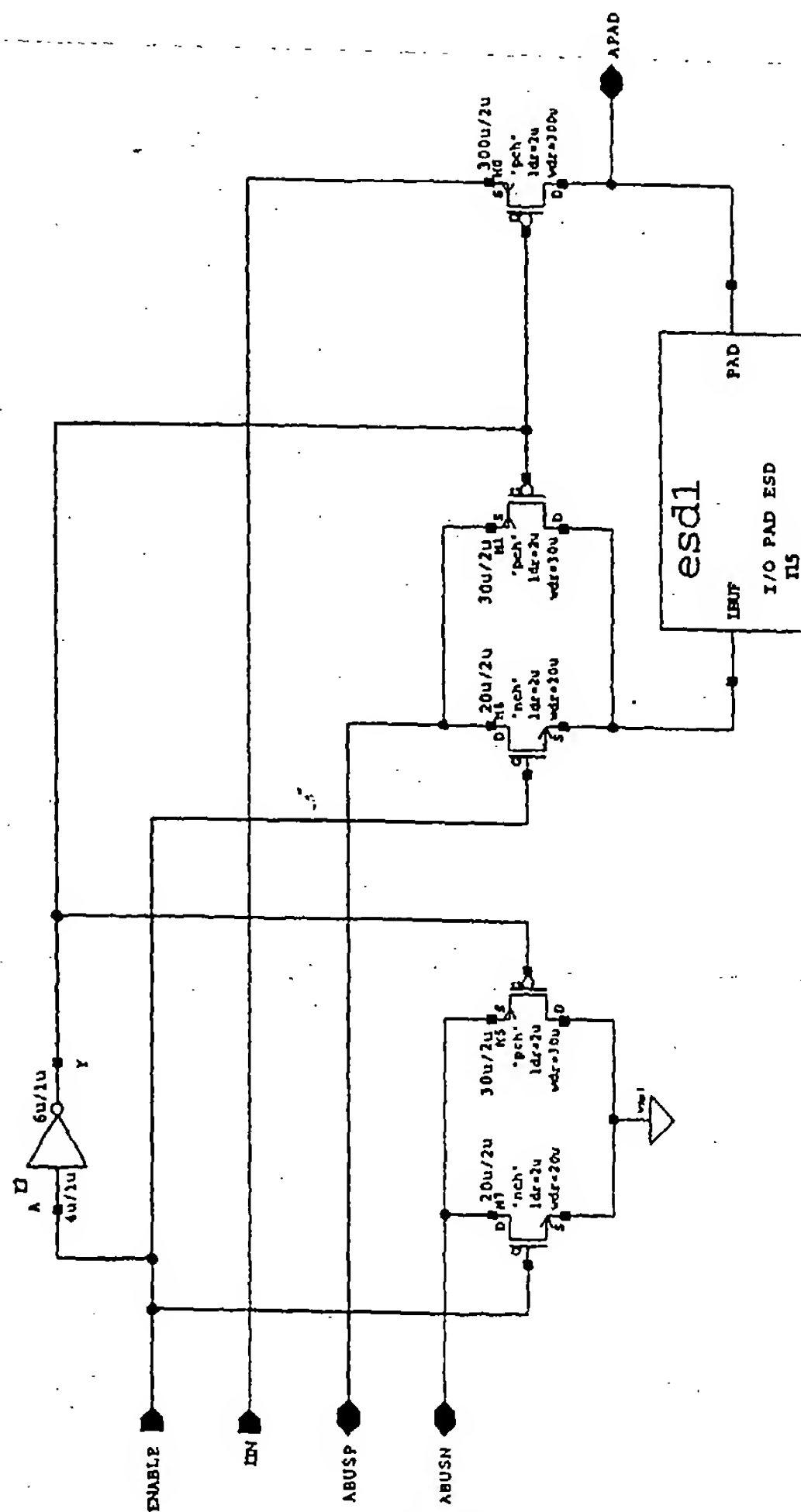
FIG. 13



MICRON		PROJECT: L03	DESIGNER: JOTOOLE
COMMUNICATIONS, INC.		TITLE: Digital Input Pad Buffer	
INTEGRATED CIRCUIT DESIGN		NAME: 103reva/paddigin2	SHEET: A
CONFIDENTIAL INFORMATION		DATE: May 24 18:28:29 1996	SHEET: 1

B13: new cell for WAKEUP\* output





MICRON		PROJECT: L03	DESIGNER: Rotzoll
COMMUNICATIONS, INC.		TITLE: Analog I/O Pad Buffer	
INTEGRATED CIRCUIT DESIGN		NAME: 103reva/padalg	REV: -
CONFIDENTIAL INFORMATION		DATE: Dec 12 21:55:41 1993	SHEET: A

FIG. 14

15AA	15AB	15AC	15AD
	15BA	15BB	15BC

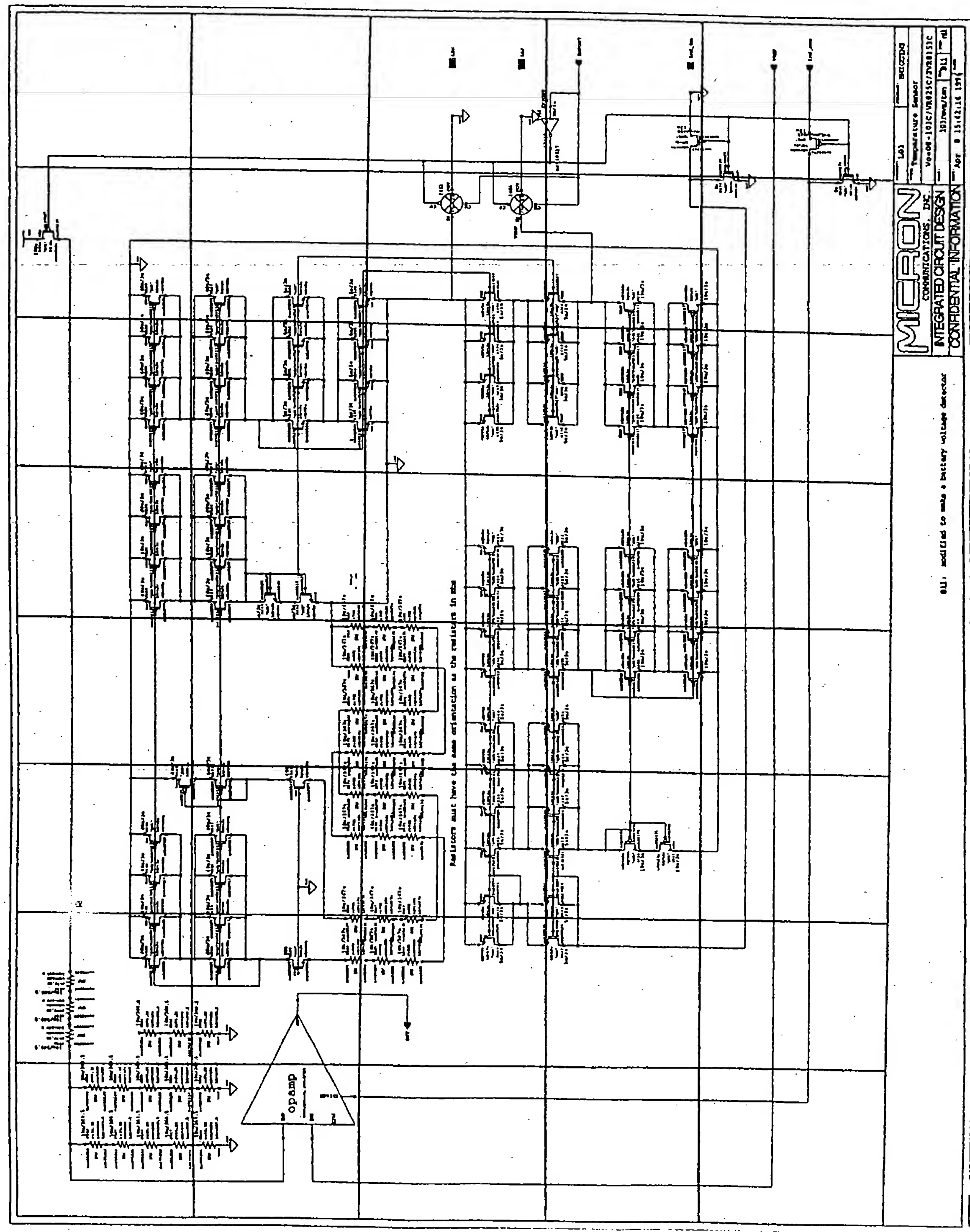
15



16AA	16AB	16AC	16AD	16AE	16AF	16AG	16AH
16BA	16BB	16BC	16BD	16BE	16BF	16BG	16BH
16CA	16CB	16CC	16CD	16CE	16CF	16CG	16CH
16DA	16DB	16DC	16DD	16DE	16DF	16DG	16DH
16EA	16EB	16EC	16ED	16EE	16EF	16EG	16EH

II 15

FIG. 16



**MICRON**  
COMMUNICATIONS, INC.  
INTEGRATED CIRCUIT DESIGN  
CONFIDENTIAL INFORMATION

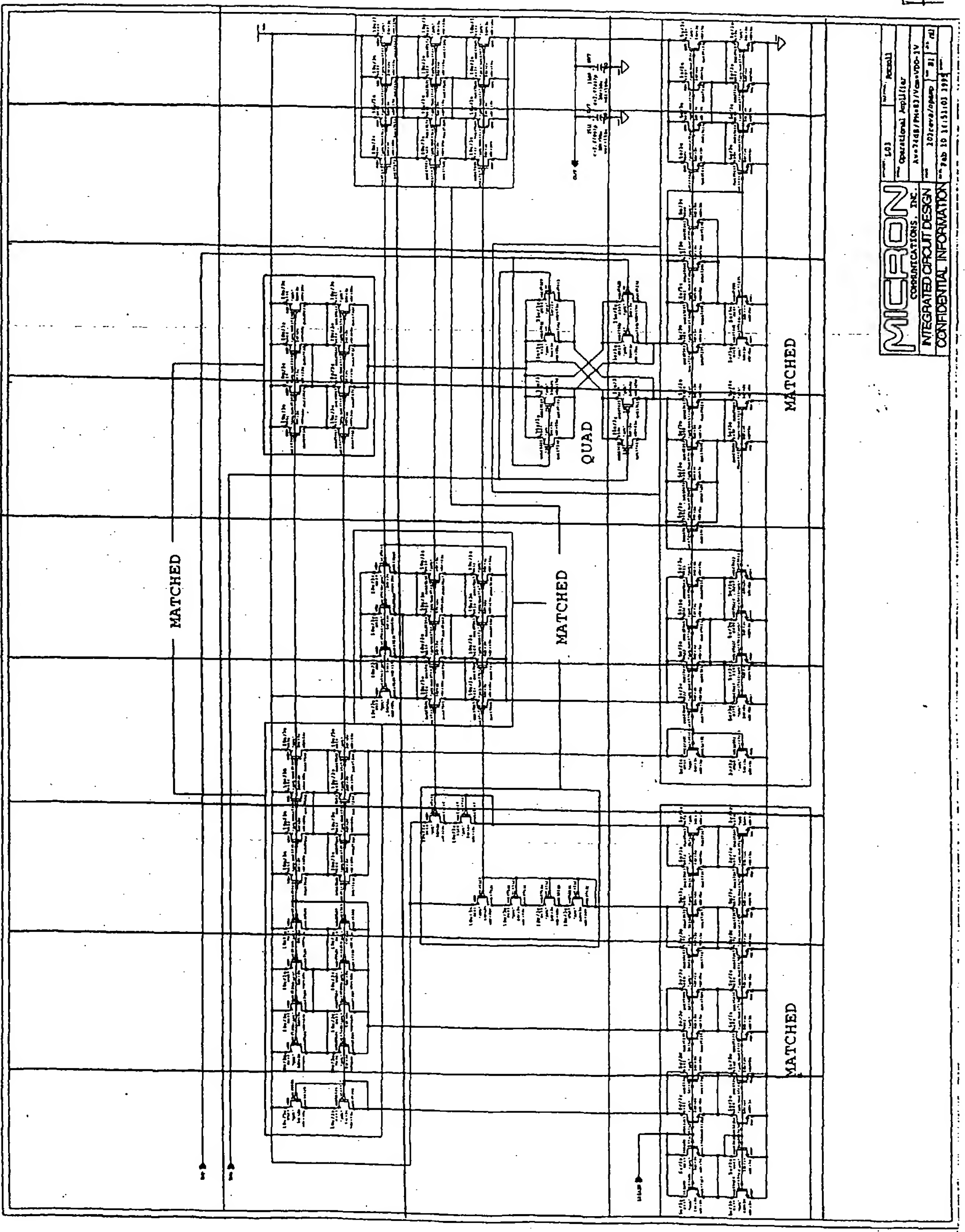
011, modified to make a battery voltage detector

101  
Temperature Sensor  
V0-08-101C/VN015C/2V0151C  
101me/tem  
111  
11  
Apr 8 13:42:16 1991

16.01AA	16.01AB	16.01AC	16.01AD	16.01AE	16.01AF	16.01AG	
16.01BA	16.01BB	16.01BC	16.01BD	16.01BE	16.01BF	16.01BG	16.01BH
16.01CA	16.01CB	16.01CC	16.01CD	16.01CE	16.01CF	16.01CG	16.01CH
16.01DA	16.01DB	16.01DC	16.01DD	16.01DE	16.01DF	16.01DG	16.01DH
							16.01DI
							16.01CI
							16.01BI

II II II II II II

FIG. 16.01



<b>MICRON</b>	Part No.	1601	Rev.	Rev. 11
	Operational Amplifier			
	Avx2148/Phx21/Verx100-1V			
	20 pins/0.050" pitch			
INTEGRATED CIRCUIT DESIGN		CONFIDENTIAL INFORMATION		
		Feb 10 11:51:01 1974		

17AB	17BB
17AA	17BA

IIII II





18AA	18AB
------	------

BB  
BB

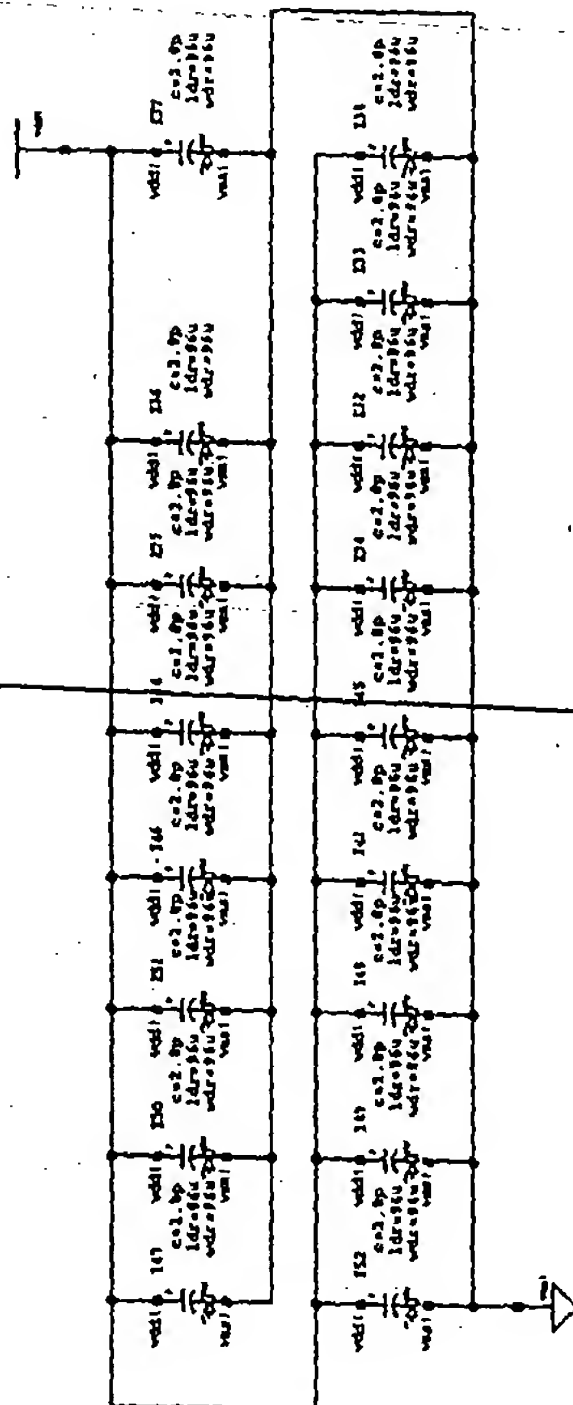


FIG. 18

<b>MICRON</b>		PRODUCT: L03	REVISION: J0000LE
COMMUNICATIONS, INC.		Title: Chip Bypass Capacitor	
INTEGRATED CIRCUIT DESIGN		Ct=pf	
CONFIDENTIAL INFORMATION		DATE: 103reva/bypcap3	REV: B2
		DATE: Jul 28 17:43:25 1995	DATE:

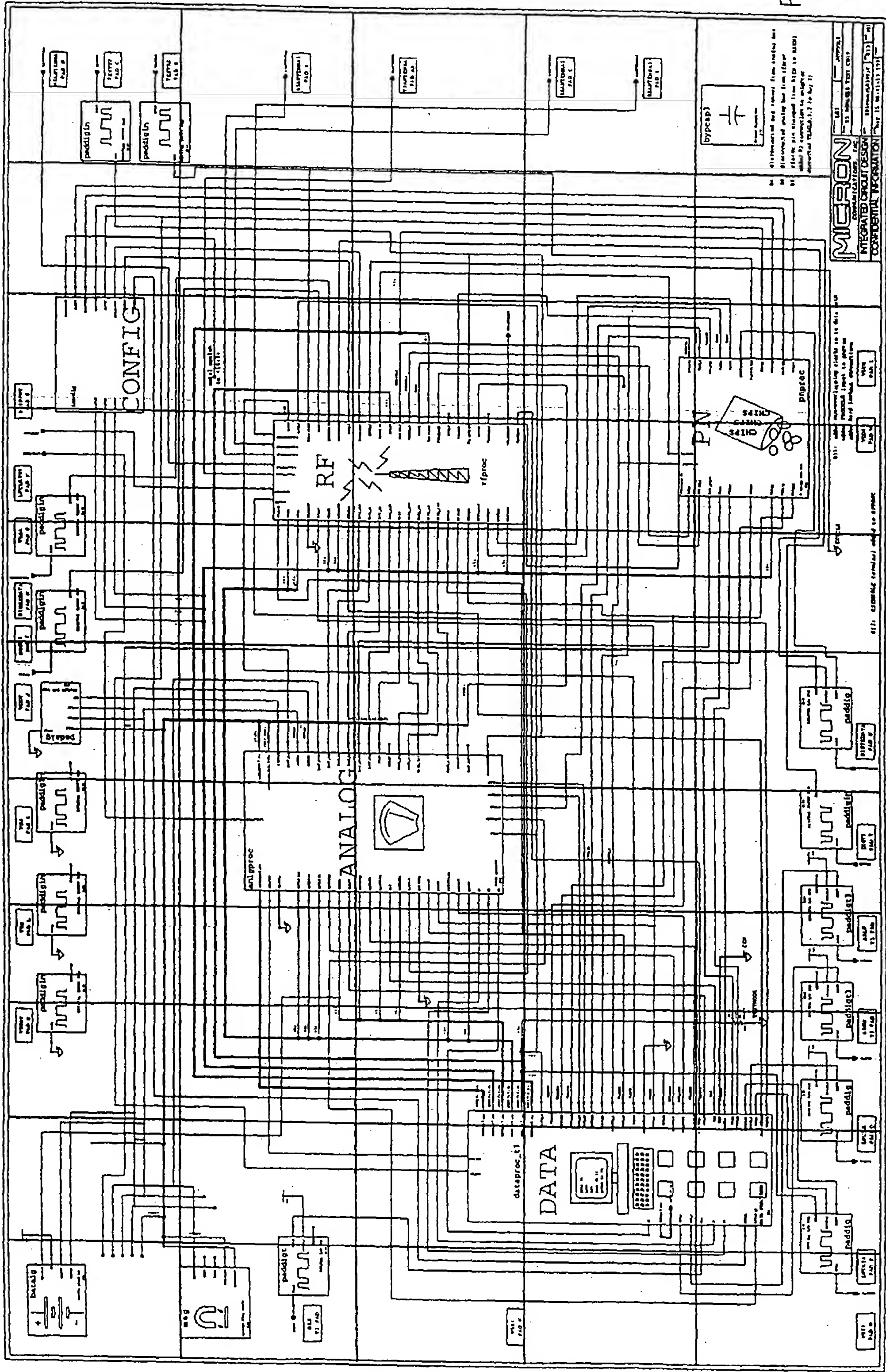
B2: deleted one cap

19AA	19AB	19AC	19AD	19AE	19AF	19AG	19AH	19AI	19AJ	19AK
19BA	19BB	19BC	19BD	19BE	19BF	19BG	19BH	19BI	19BJ	19BK
19CA	19CB	19CC	19CD	19CE	19CF	19CG	19CH	19CI	19CJ	19CK
19DA	19DB	19DC	19DD	19DE	19DF	19DG	19DH	19DI	19DJ	19DK
19EA	19EB	19EC	19ED	19EE	19EF	19EG	19EH	19EI	19EJ	19EK





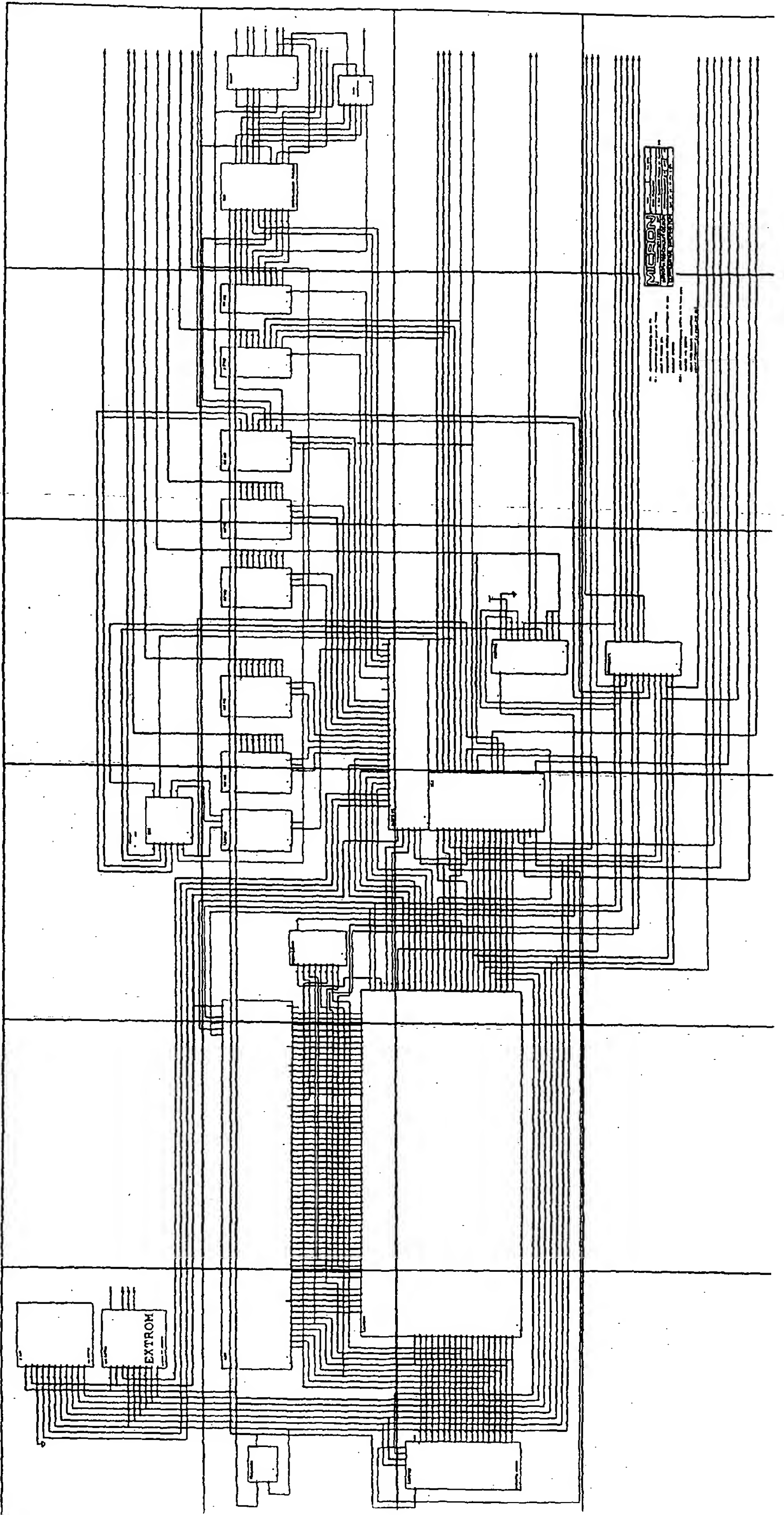
FIG. 19.AA-EK



20AA	20AB	20AC	20AD	20AE	20AF
20BA	20BB	20BC	20BD	20BE	20BF
20CA	20CB	20CC	20CD	20CE	20CF
		20DC	20DD	20DE	20DF

II II II II

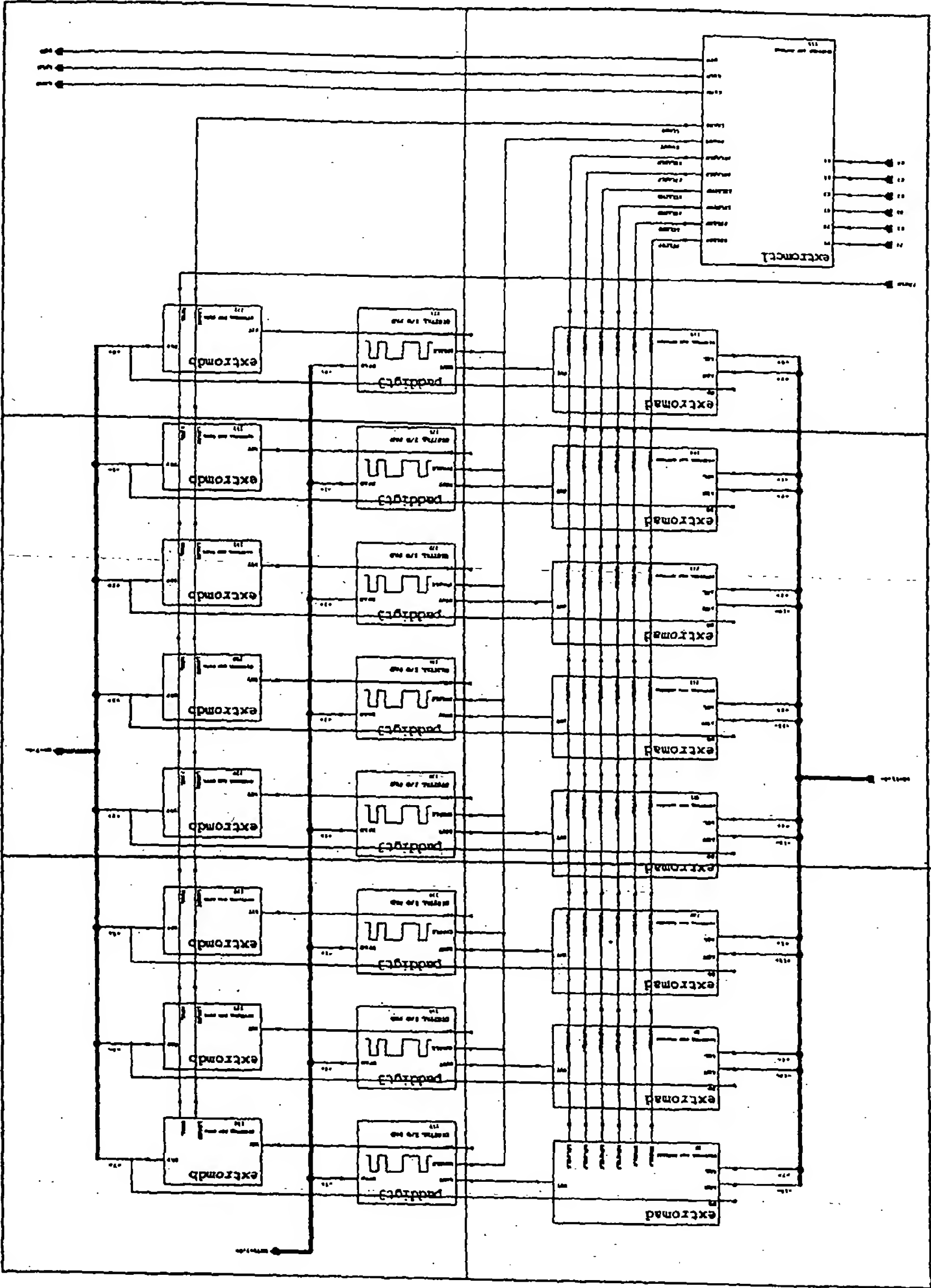
FIG. 20



20.01AA	20.01AB
20.01BA	20.01BB
20.01CA	20.01CB



FIG. 20.01



20.0101AA	20.0101AB
20.0101BA	20.0101BB

II II 20.0101 II

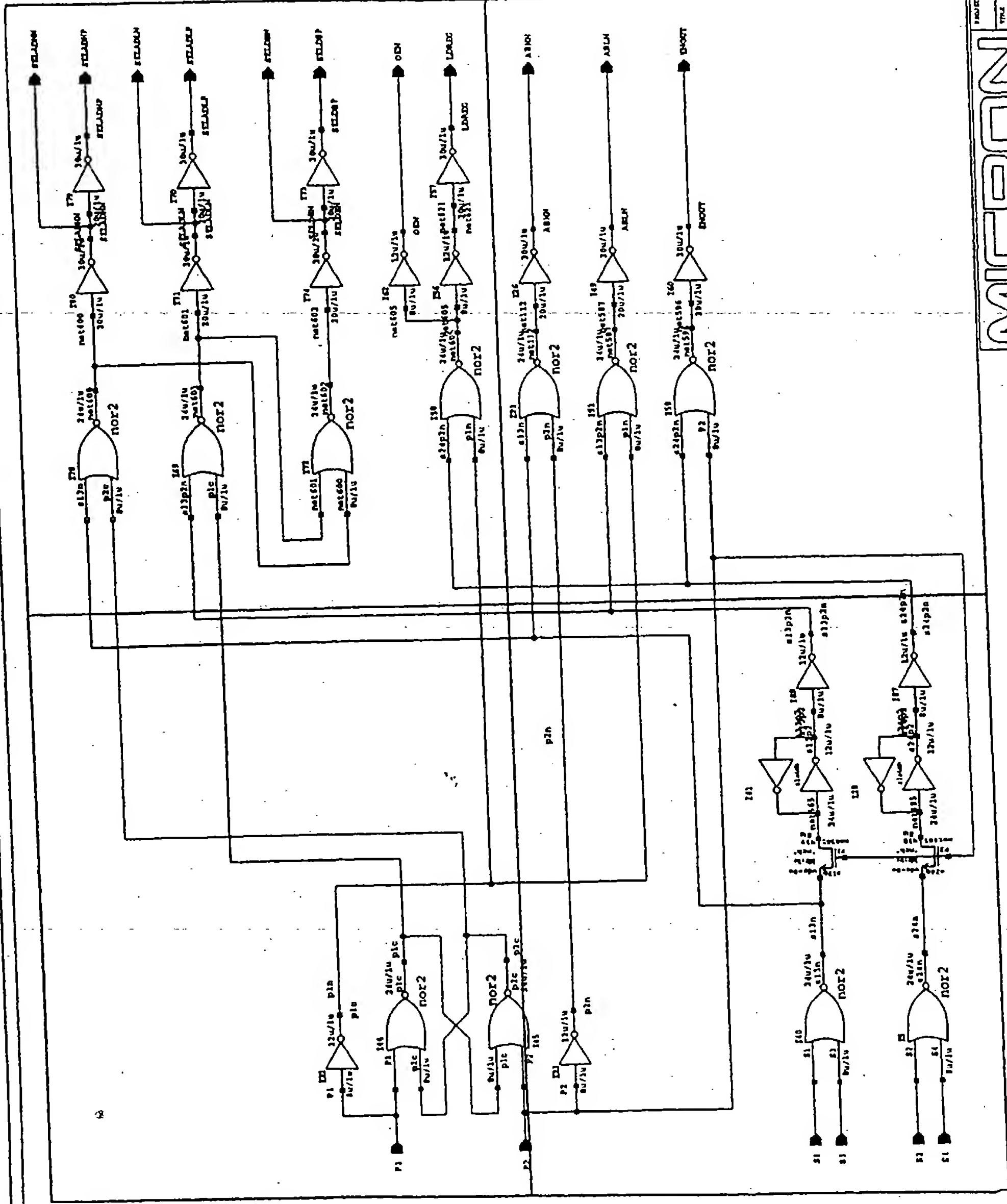


FIG. 20.0101

PROPERTY: L03		MILITARY: ROTZOLL	
TITLE: External ROM Control Logic		REV: -	
DATE: 103revs/extract1		REV: -	
DATE: Dec 11 21:56:41 1993		REV: -	
MILITARY: 103revs/extract1		REV: -	
DATE: Dec 11 21:56:41 1993		REV: -	

**MICRON**  
COMMUNICATIONS, INC.  
INTEGRATED CIRCUIT DESIGN  
CONFIDENTIAL INFORMATION

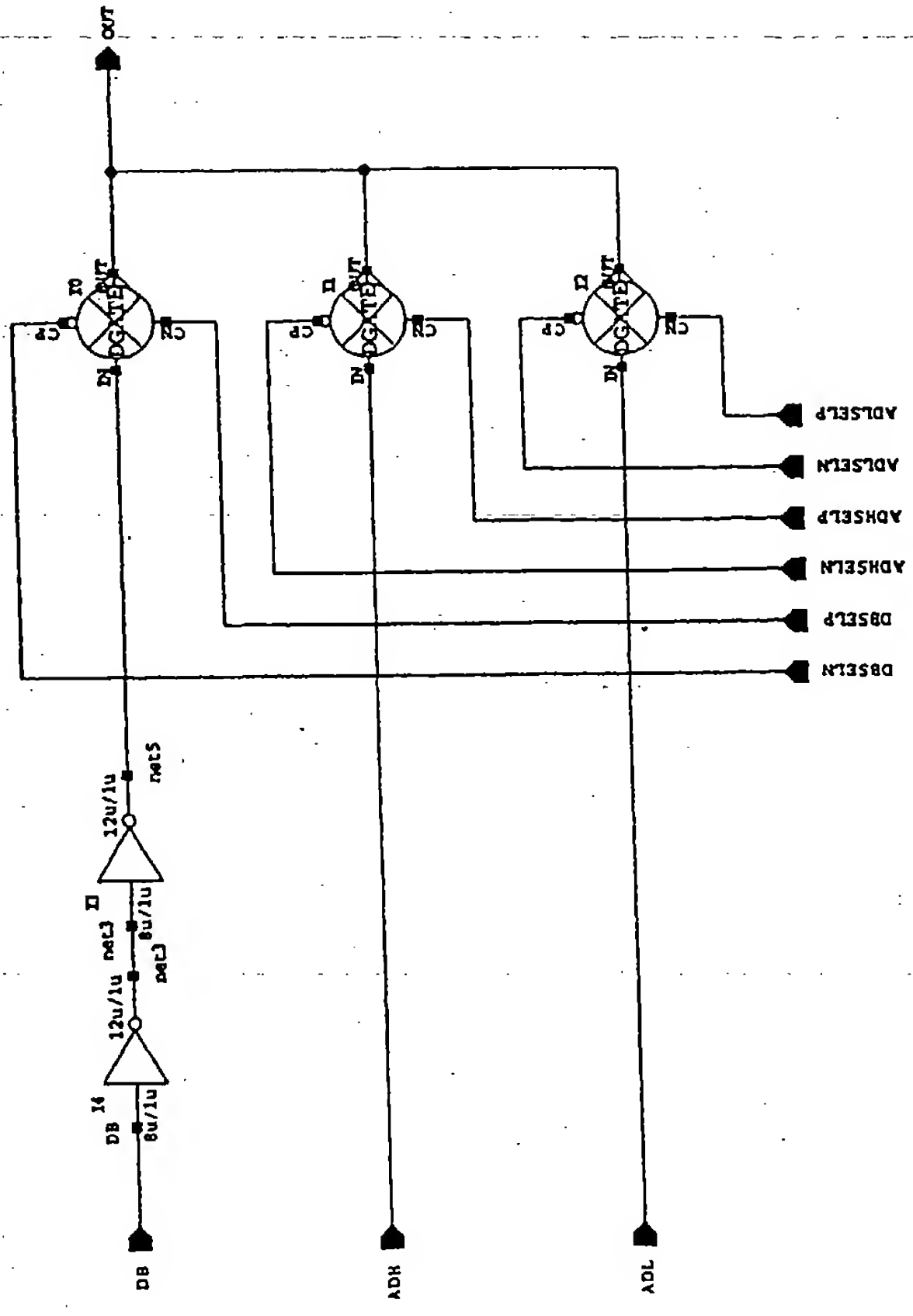


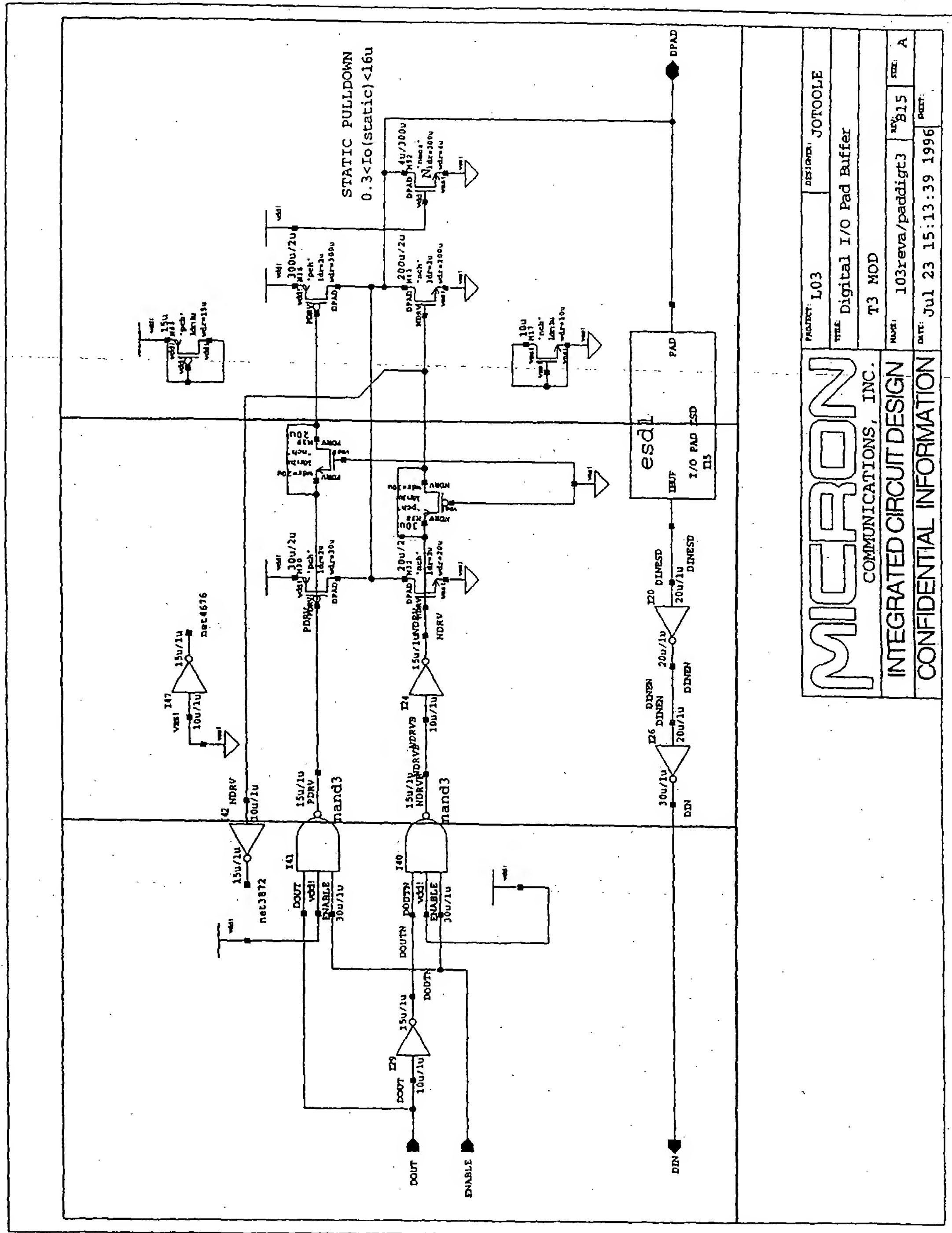
Fig. 20,0102

MICRON COMMUNICATIONS, INC.				PROJECT: L03		DESIGNER: Rotzoll	
INTEGRATED CIRCUIT DESIGN				TITLE: External ROM Address Interface			
CONFIDENTIAL INFORMATION				NAME: 103reva/extromad		REV: -	SIZE: A
				DATE: Dec 11 01:09:14 1993		SHEET: 1	

**MICRON**  
COMMUNICATIONS, INC.  
INTEGRATED CIRCUIT DESIGN  
CONFIDENTIAL INFORMATION

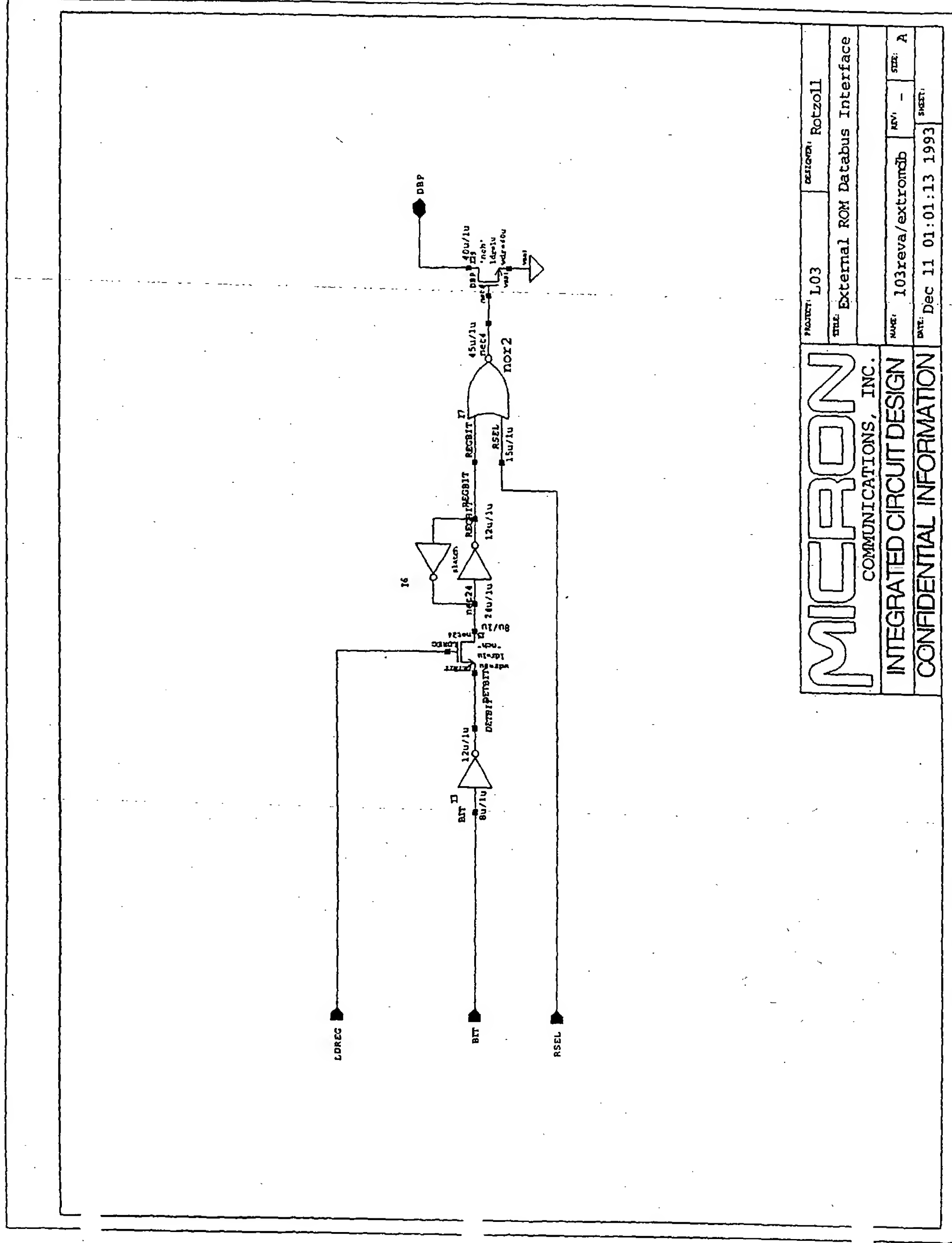
20.0103AA	20.0103AB	20.0103AC
-----------	-----------	-----------

20.0103



K19 20.0103AA-AC

FIG. 20.0104



PROJECT: L03		DESIGNER: Rotzoll	
TITLE: External ROM Databus Interface			
NAME: 103reva/extromdb		REV: -	SHEET: A
DATE: Dec 11 01:01:13 1993		SHEET:	

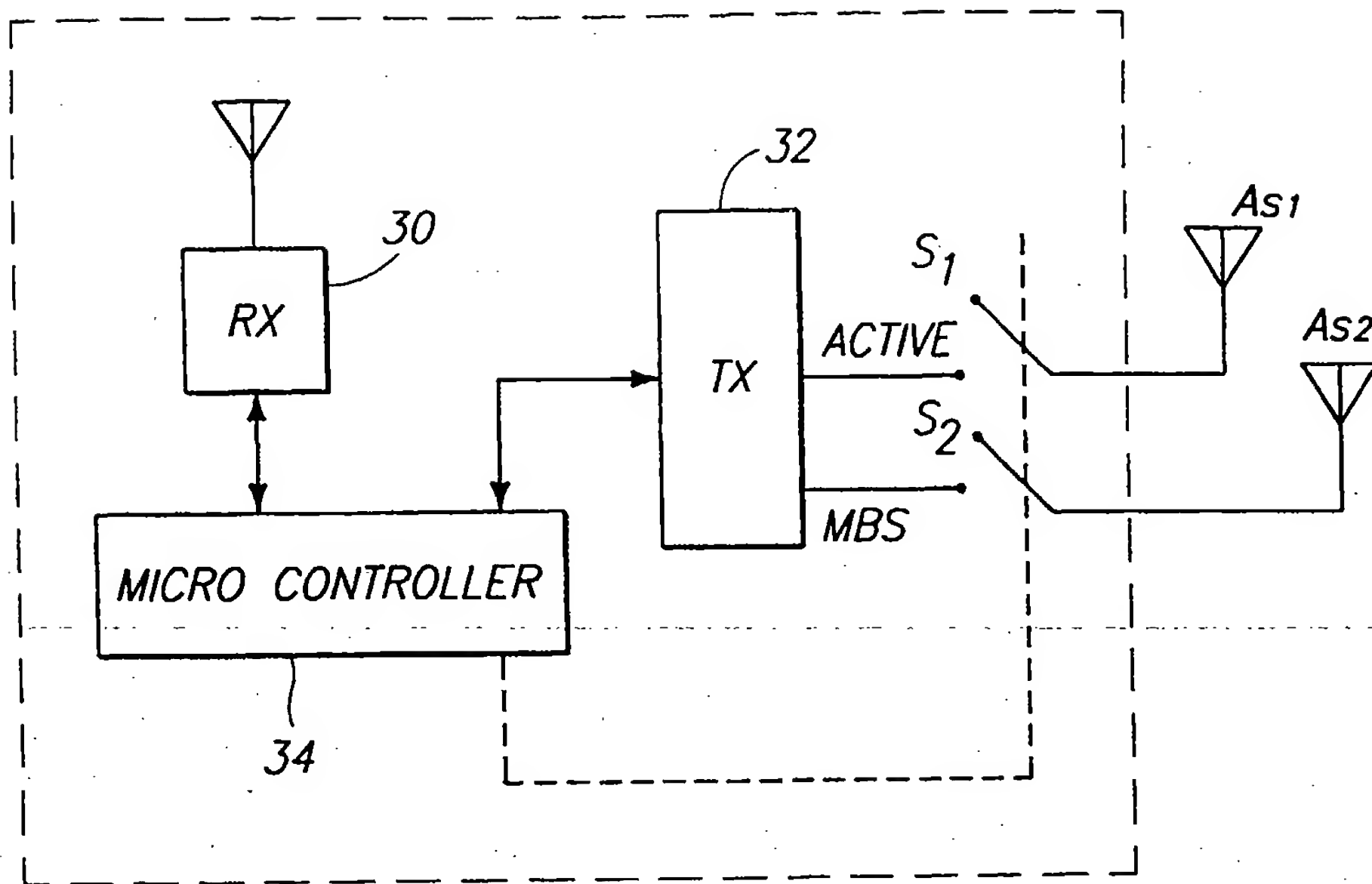


FIG. 2

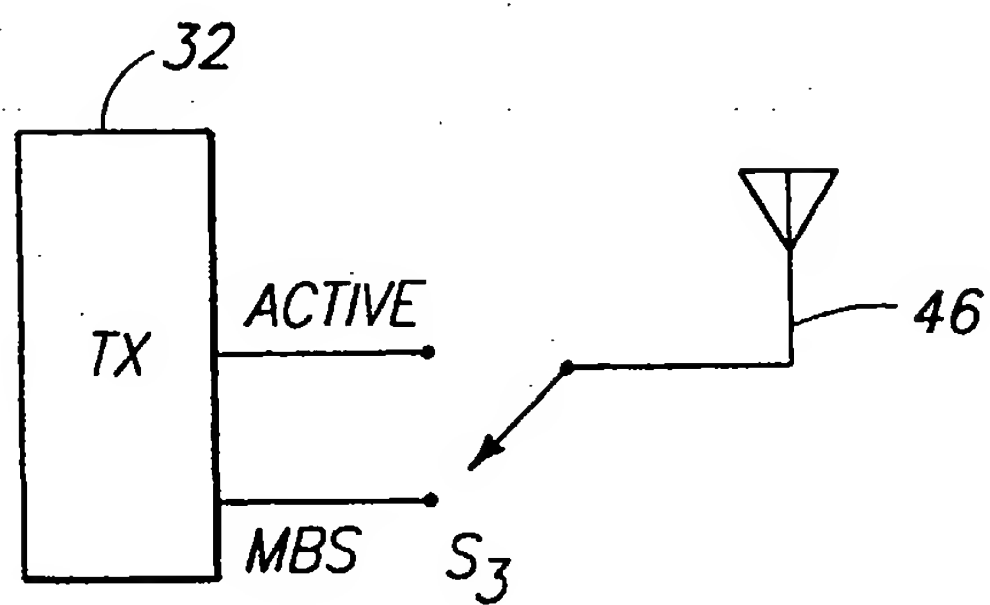
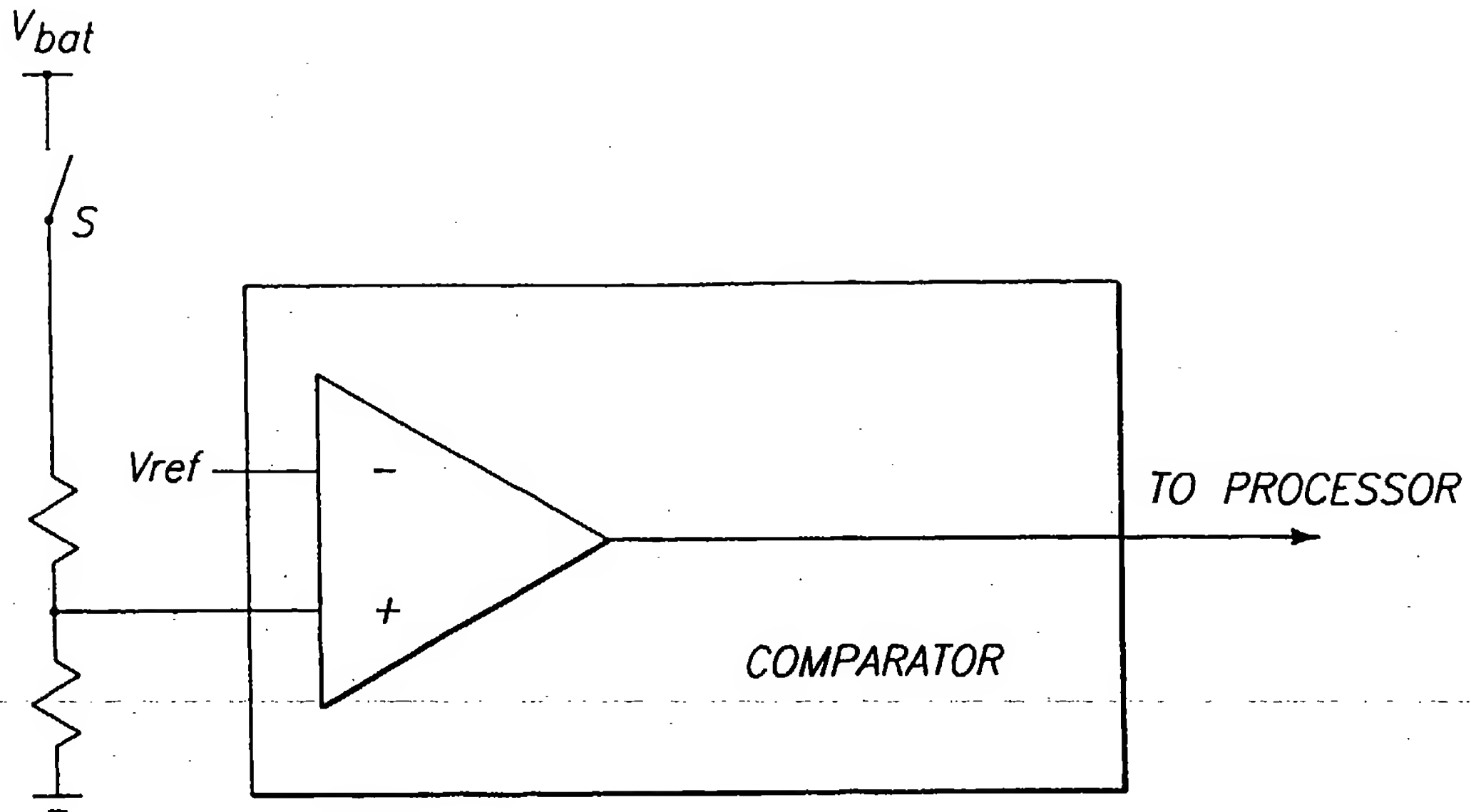


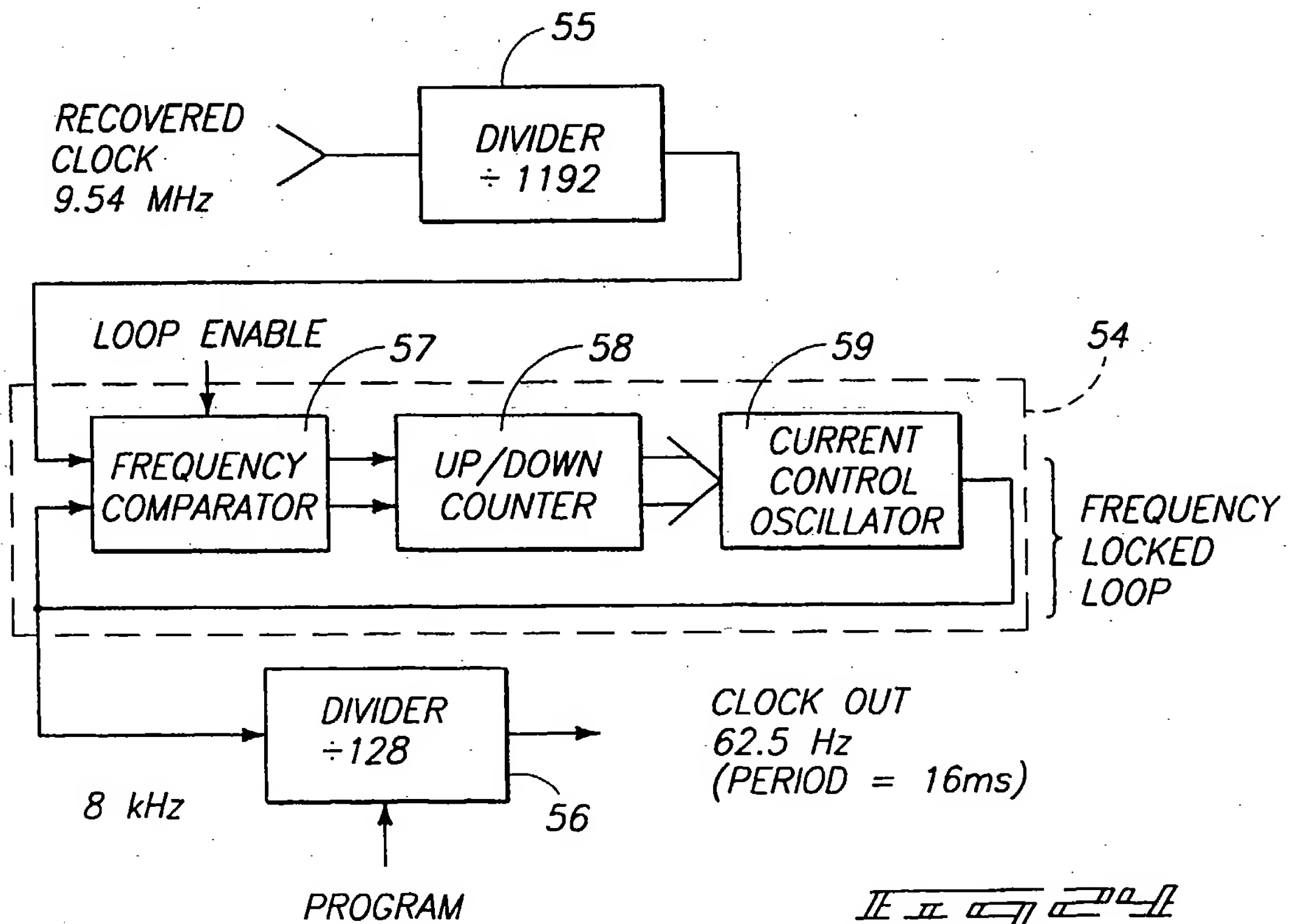
FIG. 3





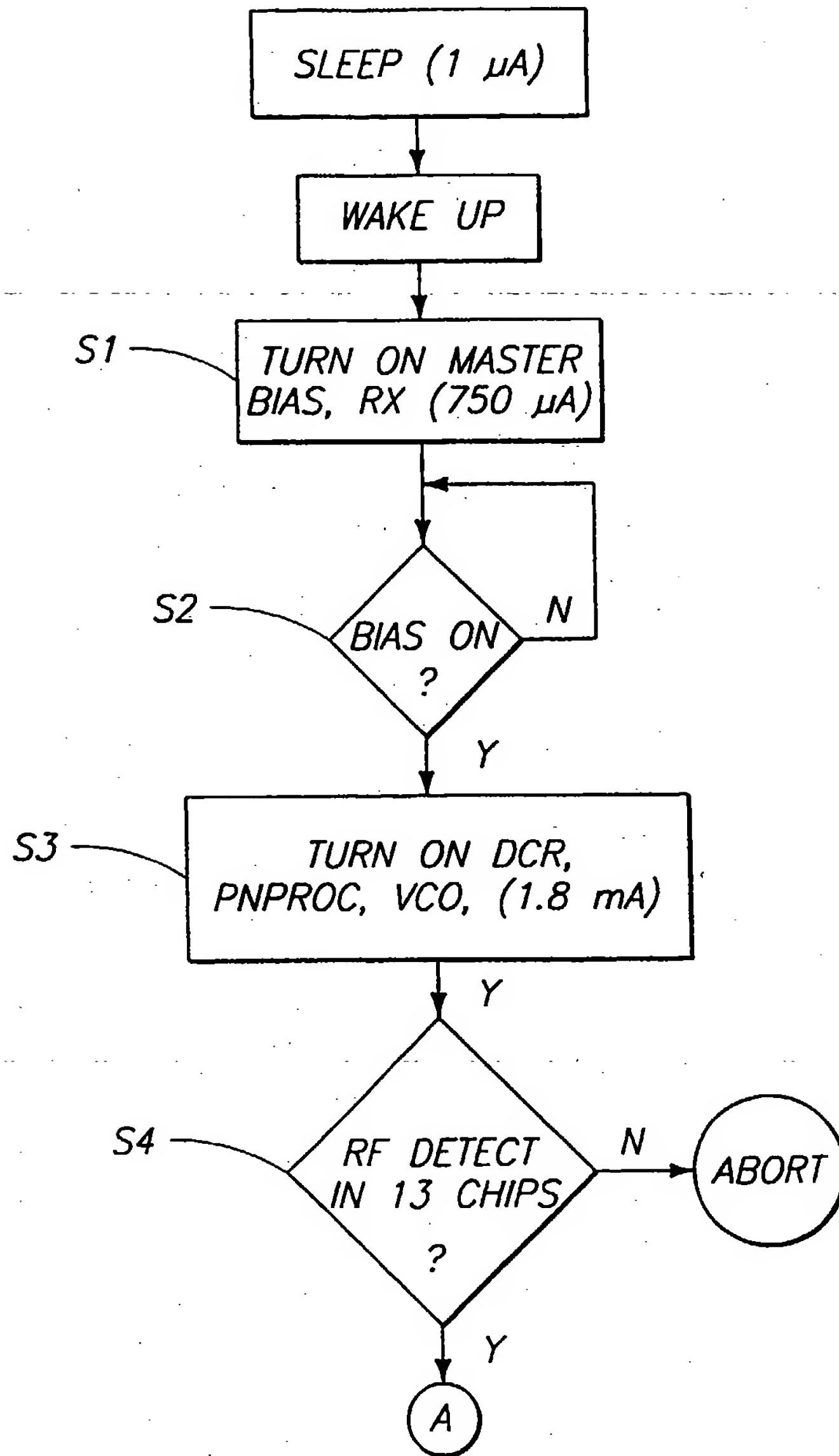
$V_{ref}$  = bandgap voltage  $\approx 1.2$  V for silicon

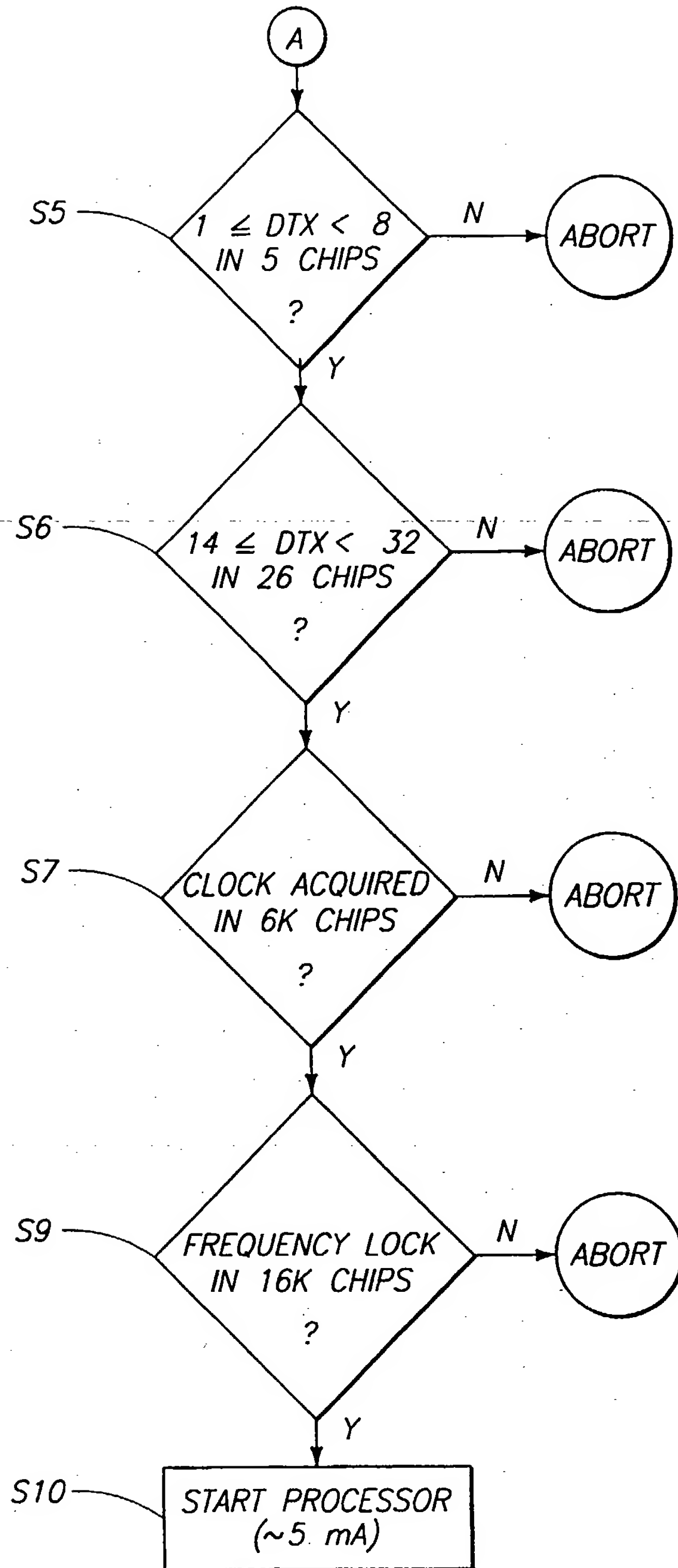
II II II II II

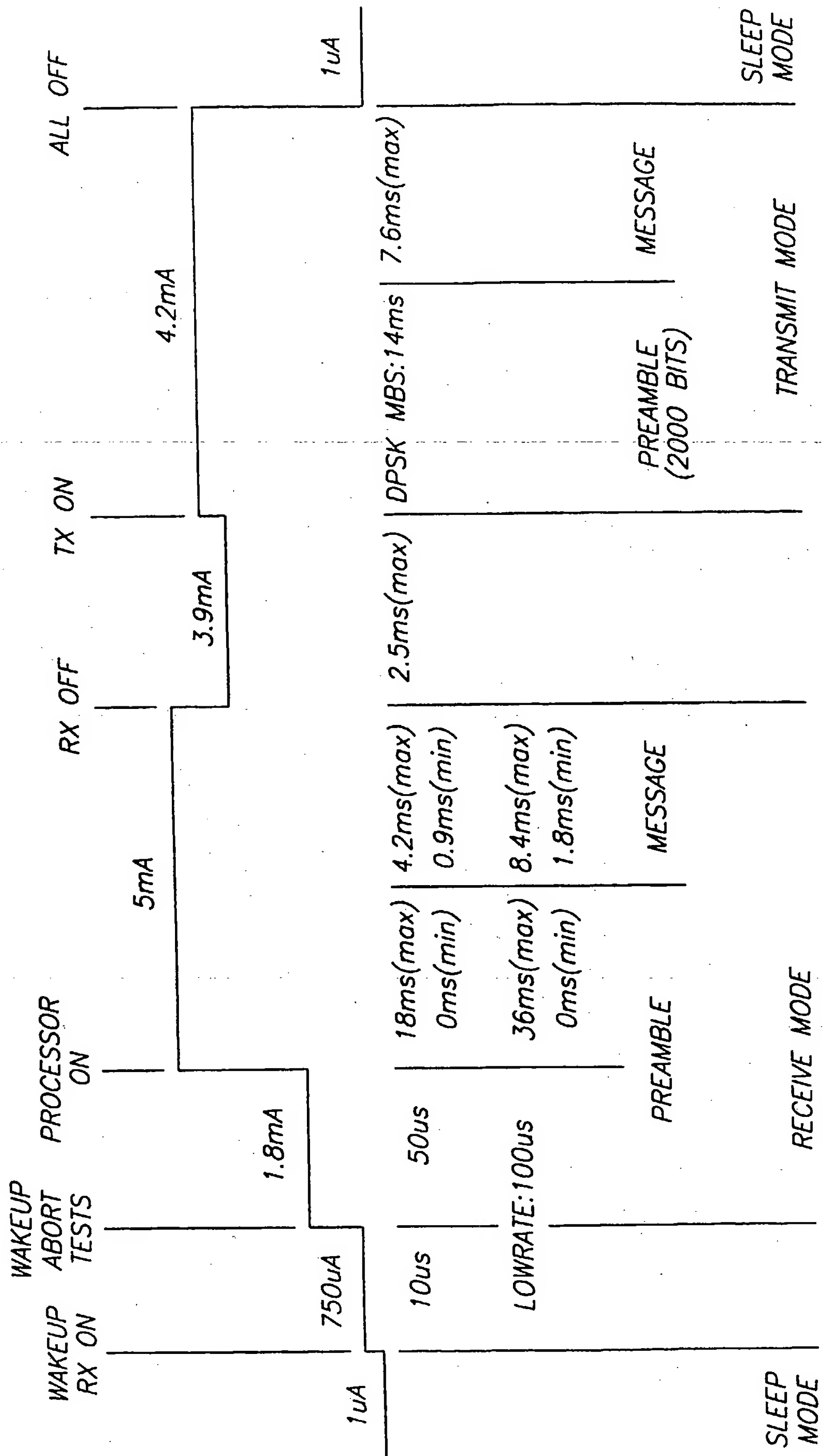


II II II II II

WAKEUP SEQUENCE







И. П. Б.

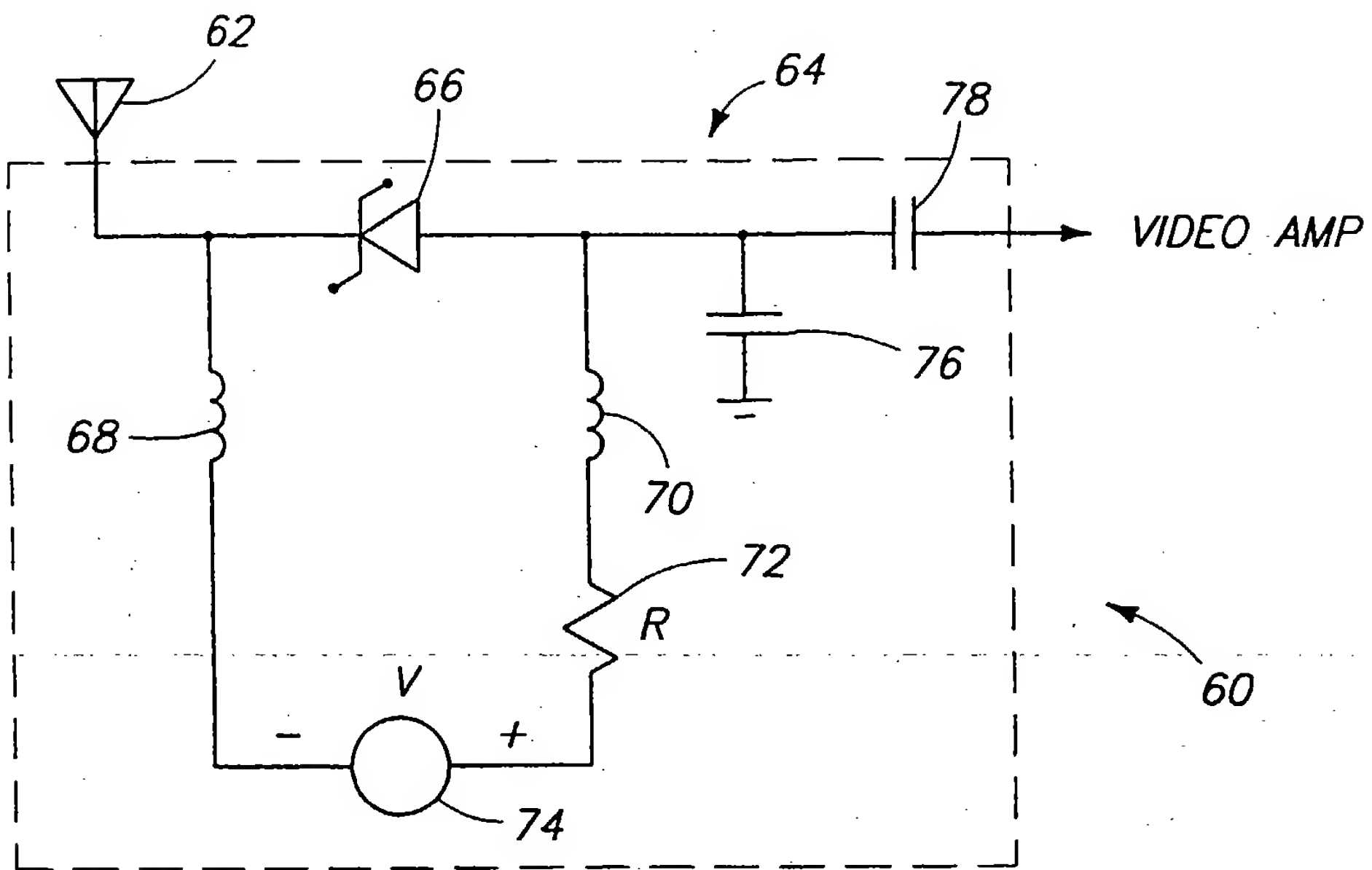


FIG. 2

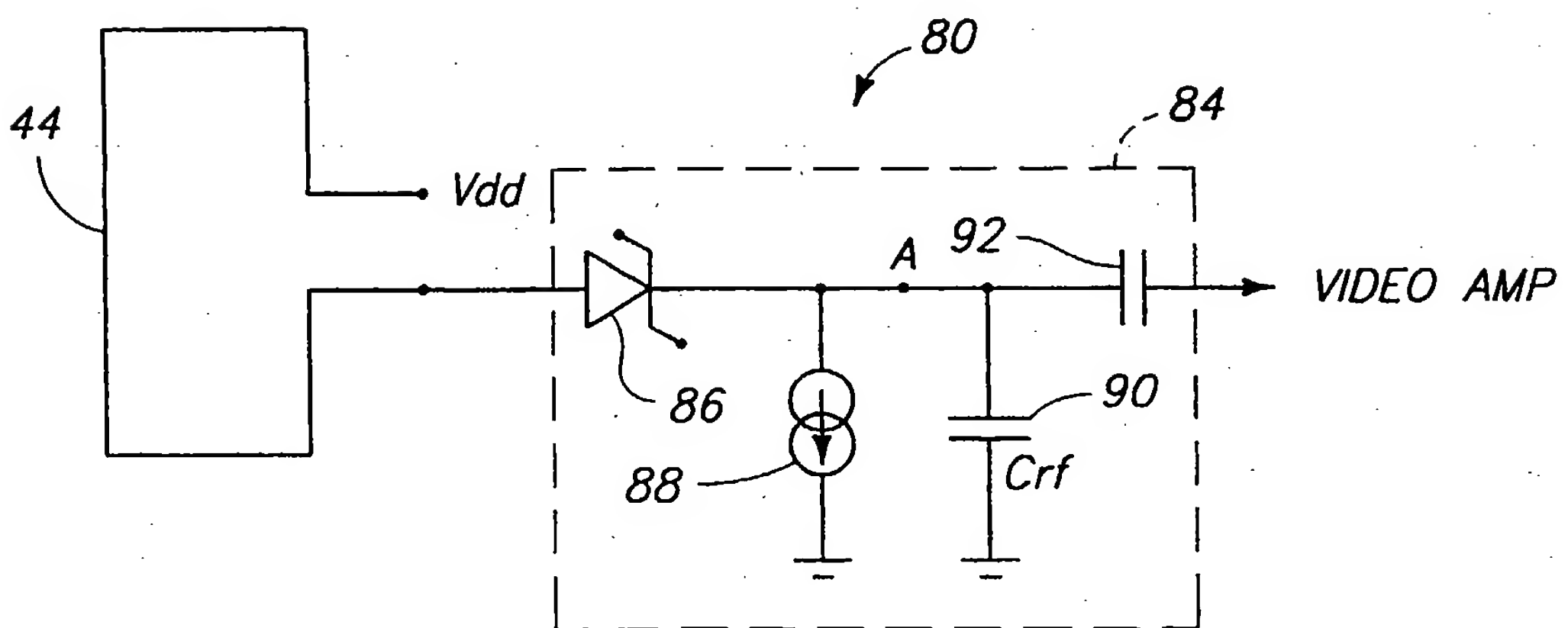
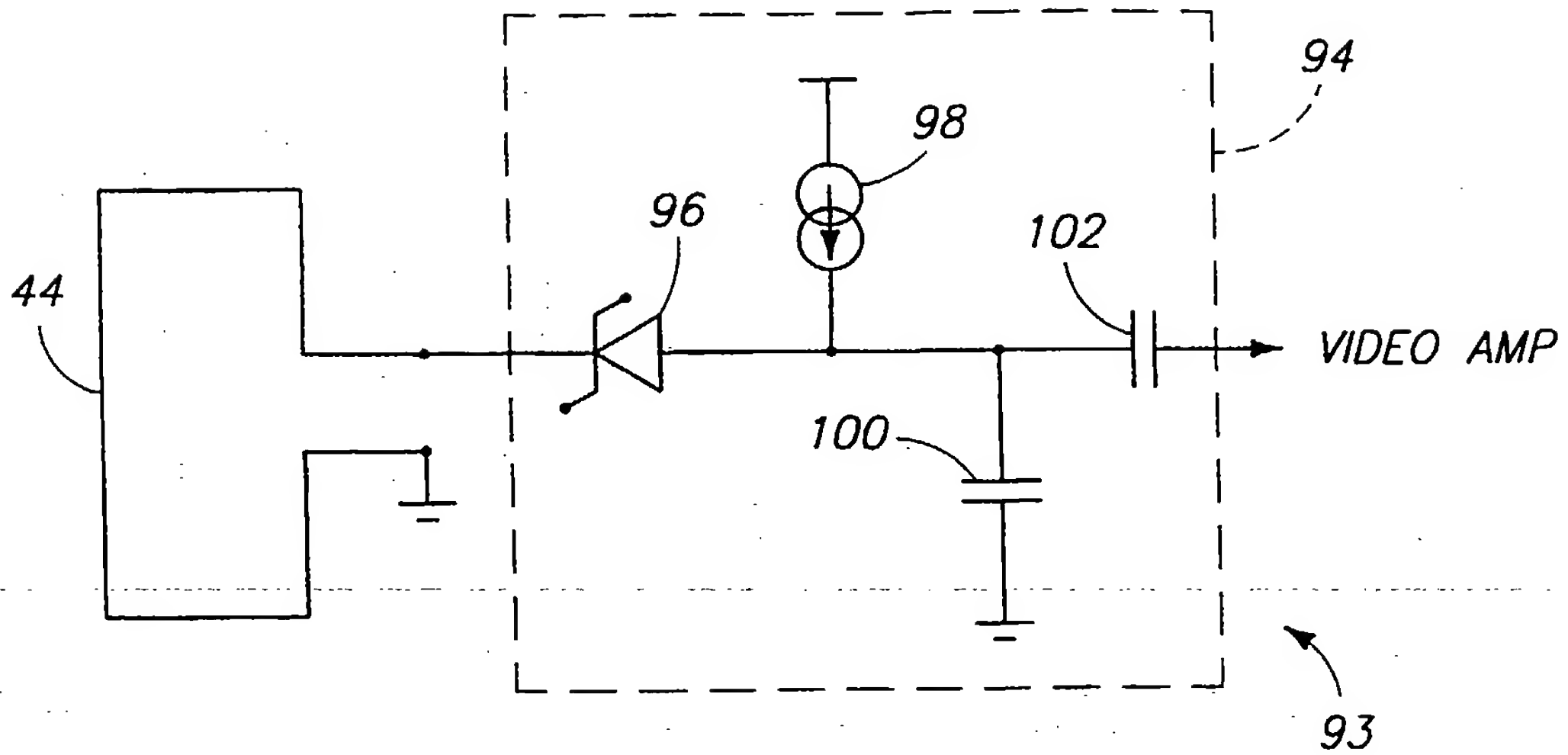
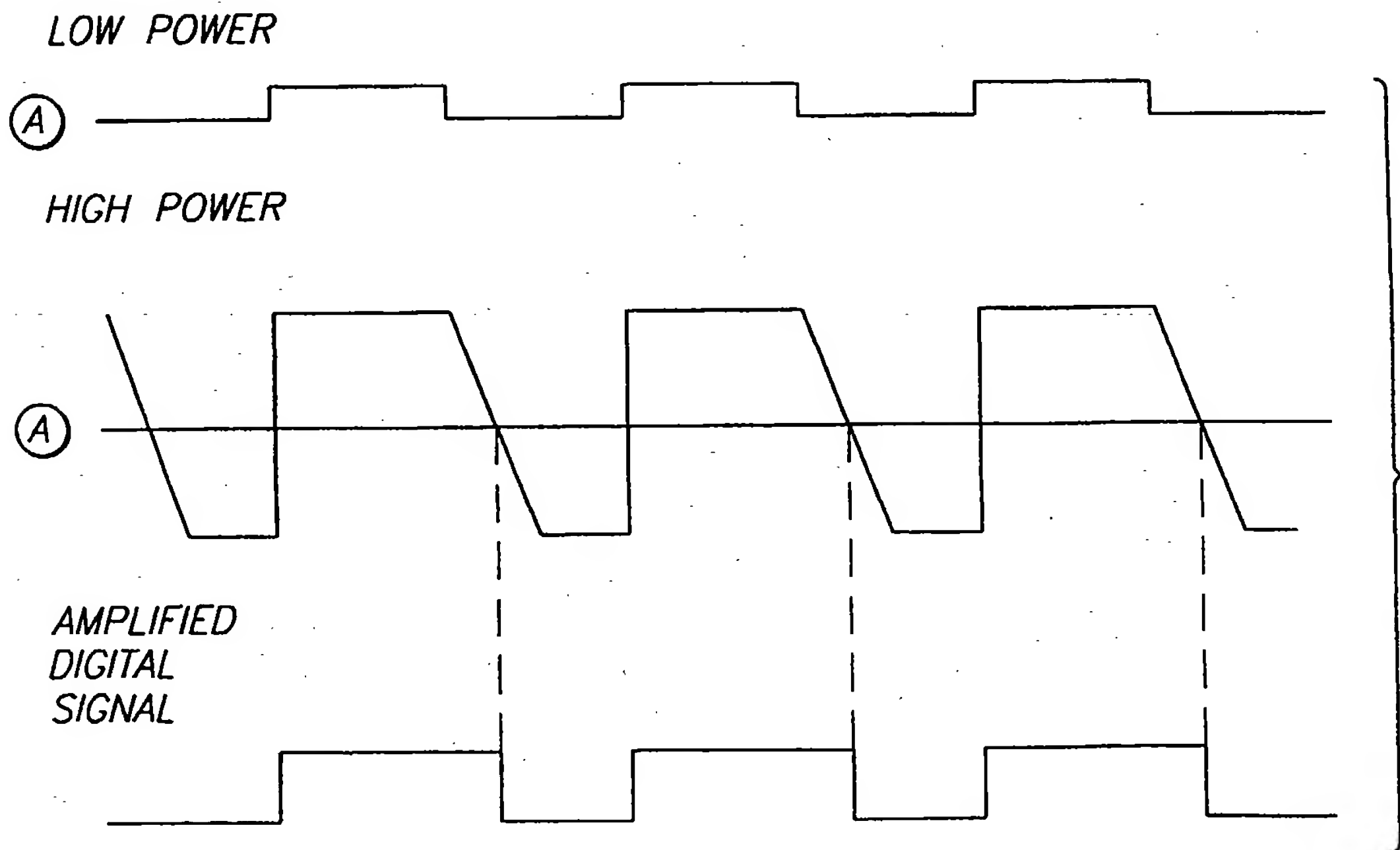


FIG. 3



*II II II II*



*II II II II*

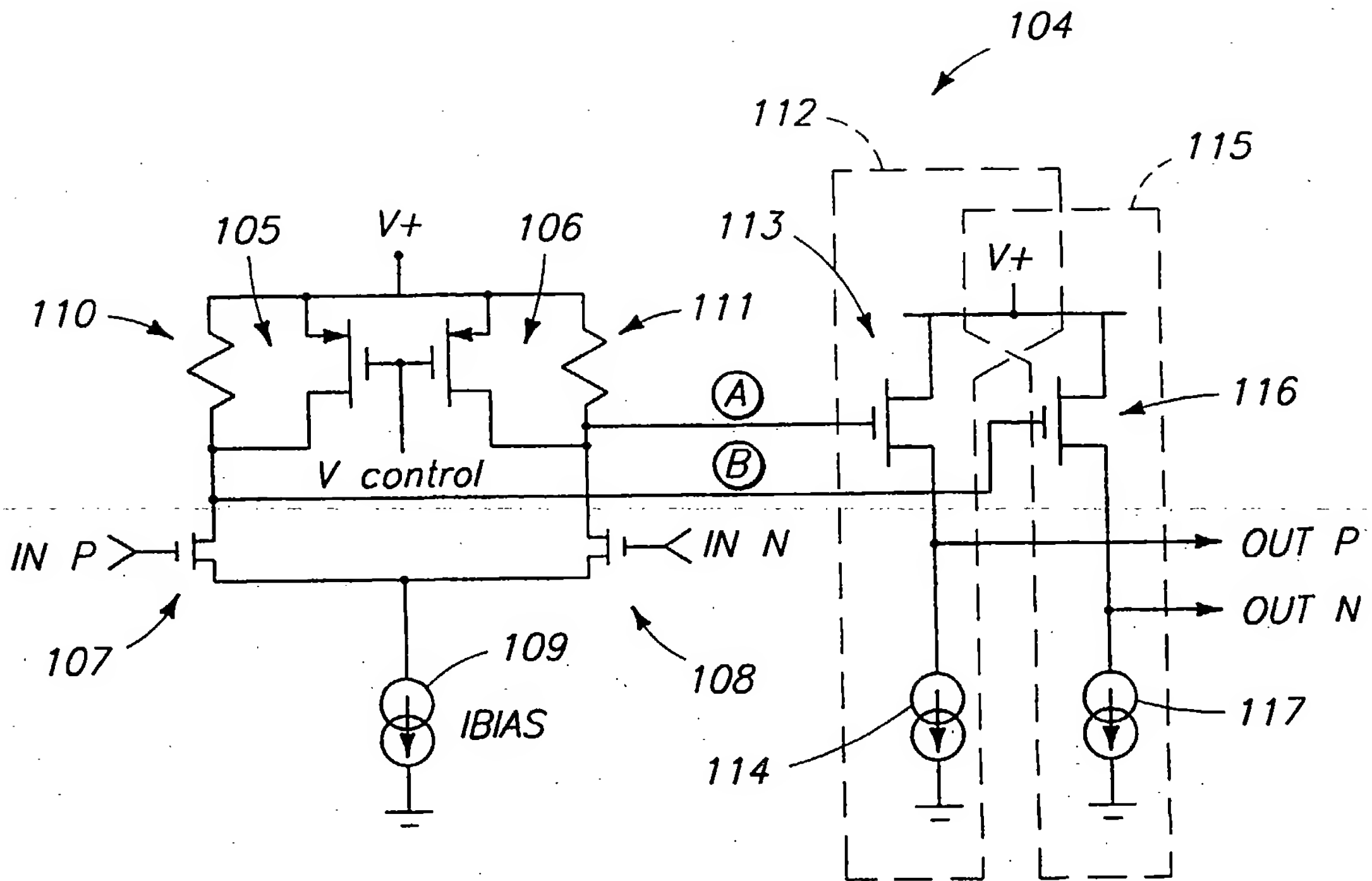


FIG. 2

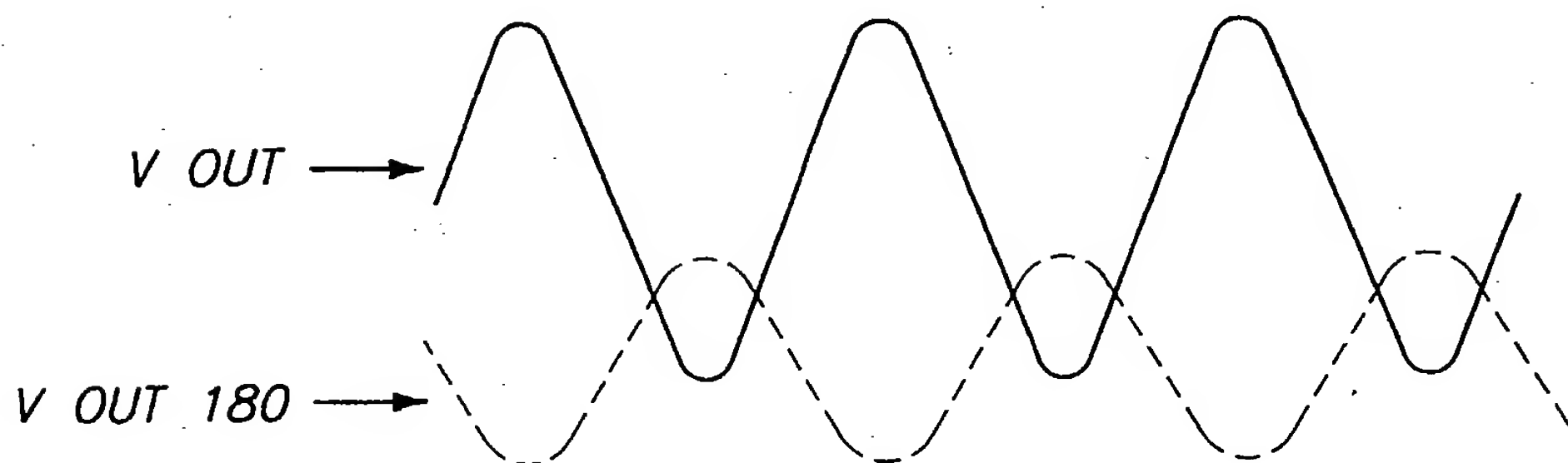
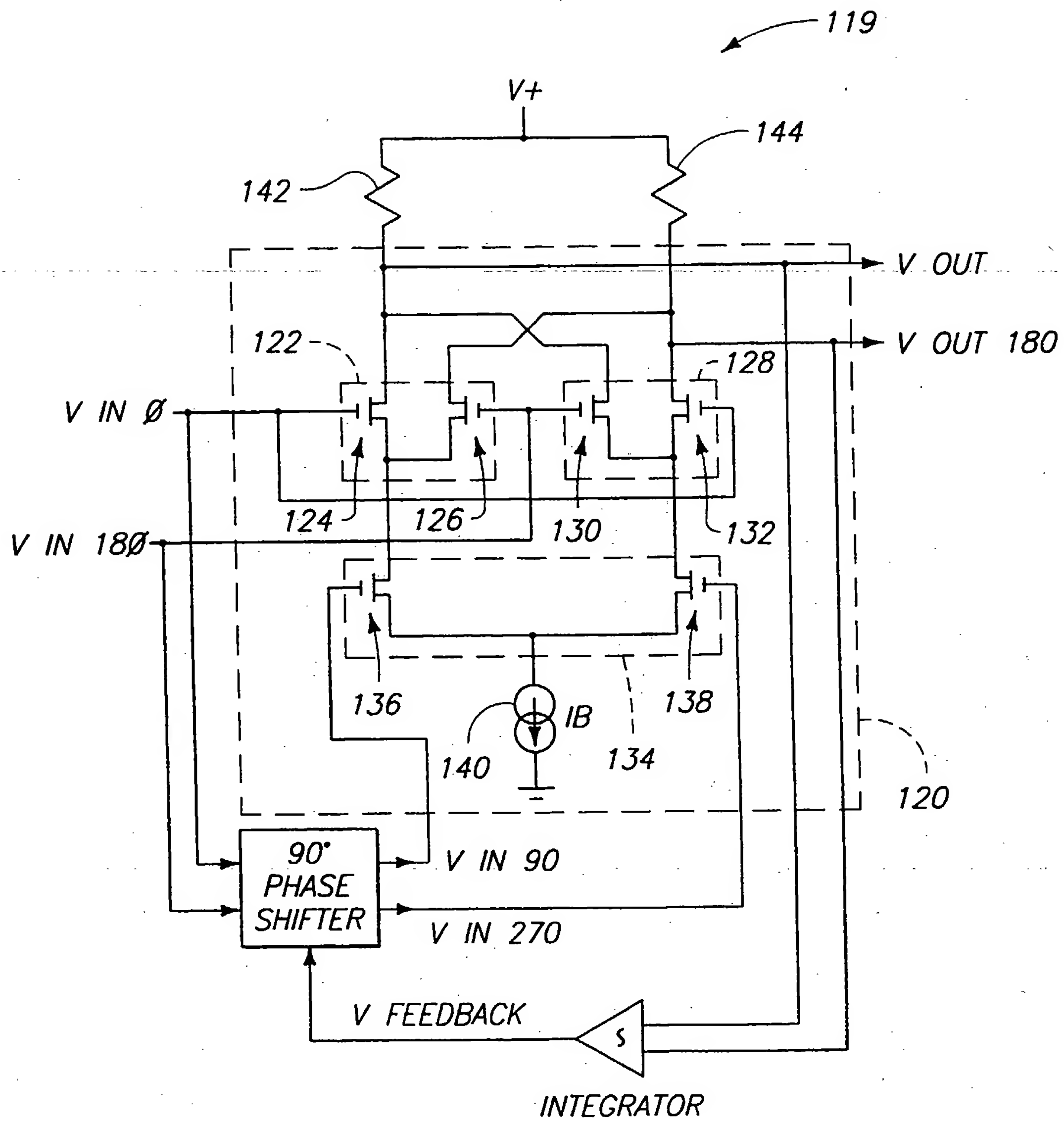
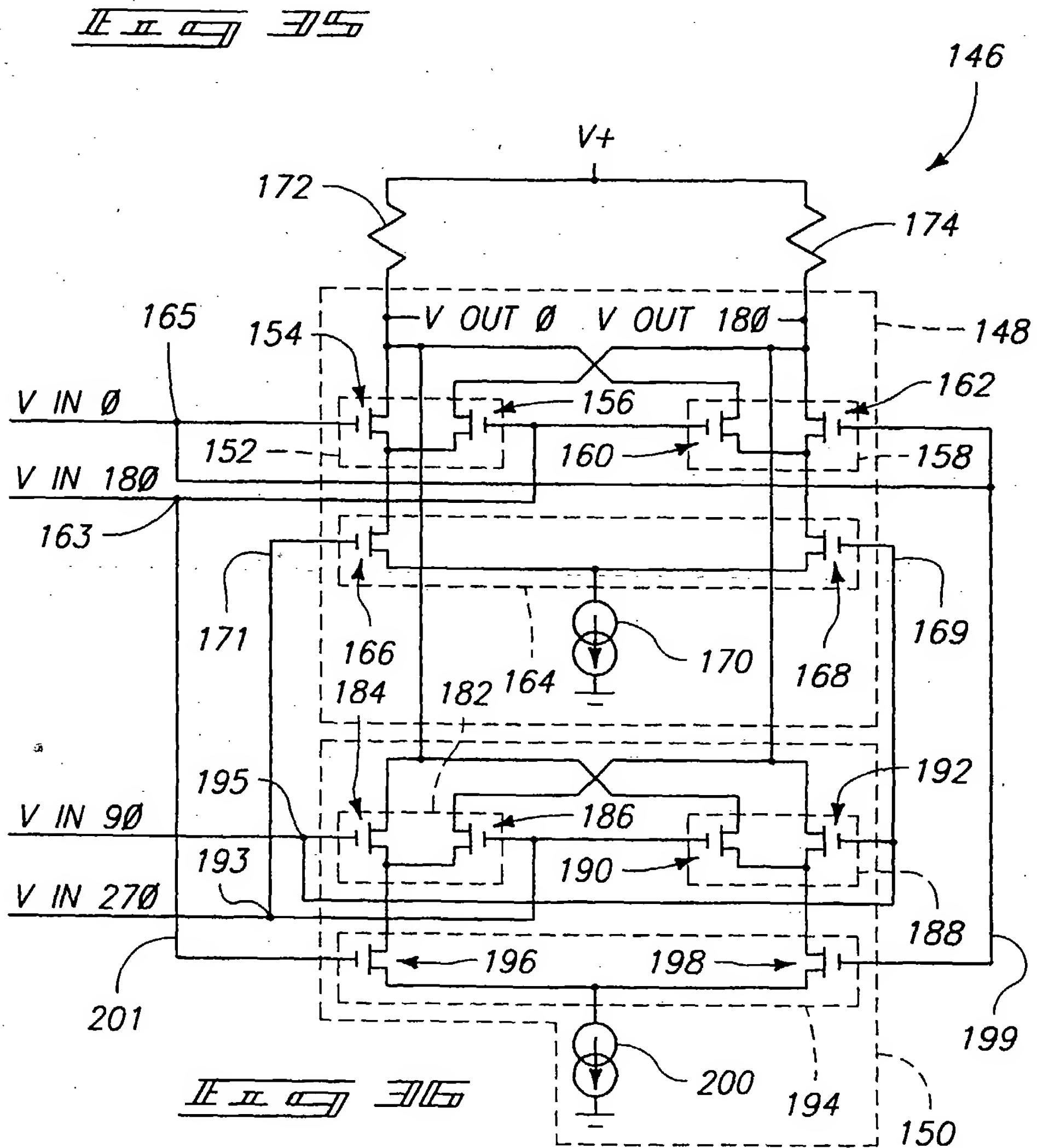
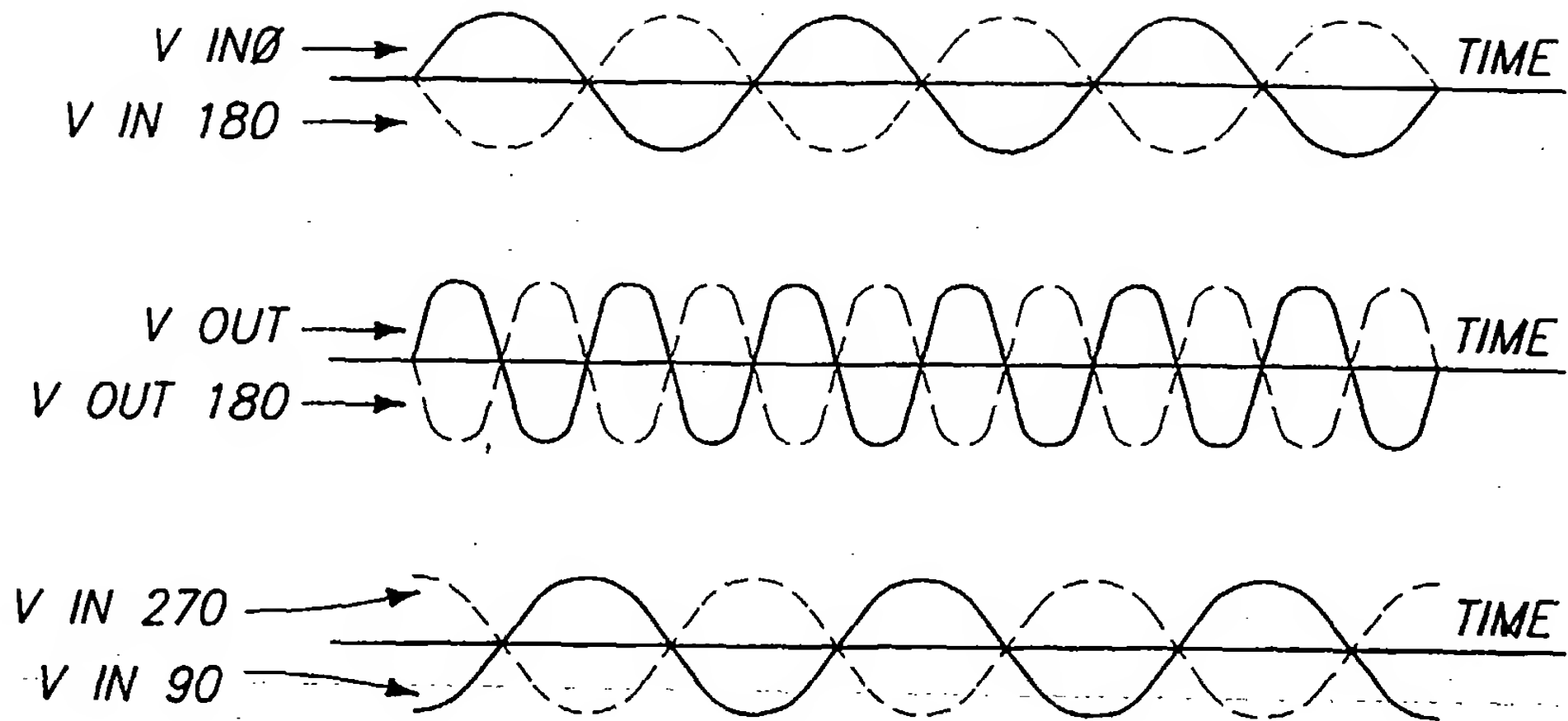


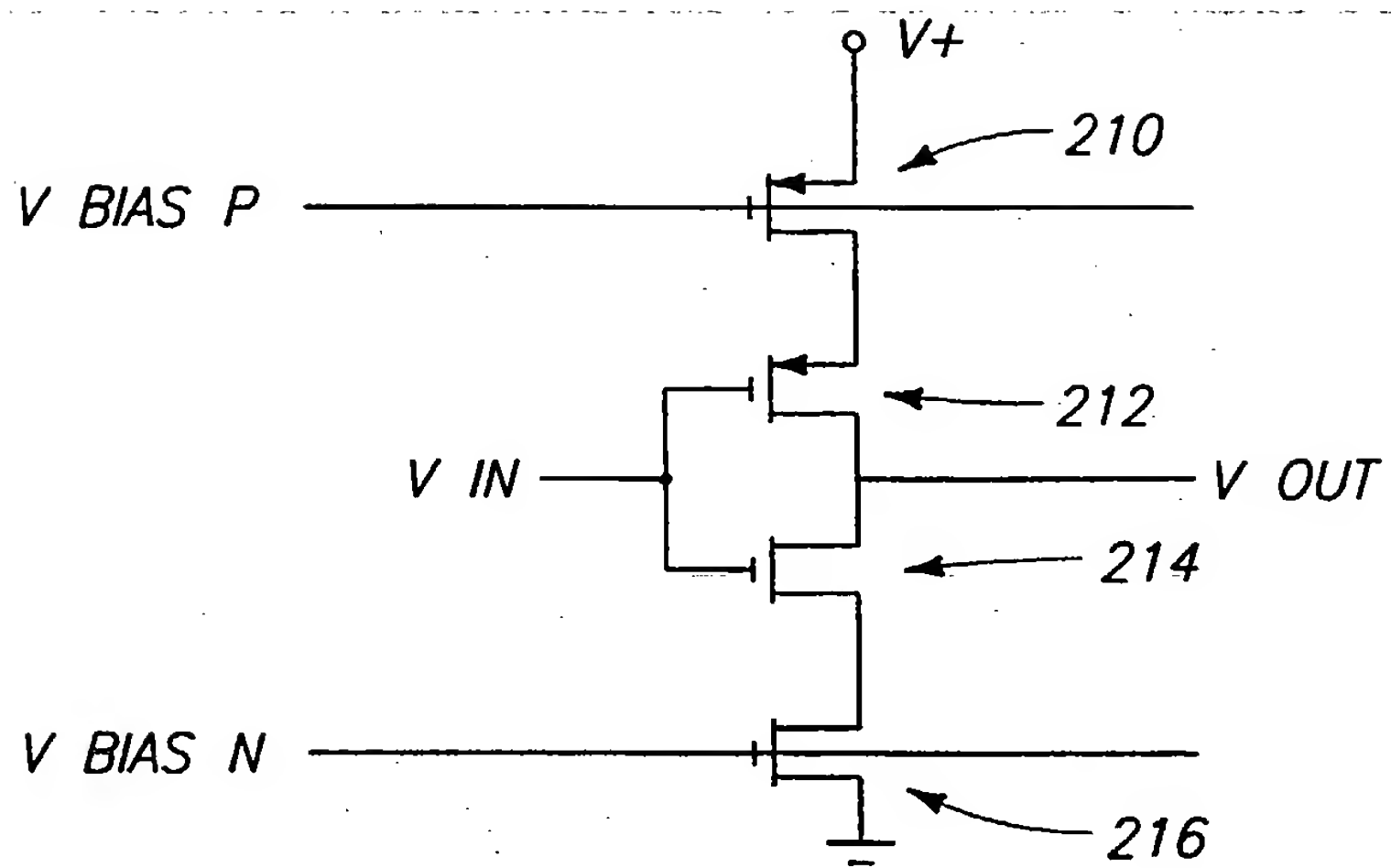
FIG. 3



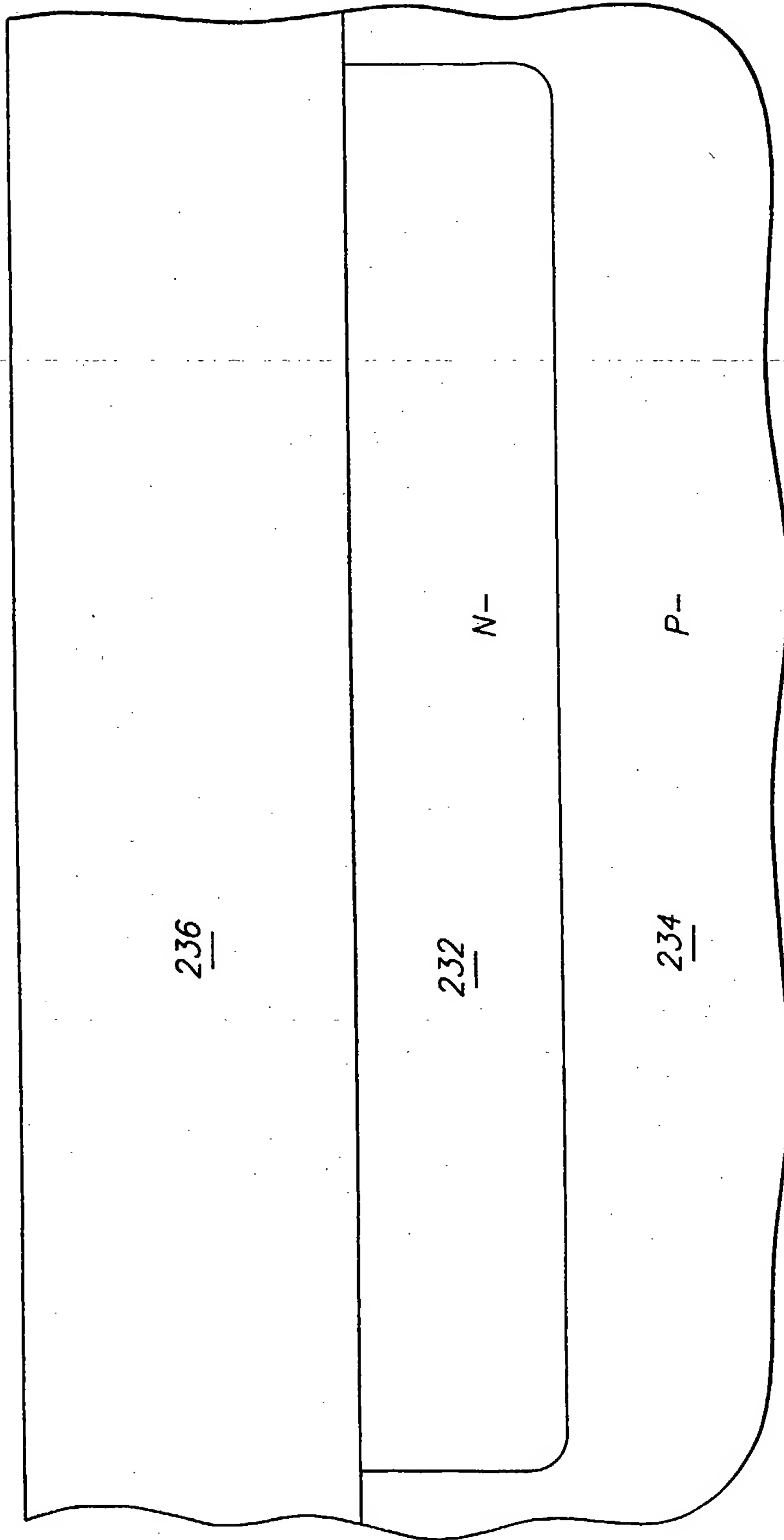
II II II II II II







IEEE



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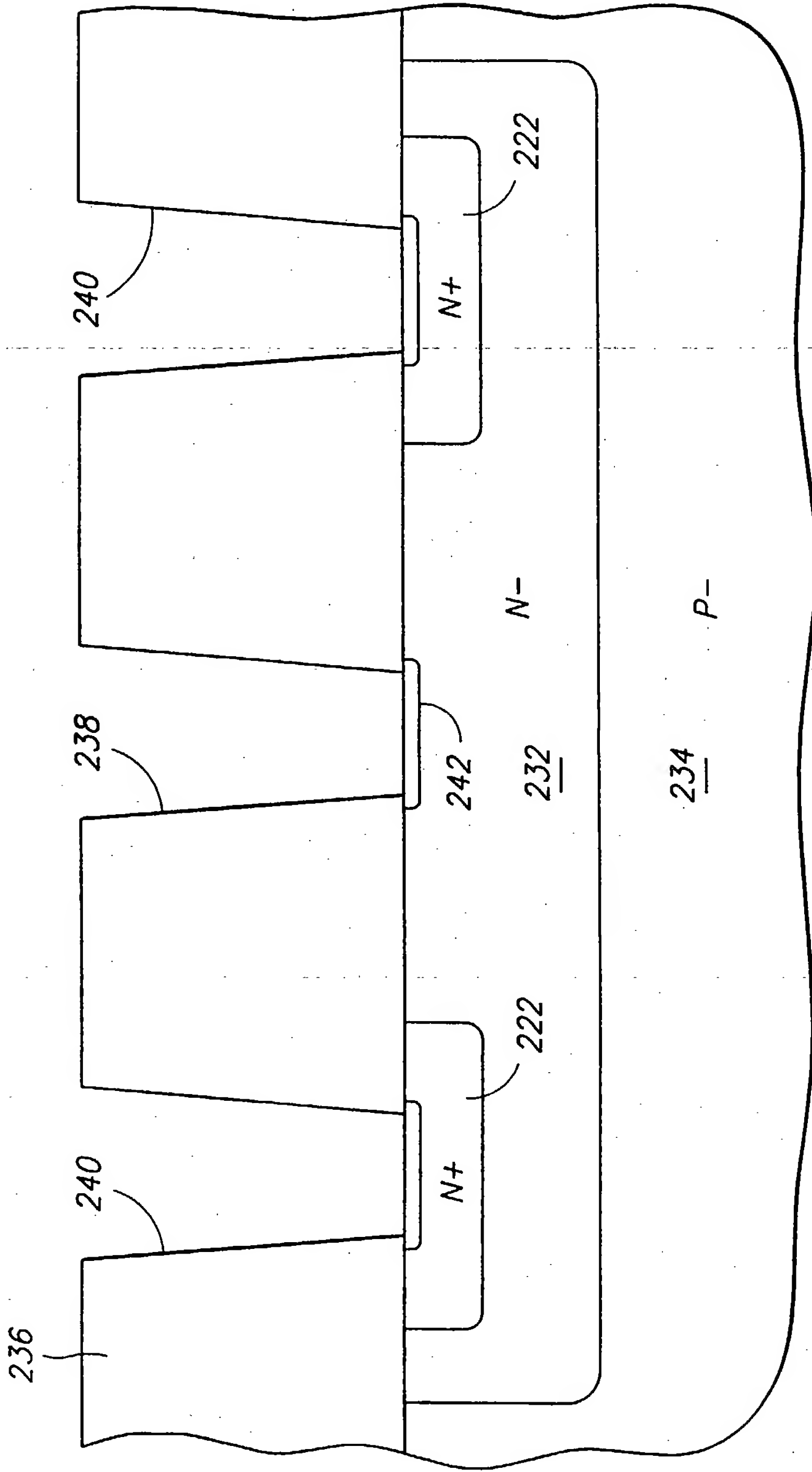
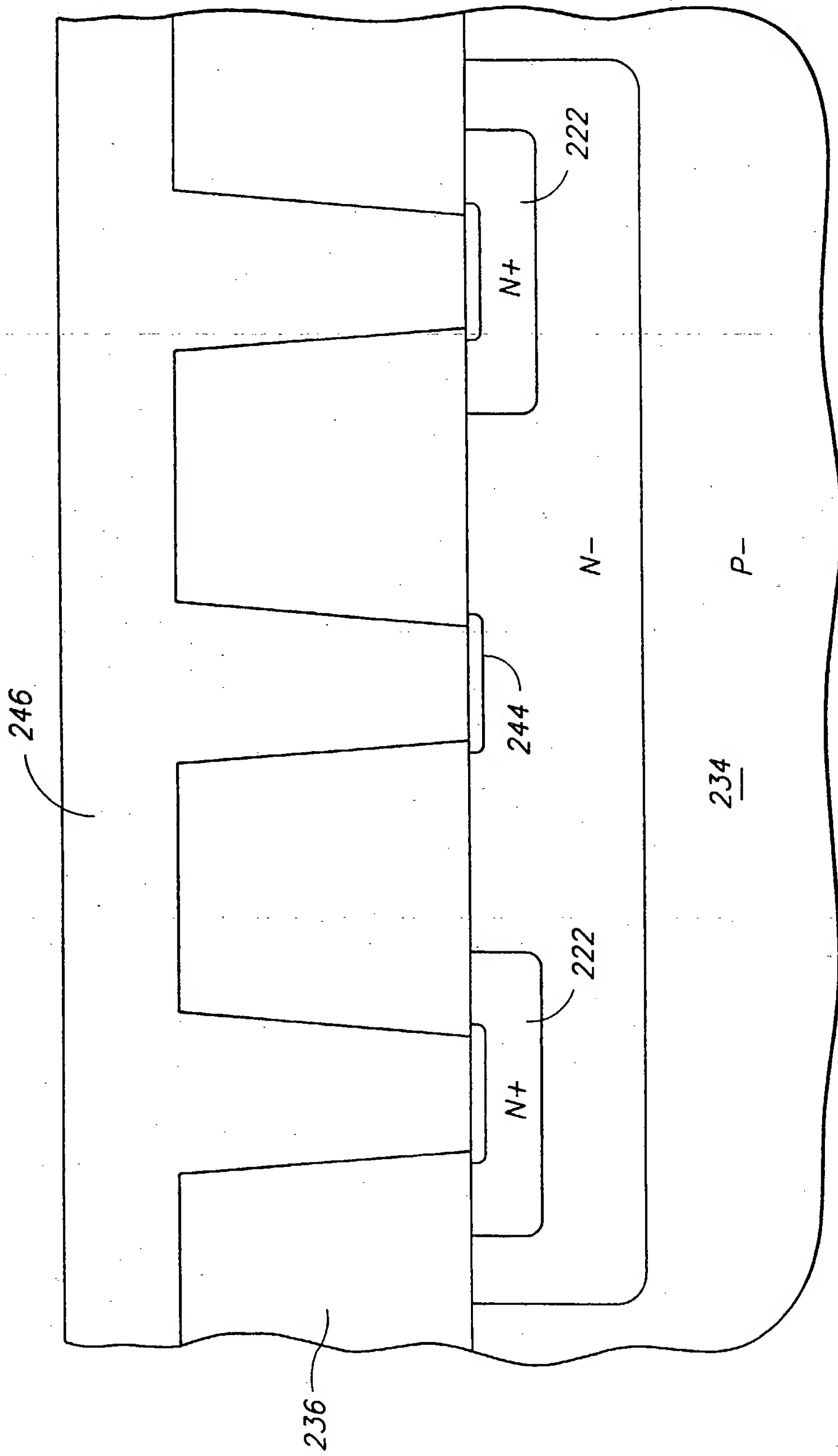
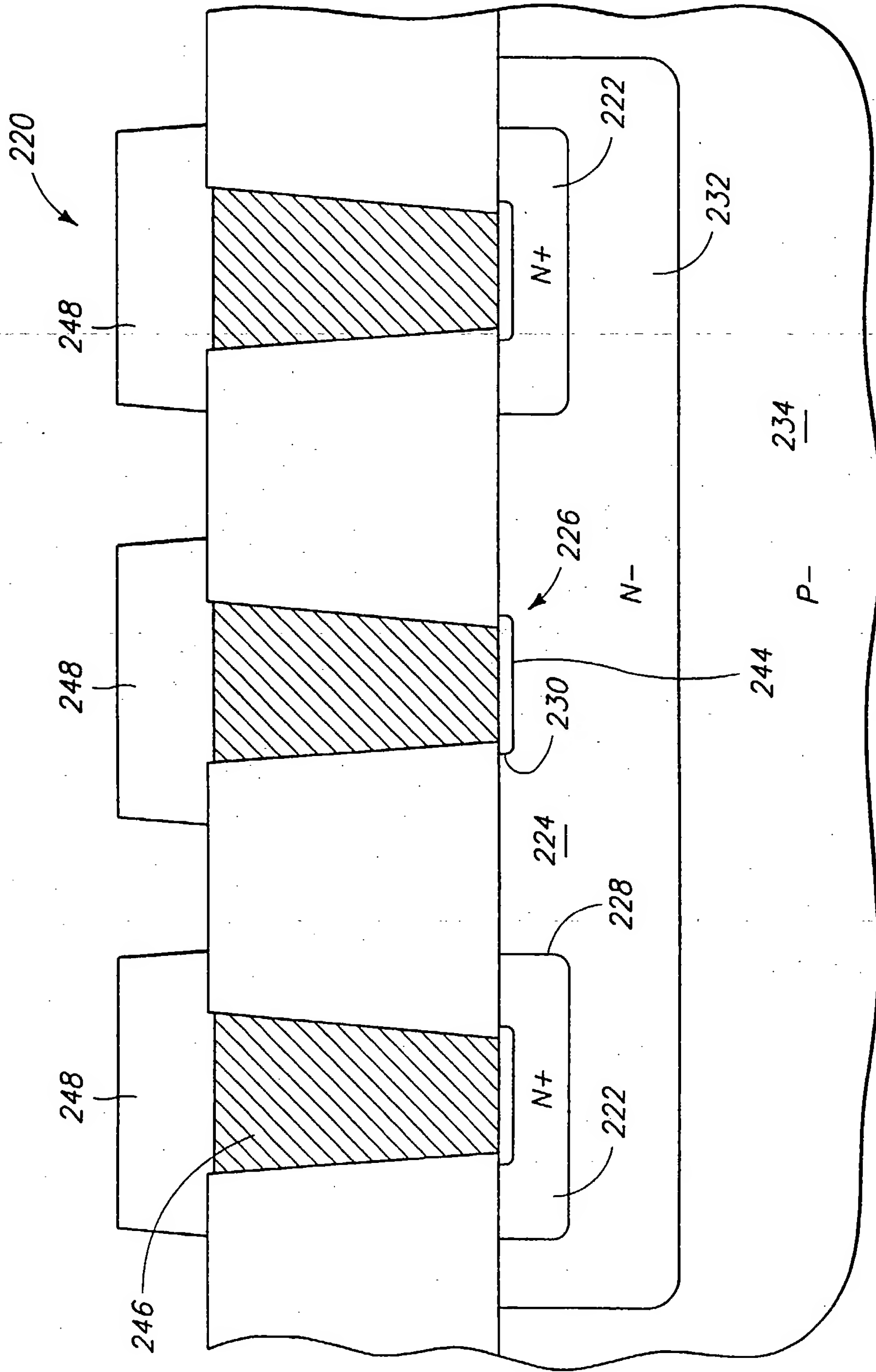
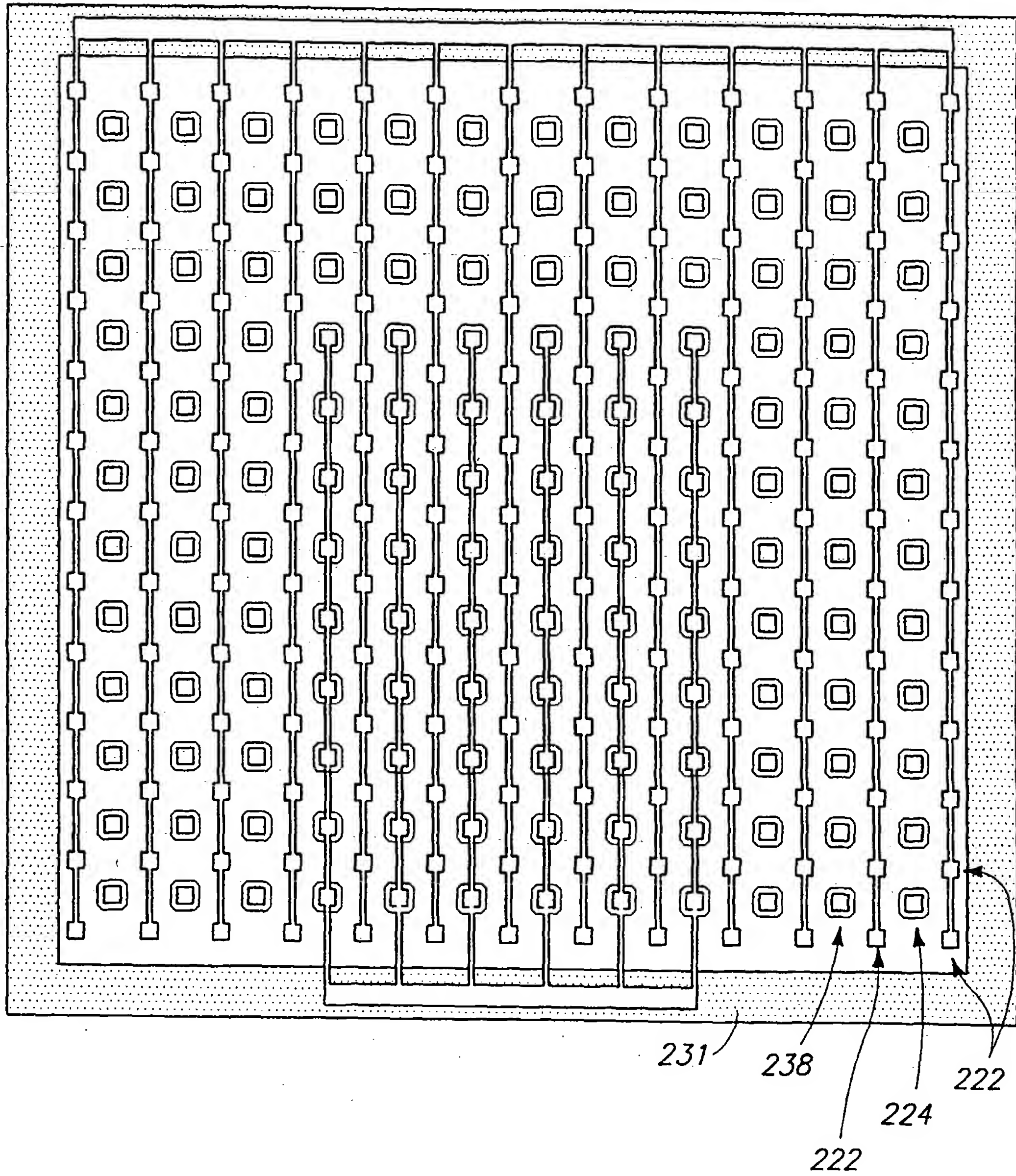


FIG. 3



II II II II II





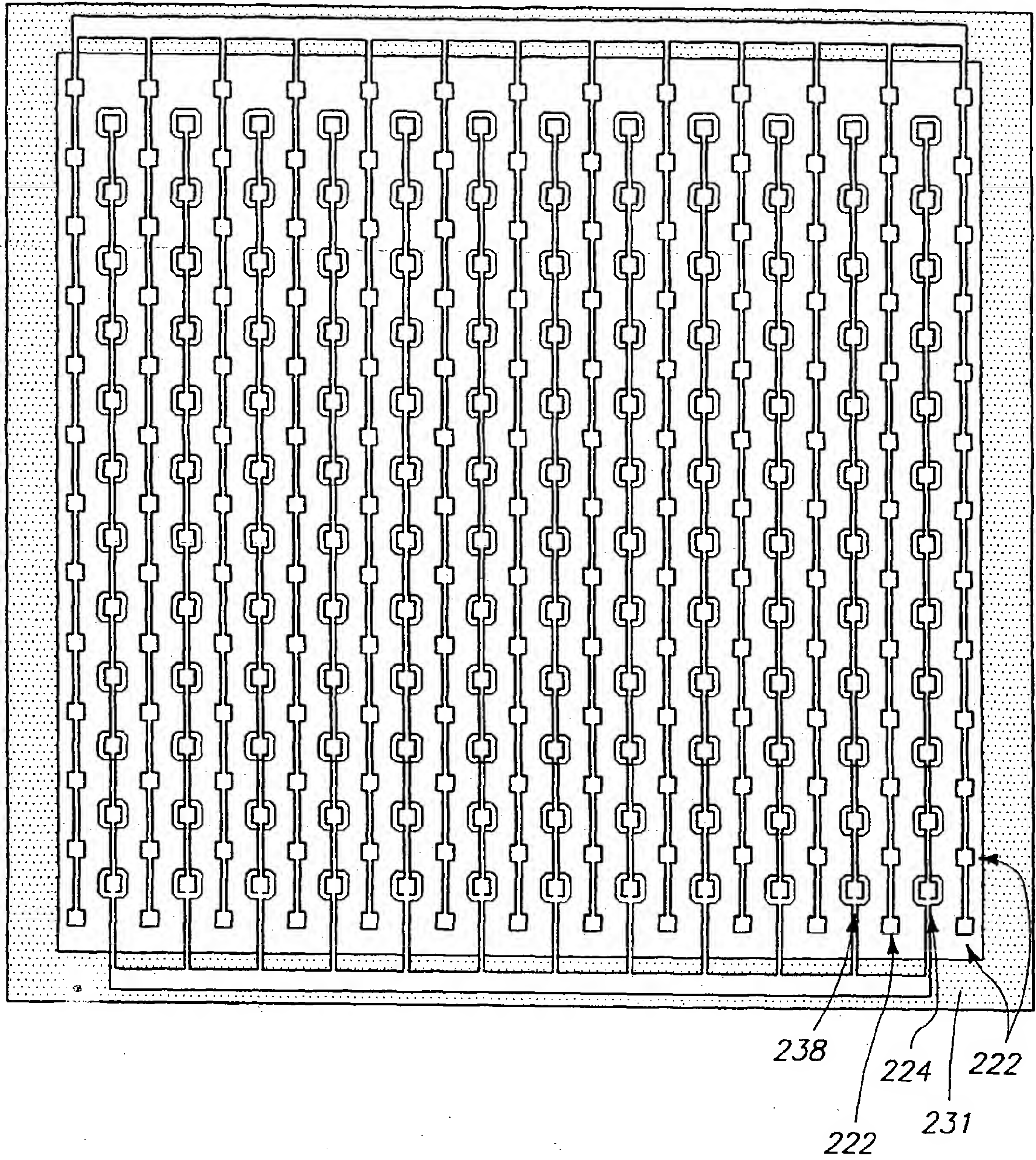
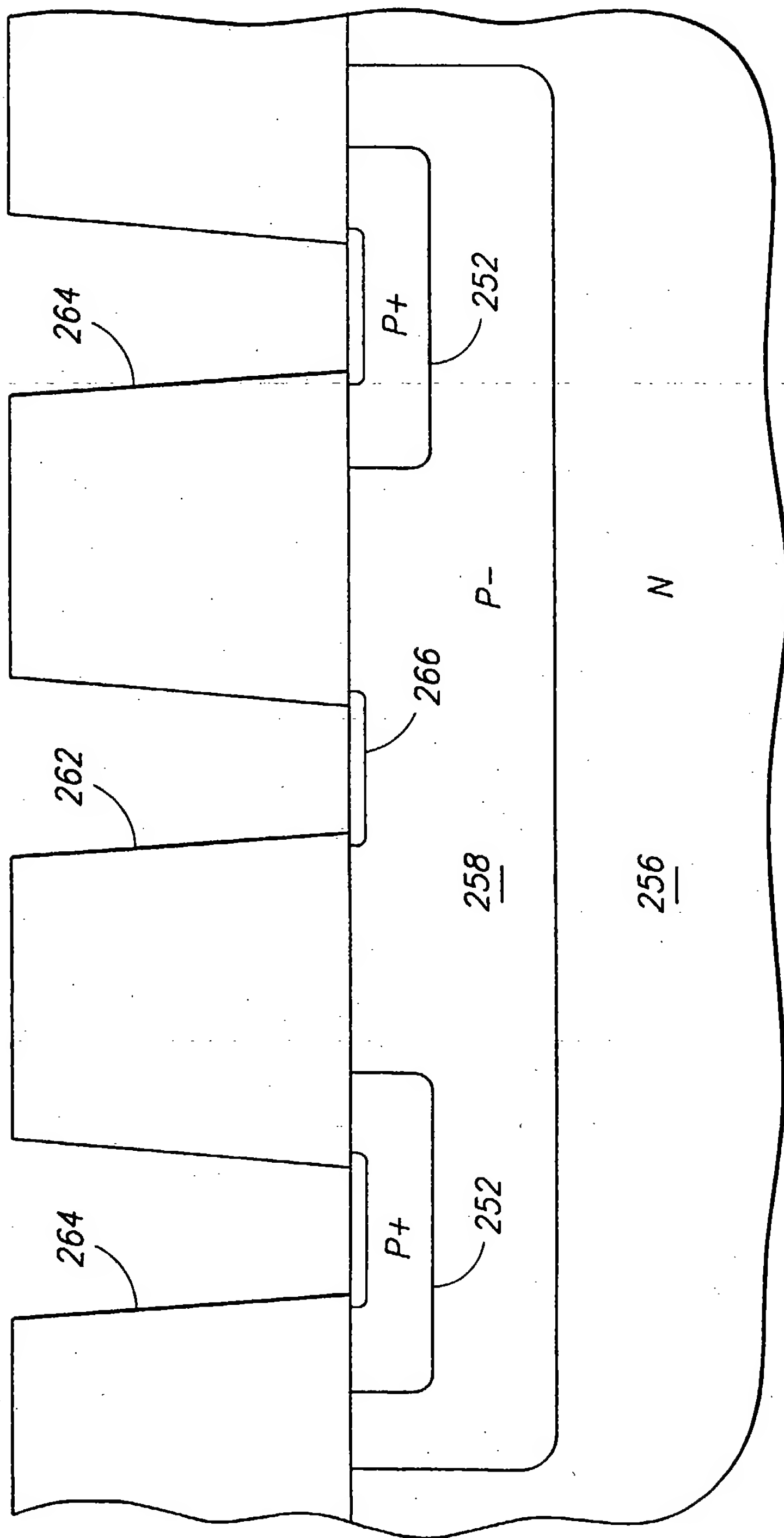


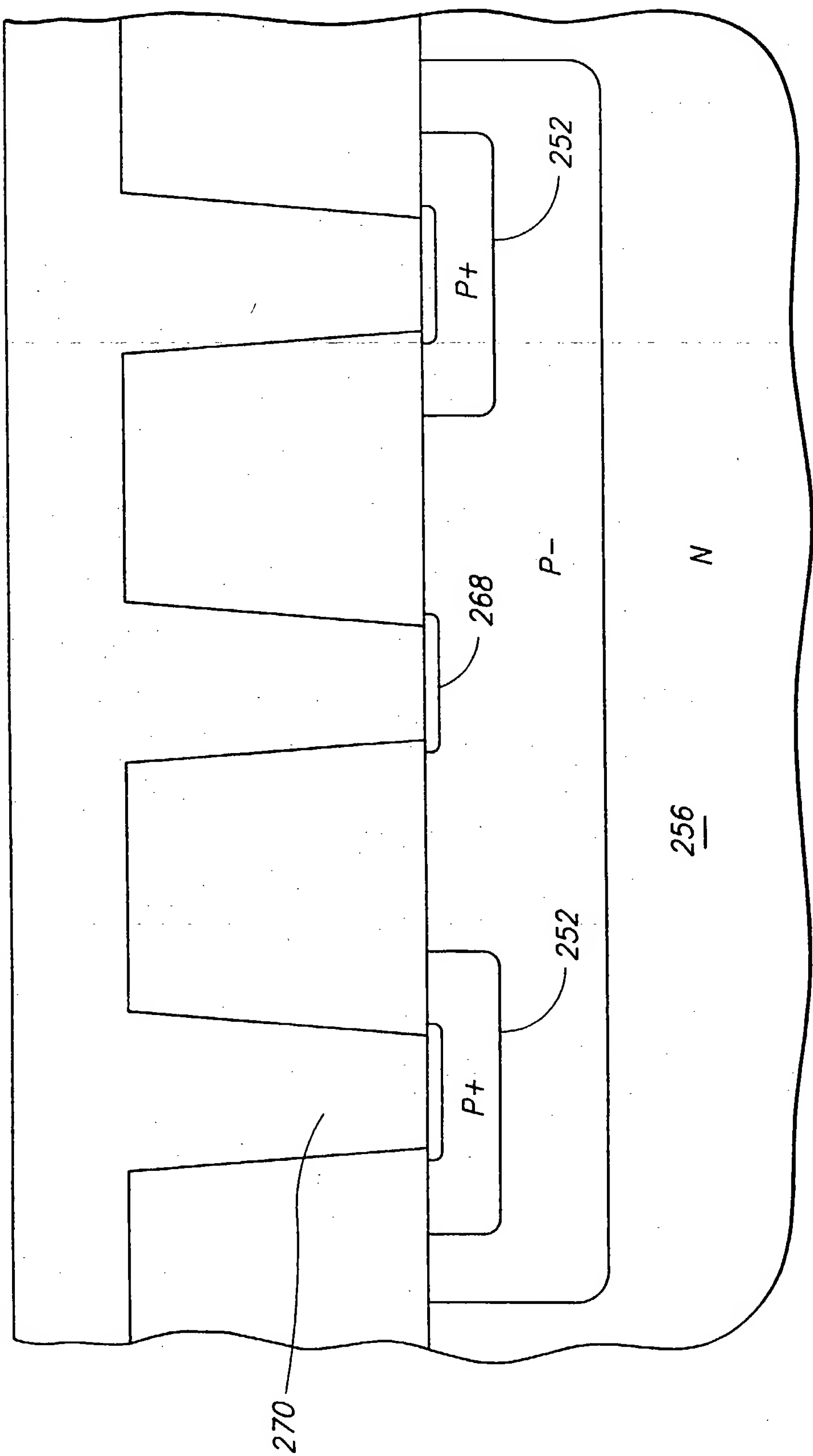
FIG. 2



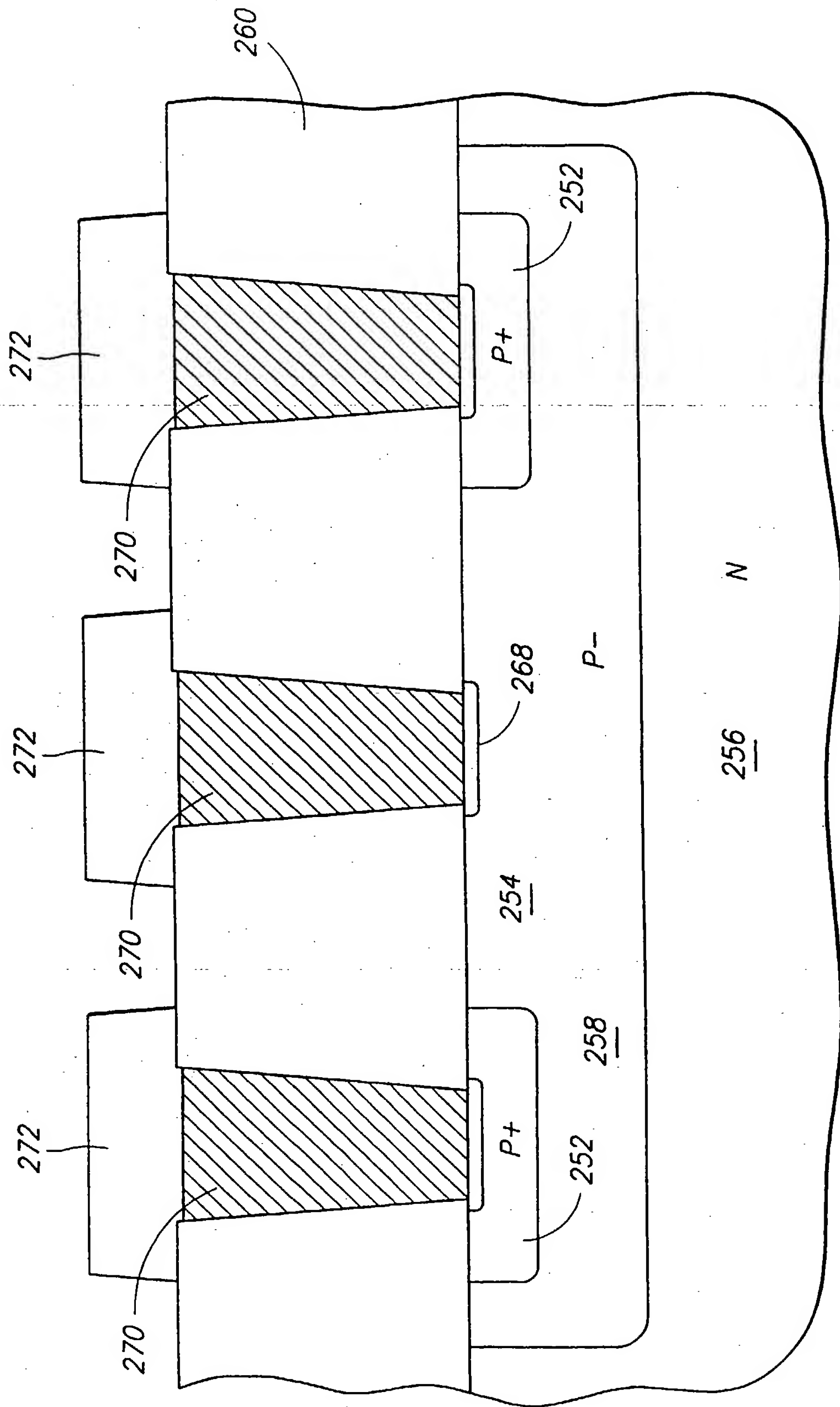




II II II II II



II II II II II



II II II II II II

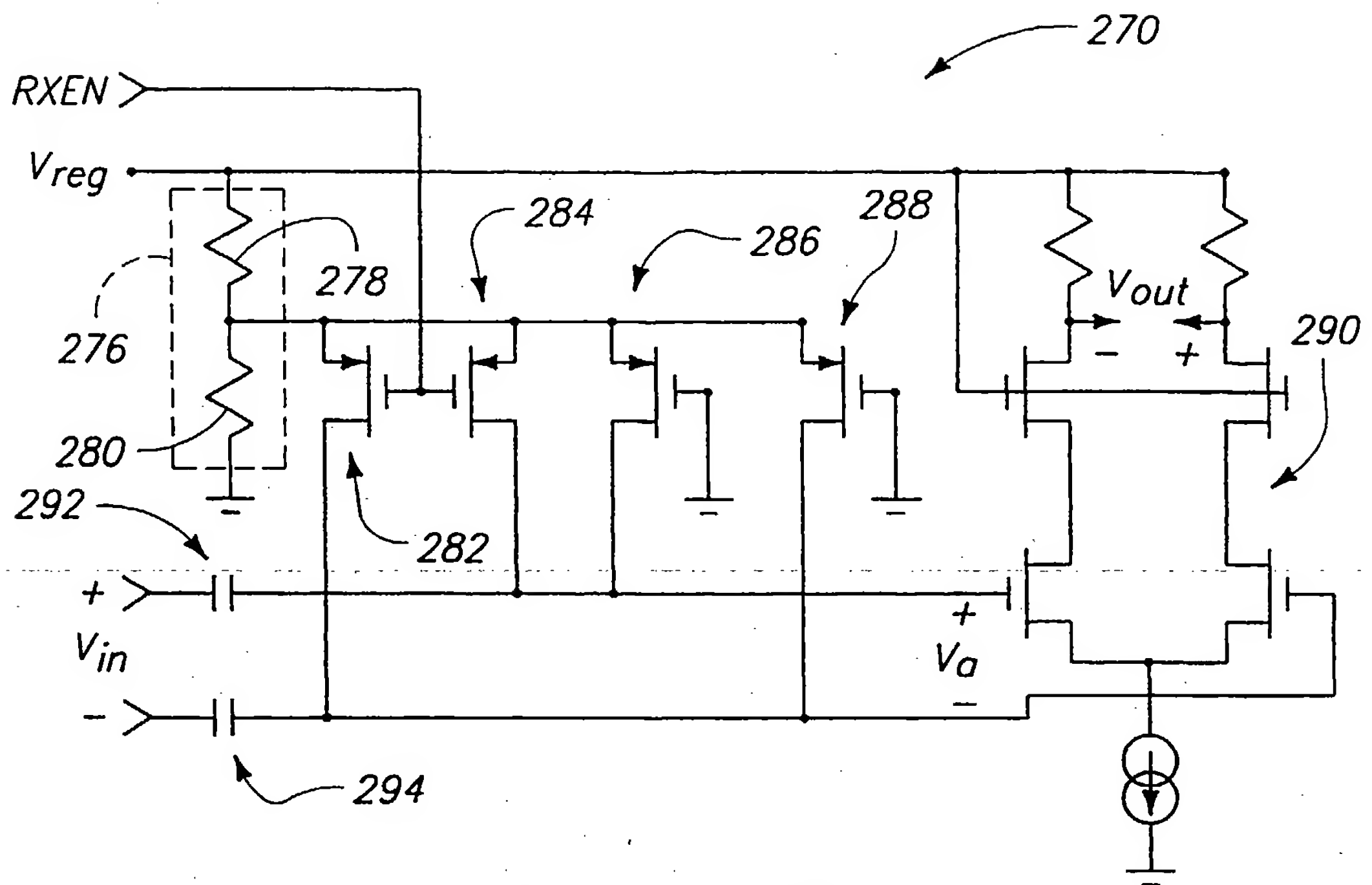


FIG. 2

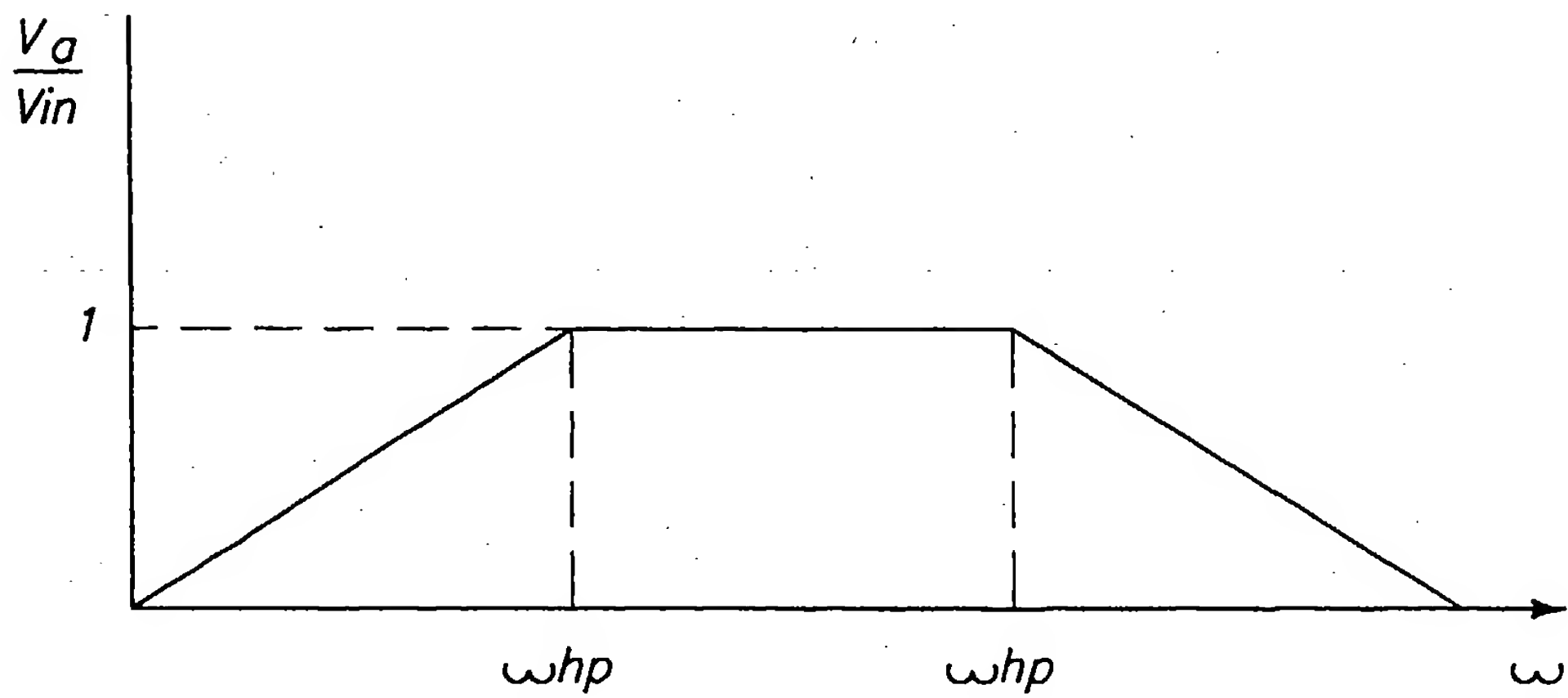
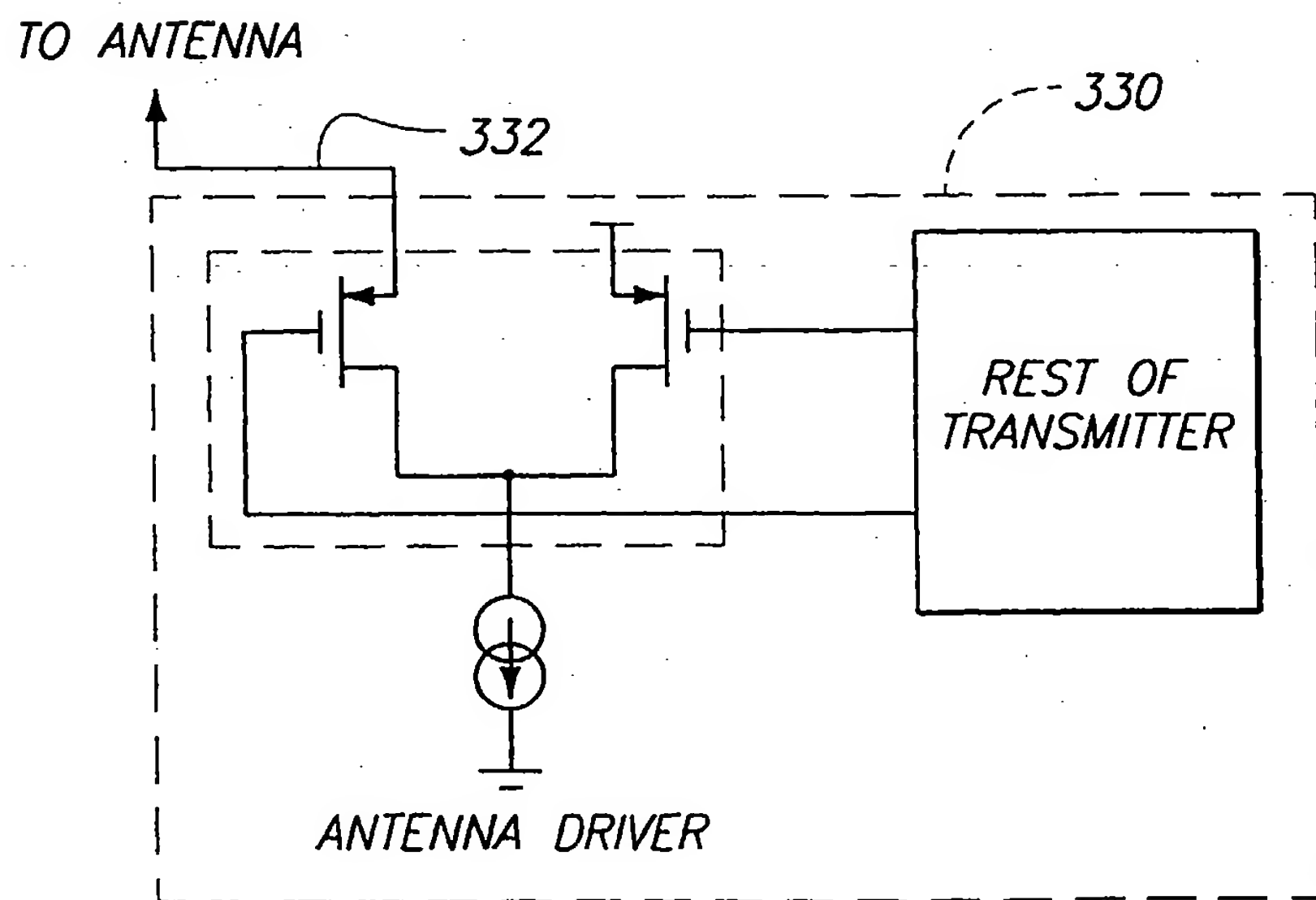
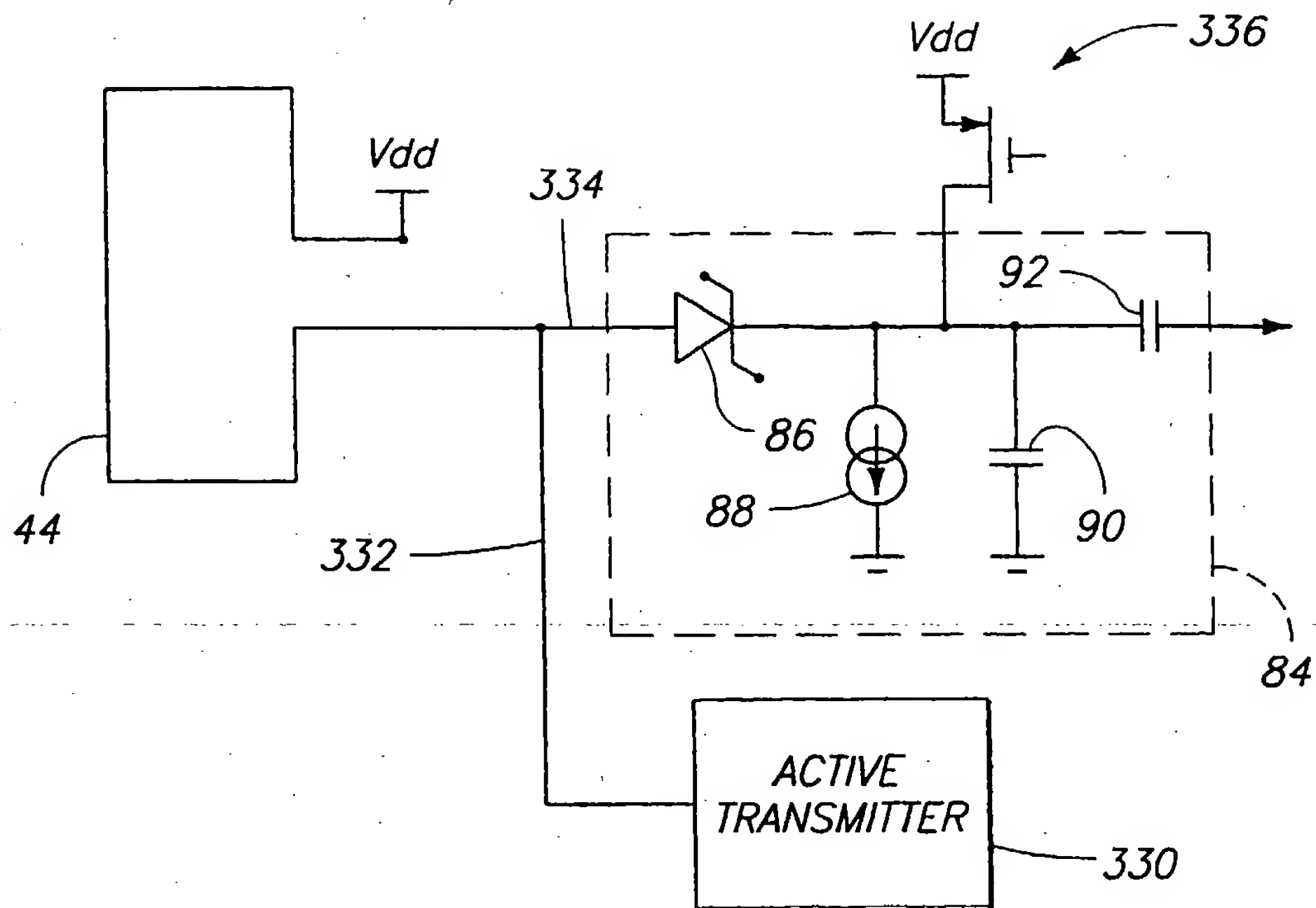


FIG. 3



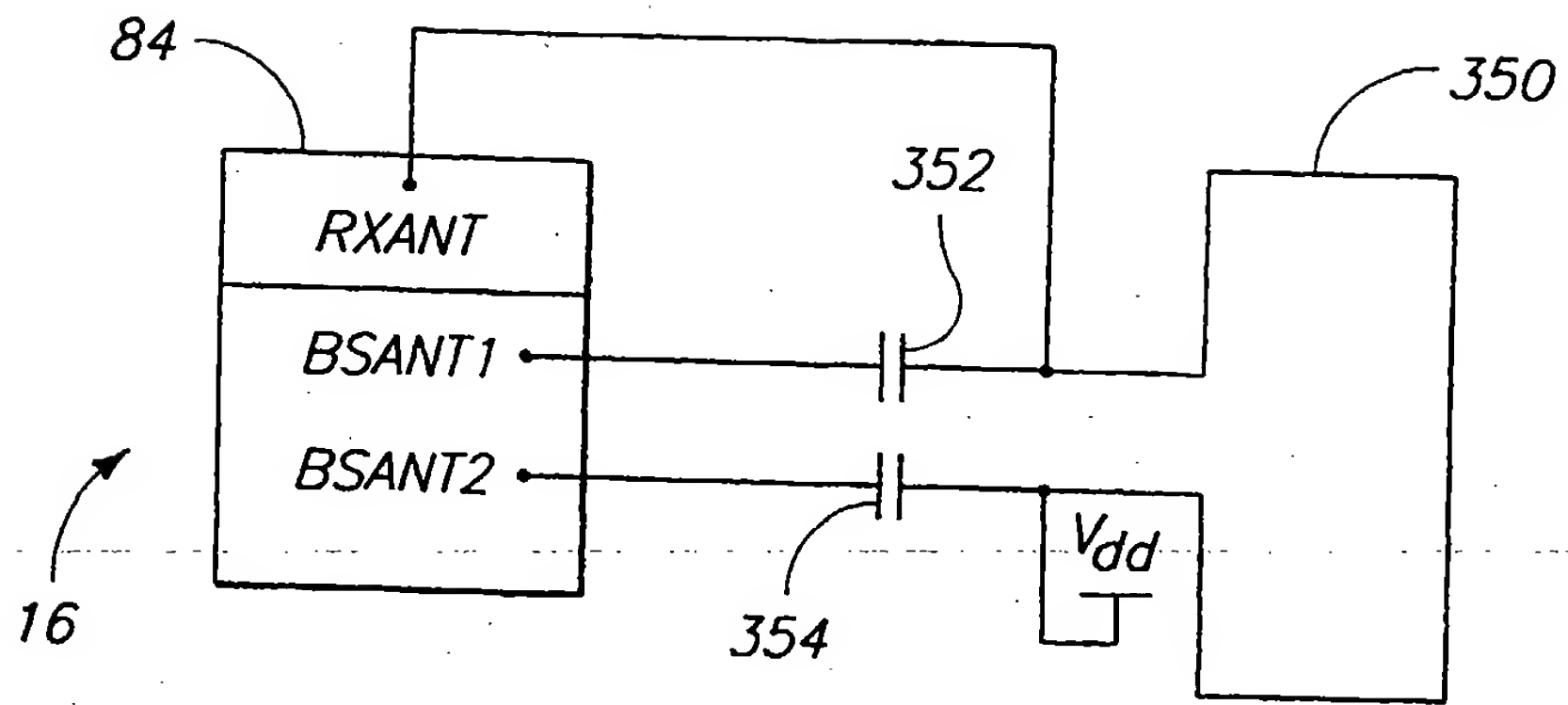


FIG. 52

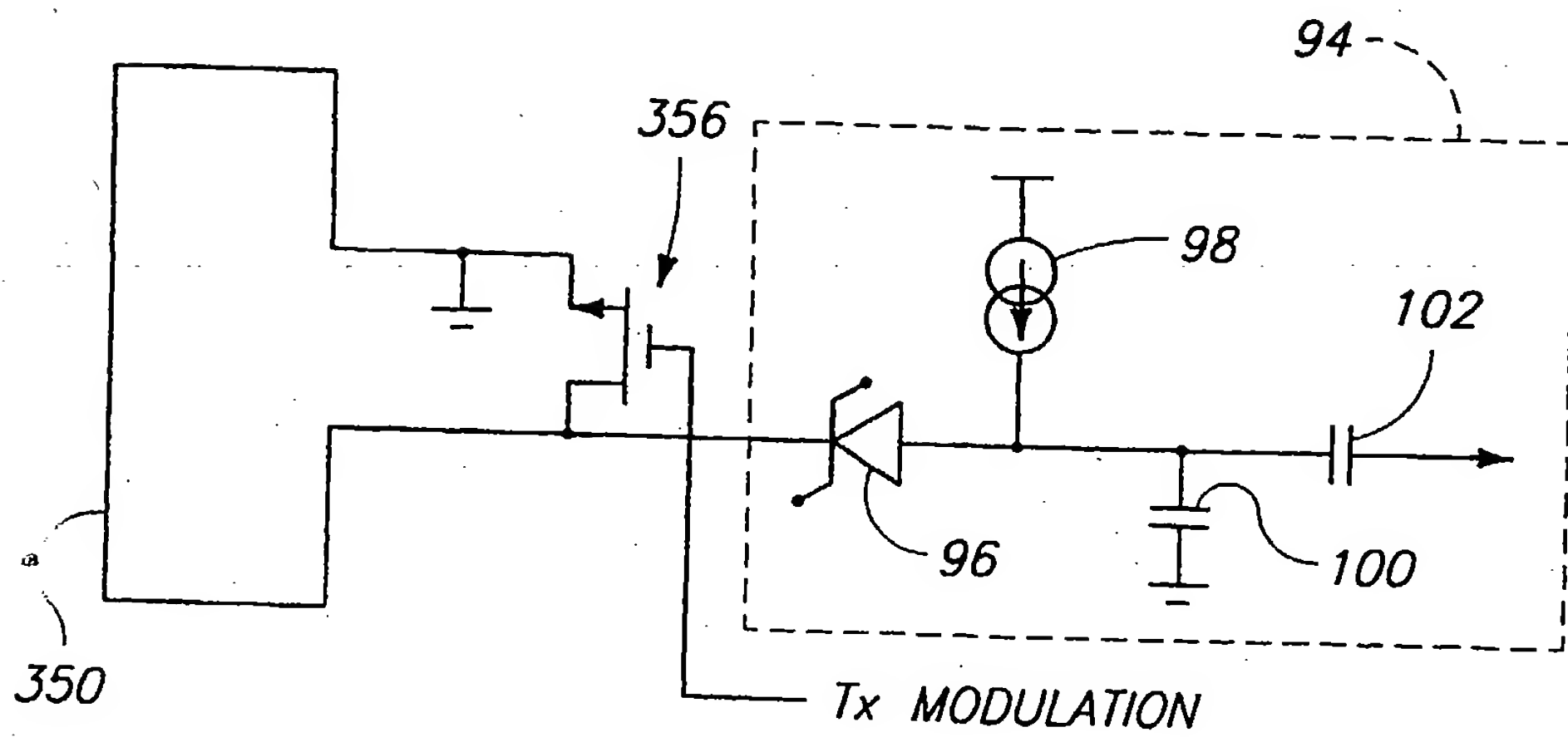
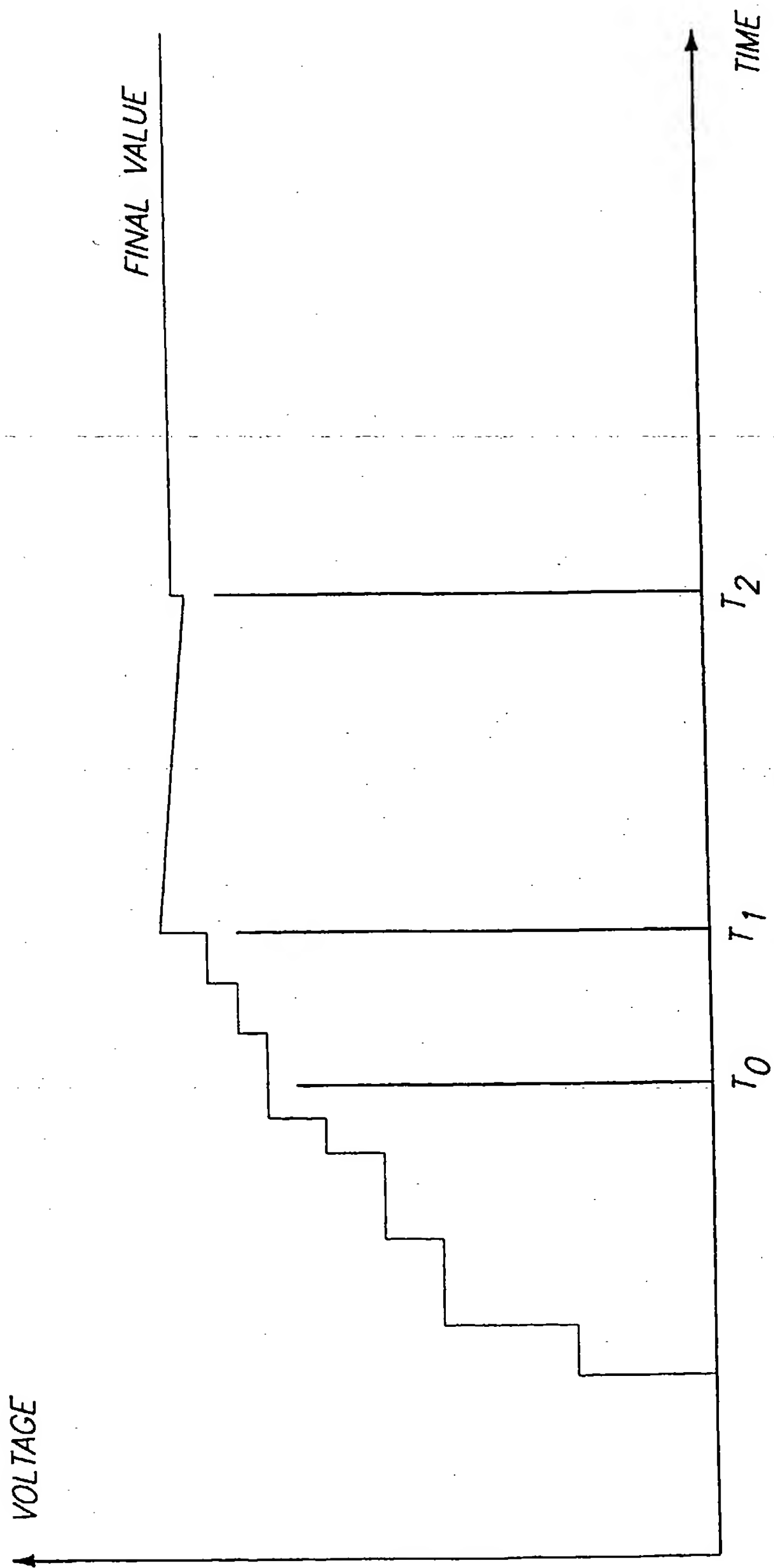
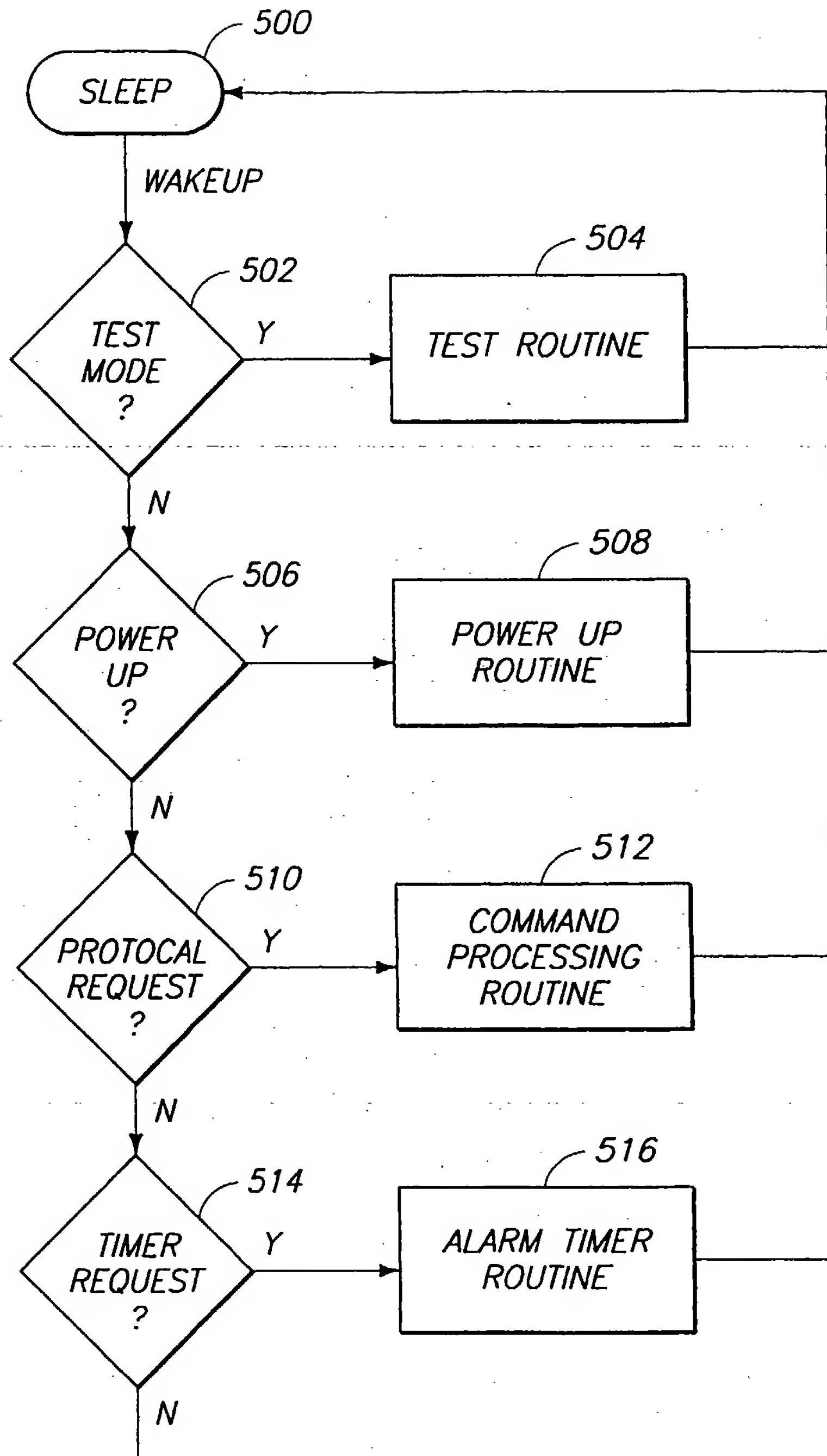


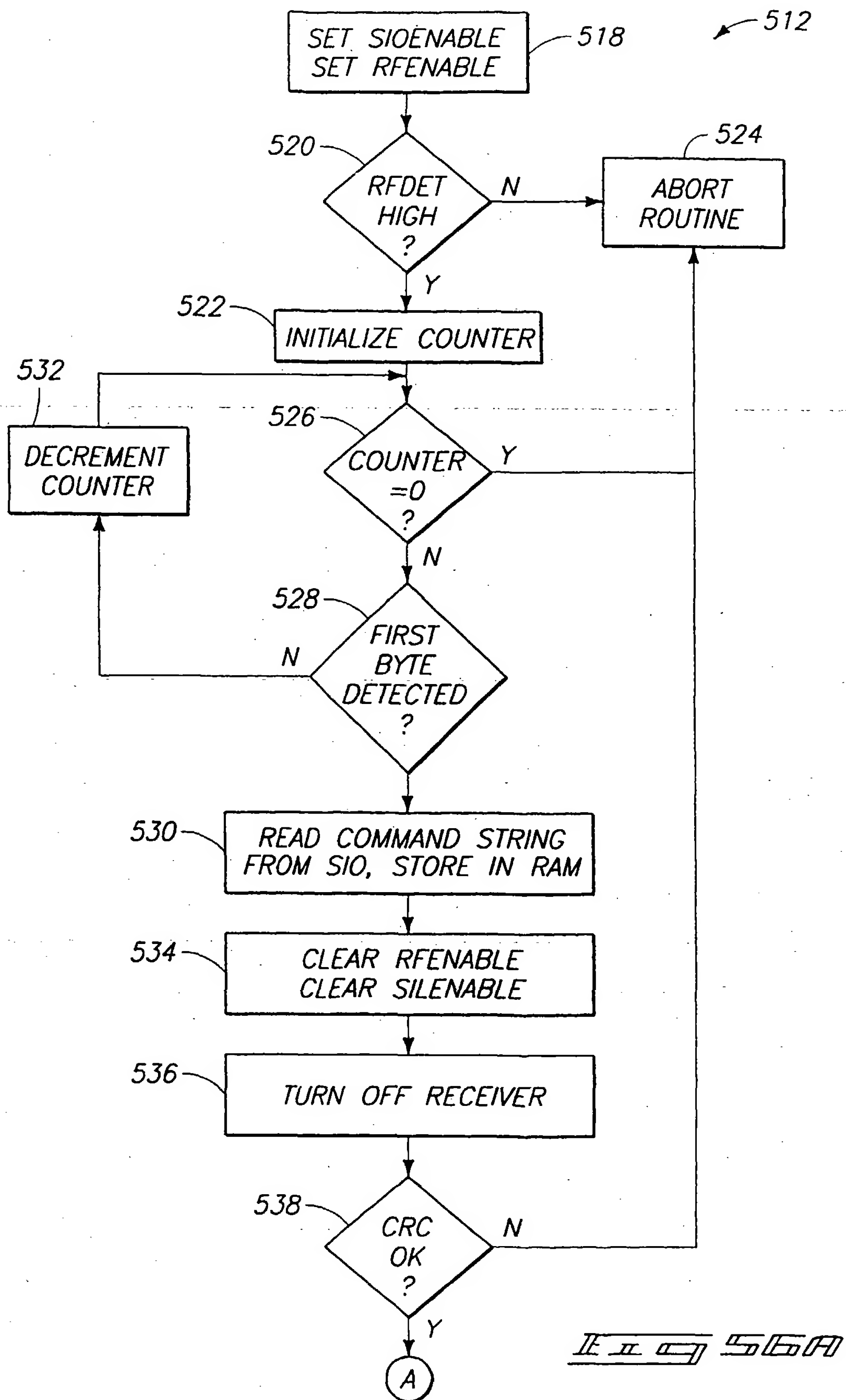
FIG. 53

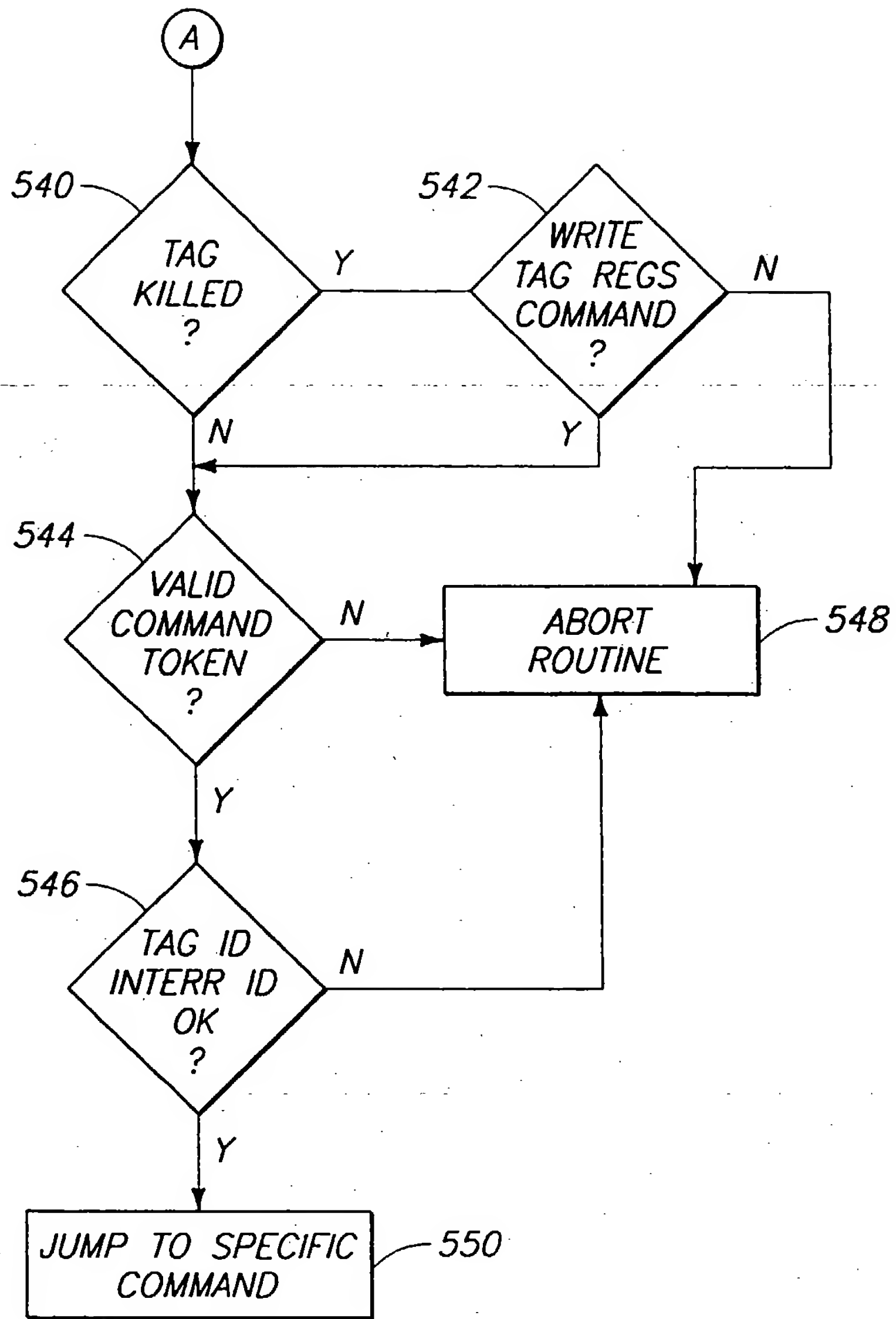


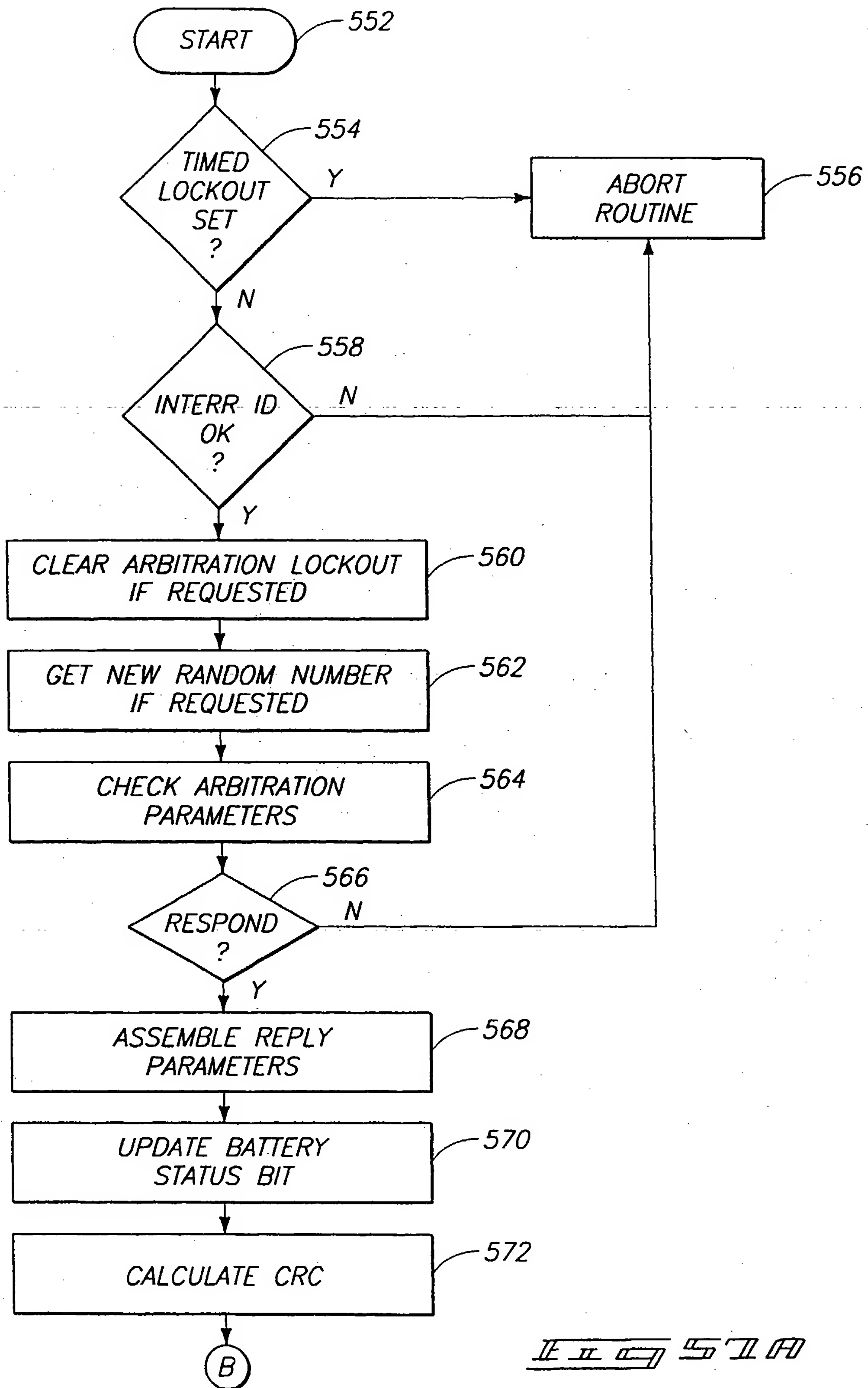
SECRET

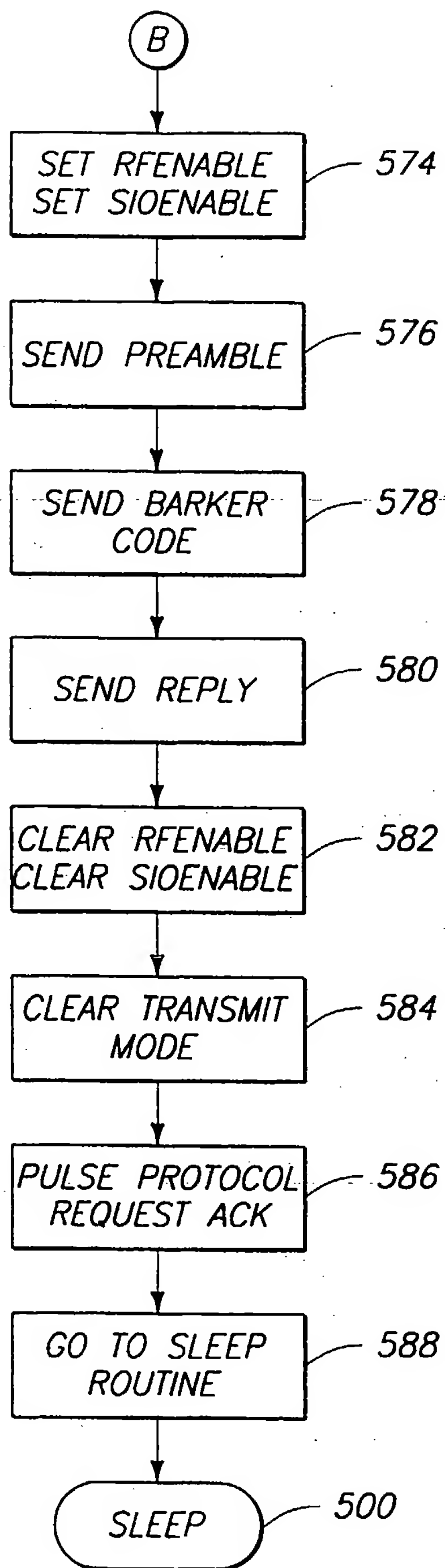


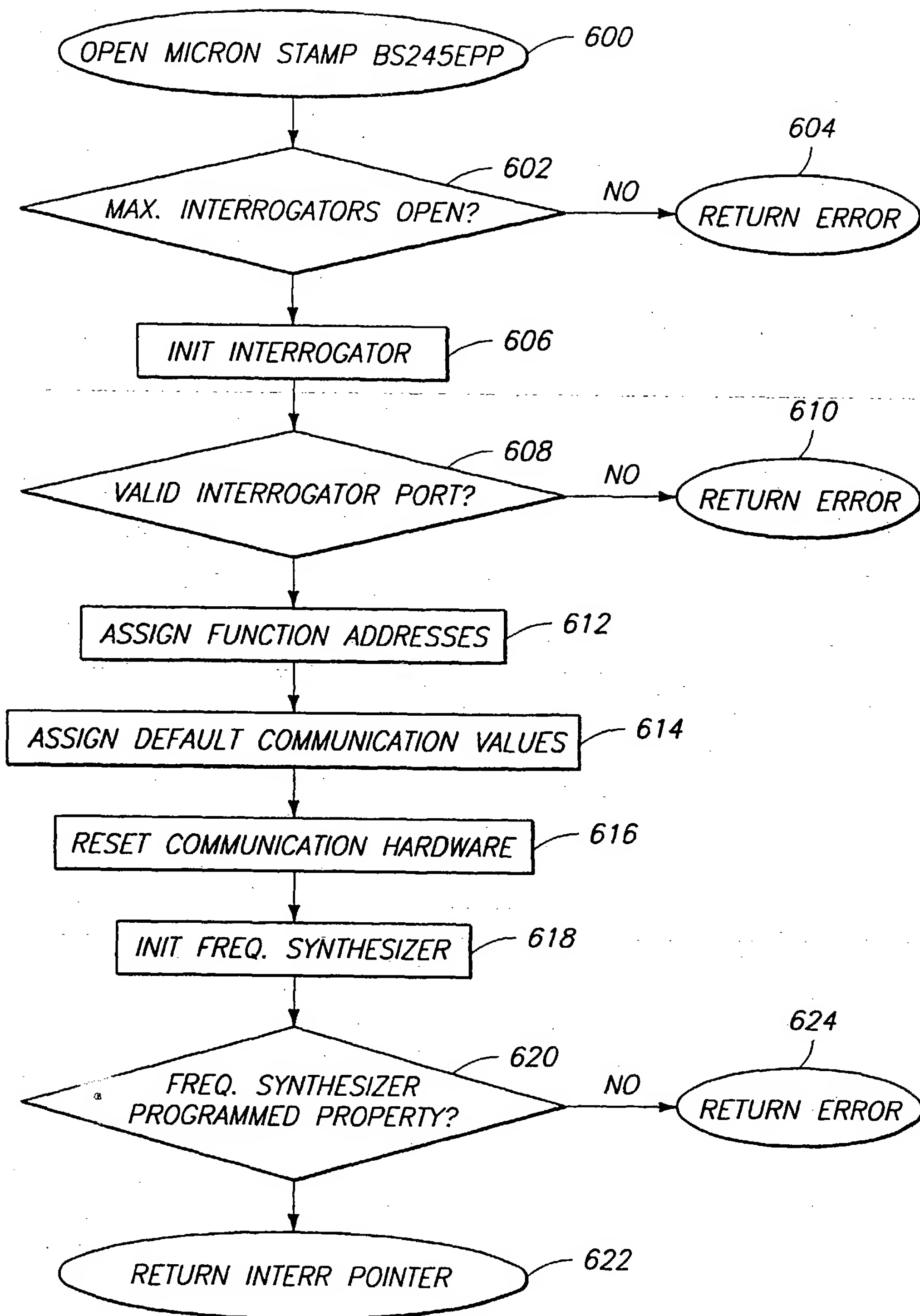


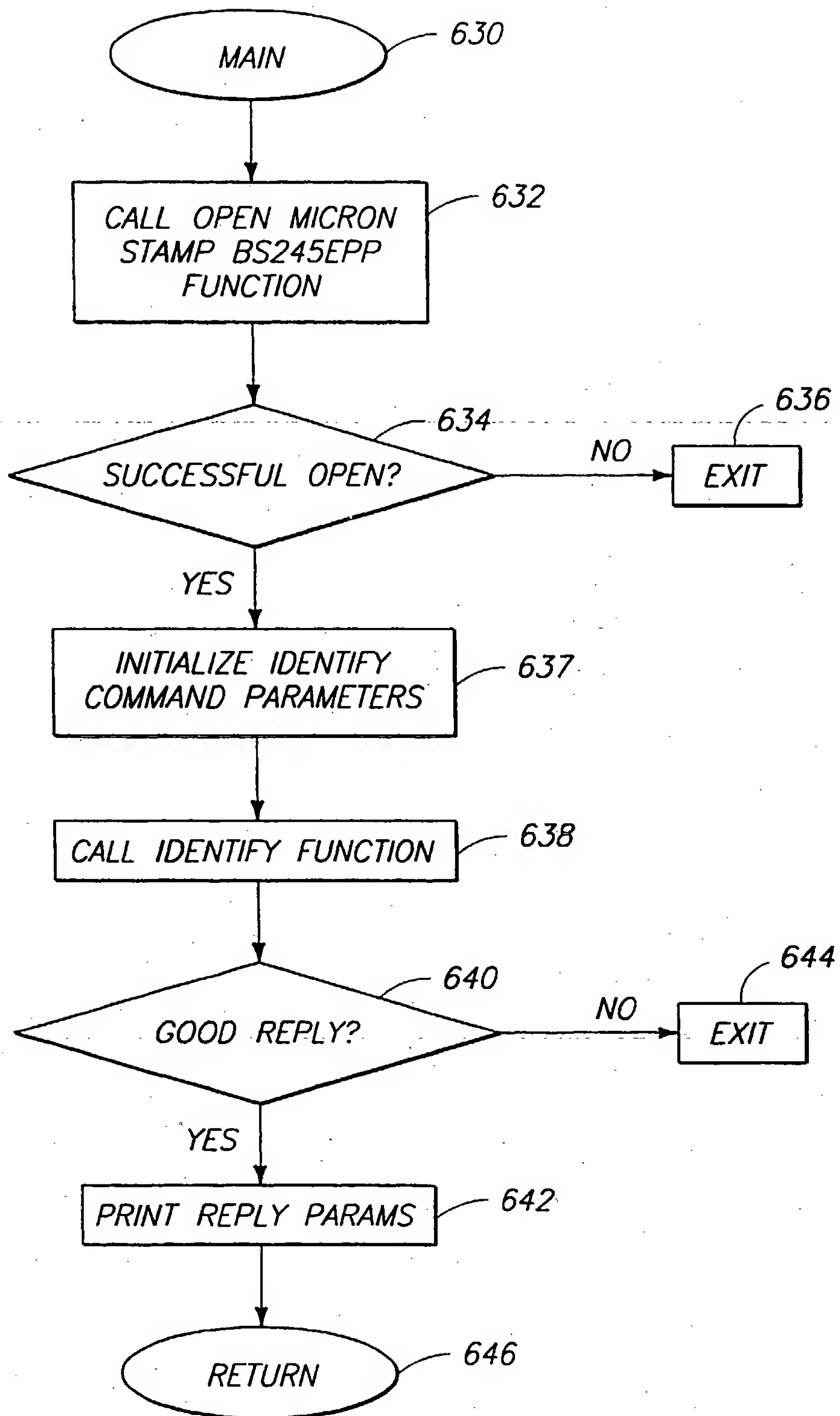


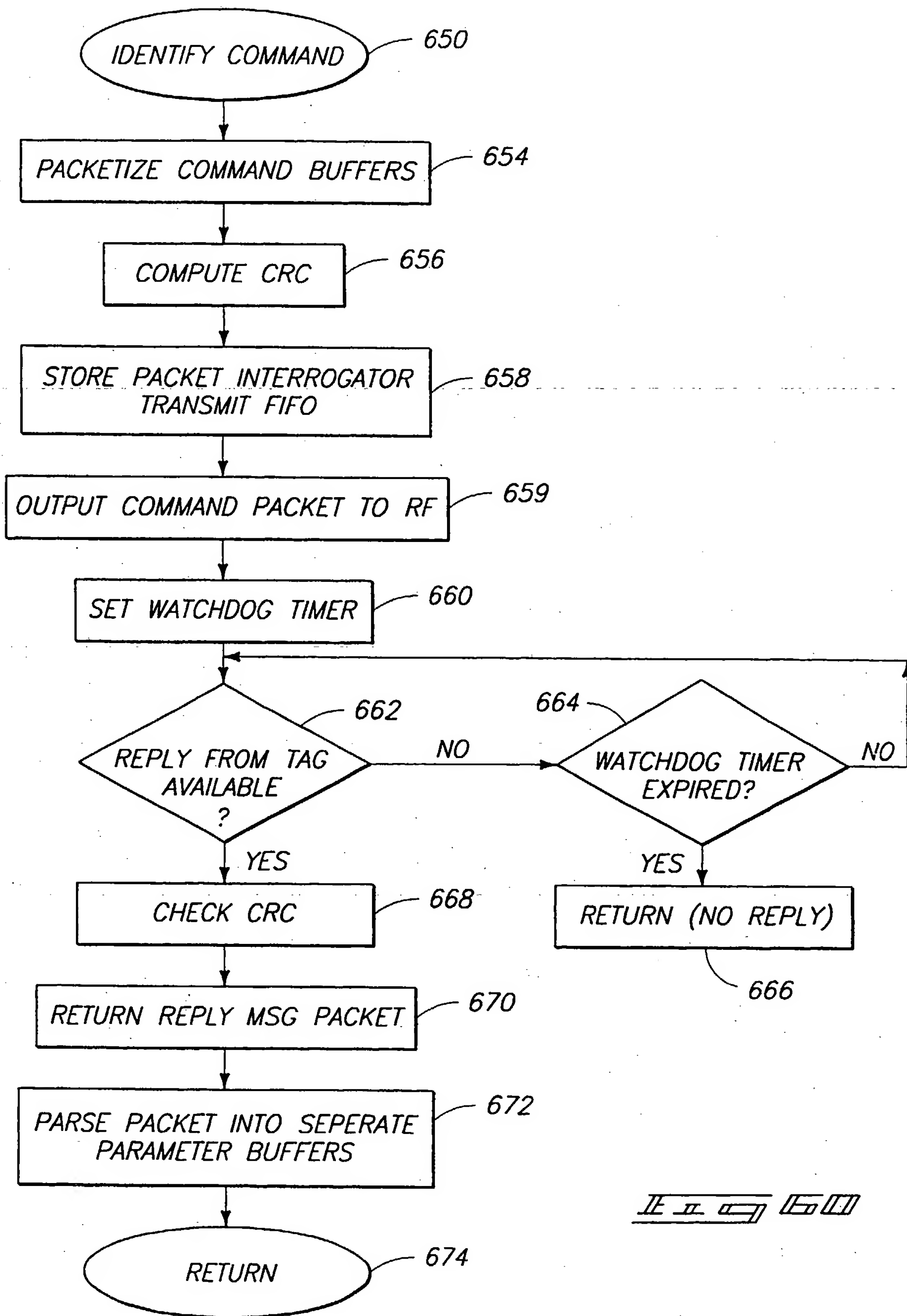


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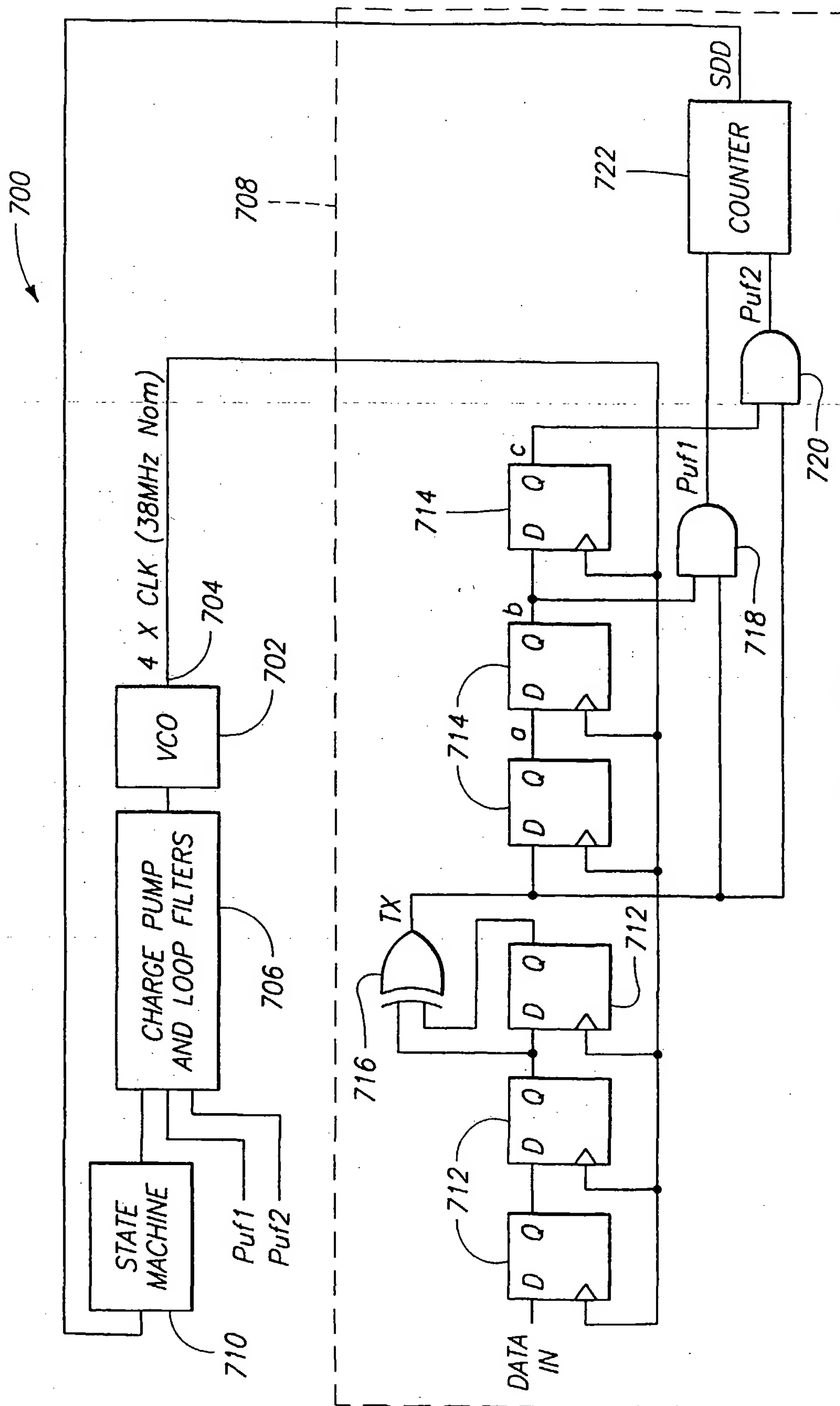


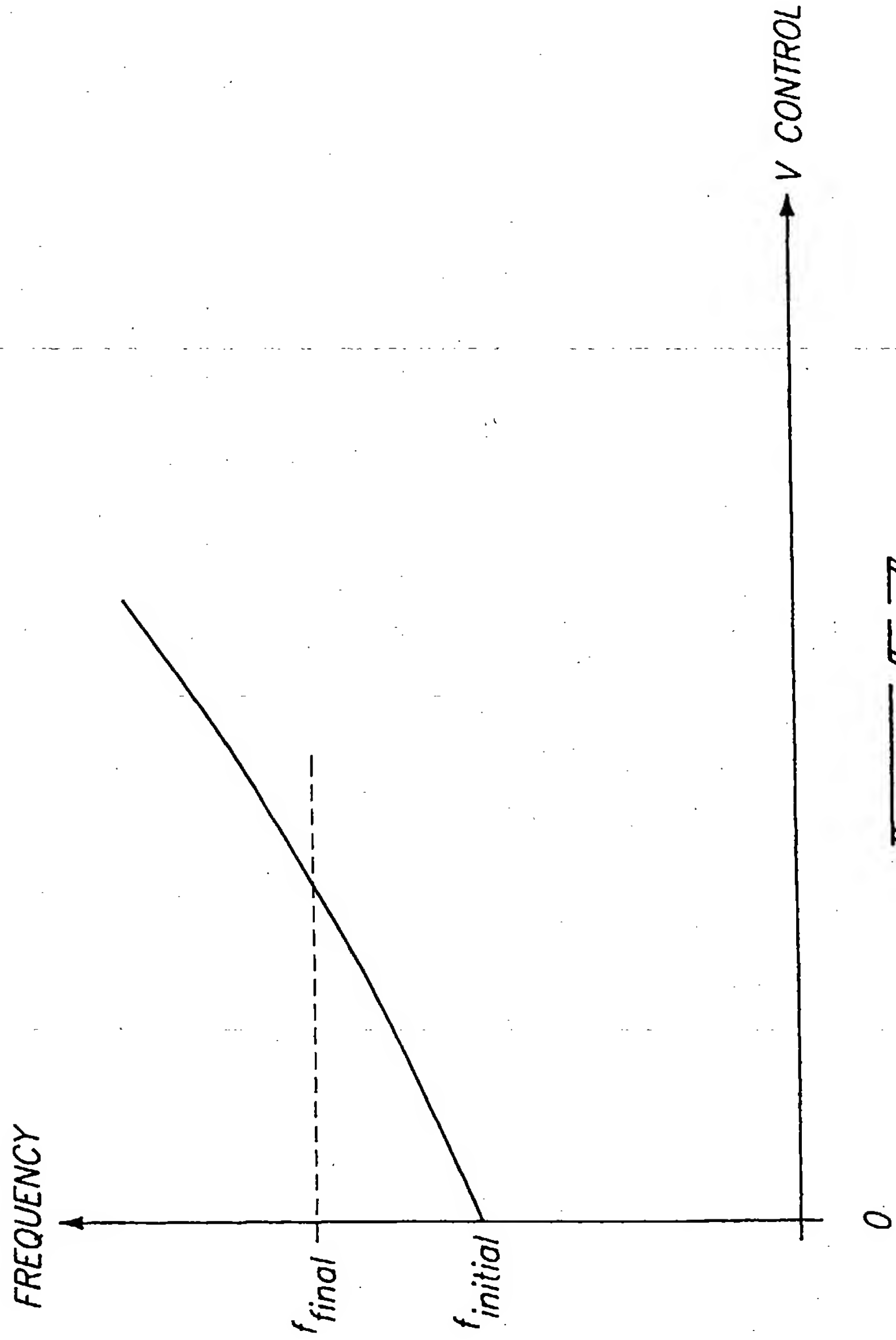




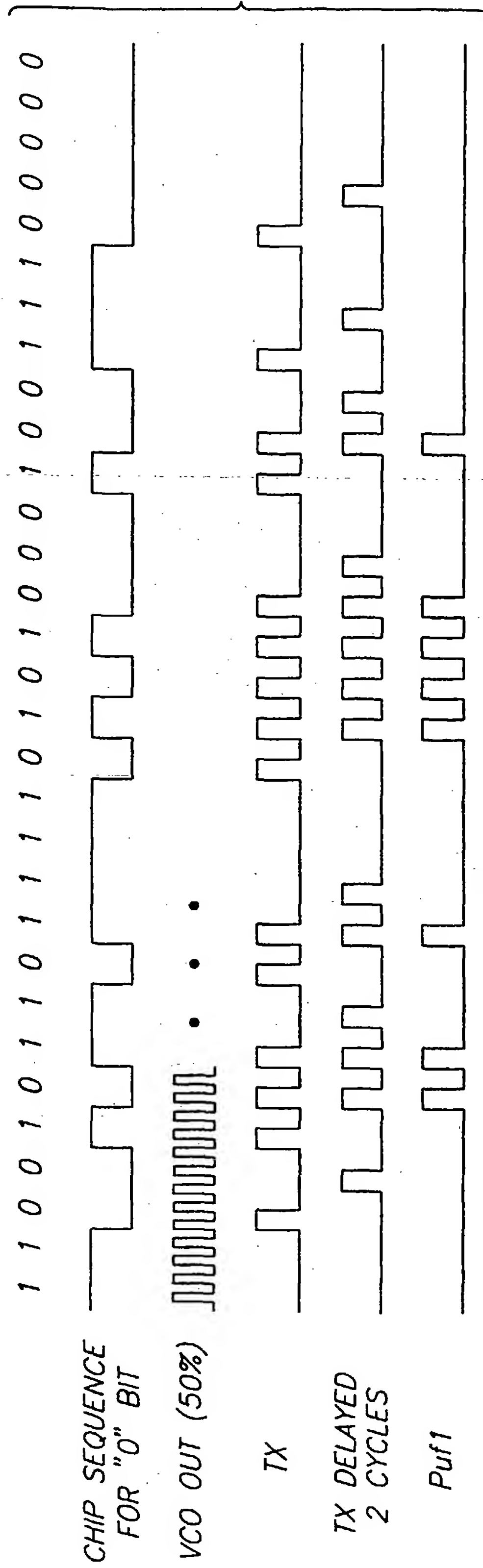
II II II II



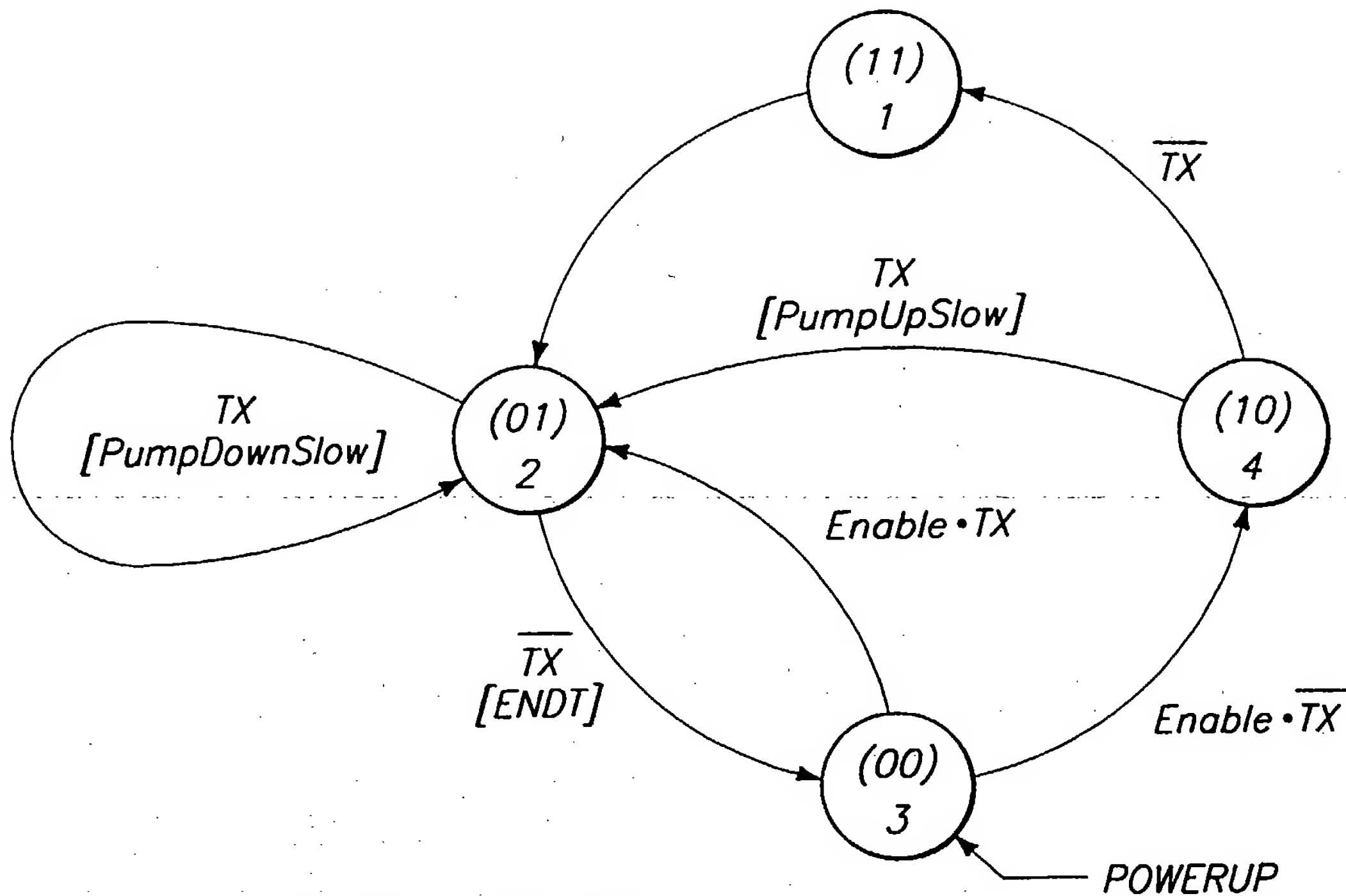




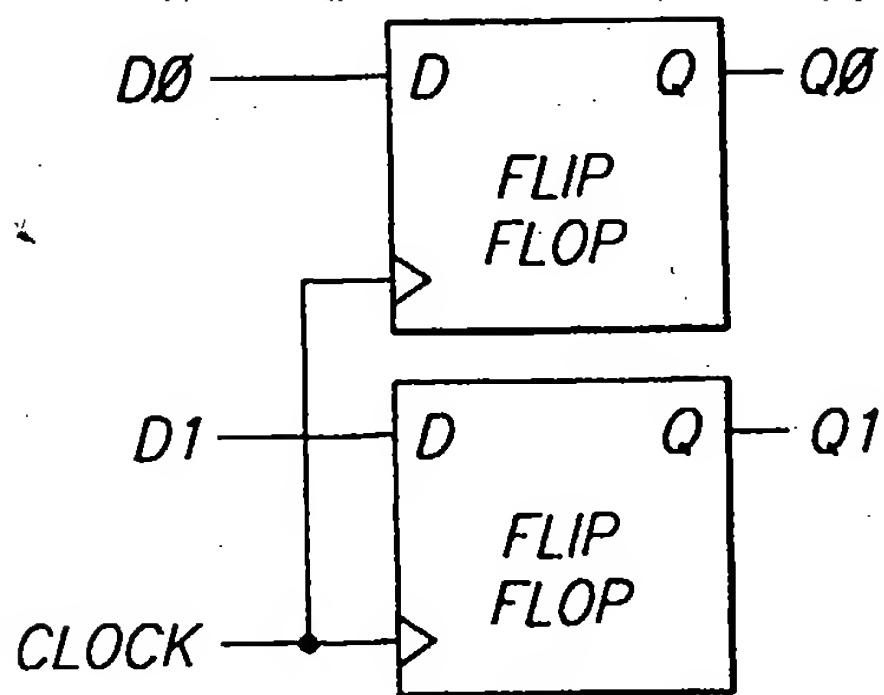
SECRET



IF  $\pi$   $\pi$   $\pi$   $\pi$



II II II II II



II II II II II

PRESENT STATE					NEXT STATE	
ENABLE	TX	Q1	Q0		D1	D0
0	0	0	0		0	0
0	1	0	0		0	0
1	0	0	0		1	0
1	1	0	0		0	1
X	0	0	1		0	0
X	1	0	1		0	1
X	X	1	1		0	1
X	0	1	0		1	1
X	1	1	0		0	1



En TX

Q1 Q0

D0:

	00	01	11	10
00	0	0	1	1
01	0	1	1	1
11	1	1	1	1
10	0	0	1	1

II II 6 7

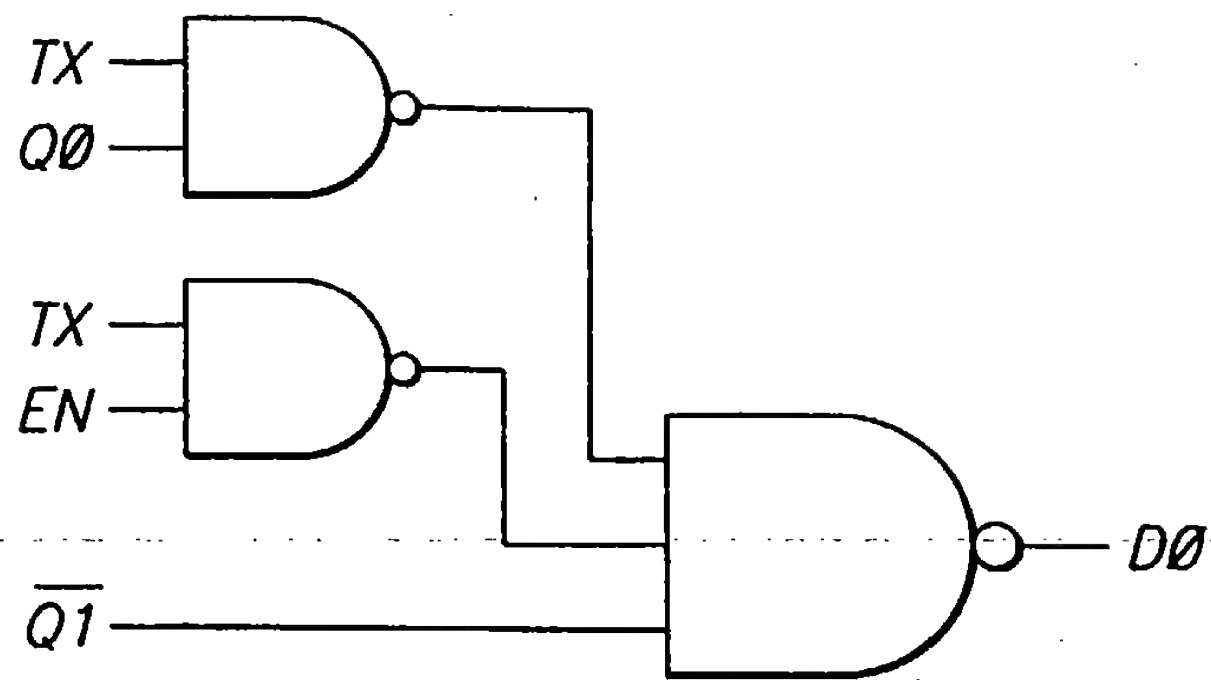
En TX

Q1 Q0

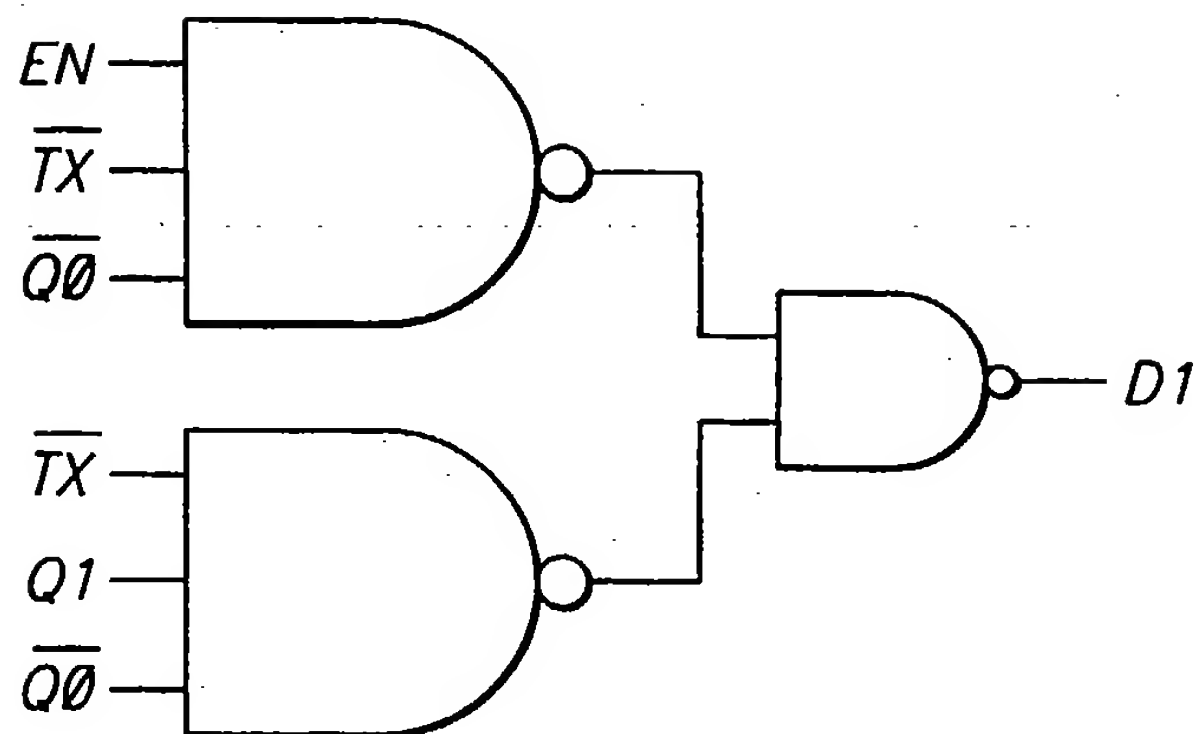
D1:

	00	01	11	10
00	0	0	0	1
01	0	0	0	0
11	0	0	0	0
10	1	0	0	1

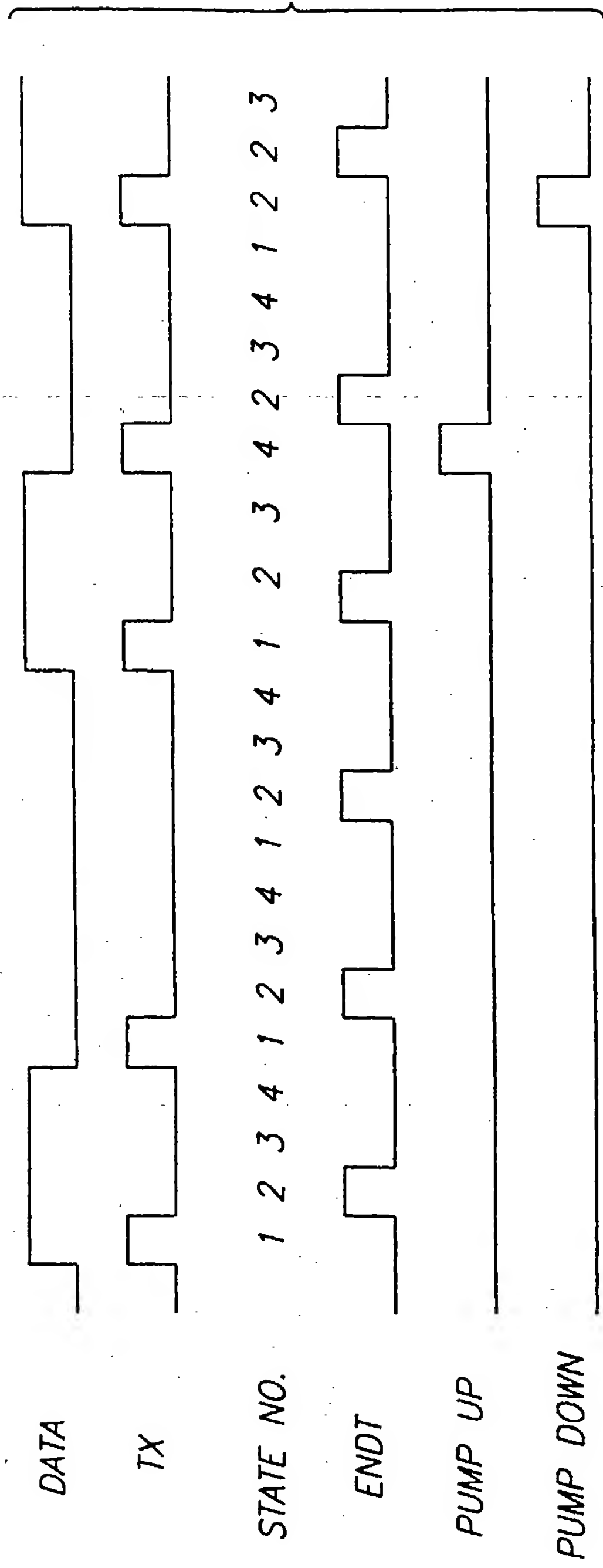
II II 6 8



II II II II II



II II II II II



II II II II



NAME	CURRENT ( $\mu$ A)	$\Delta V$ (mV)	$\Delta V/V$ CONTROL(NOM) X 100
COARSE	40	160	13.3%
MEDIUM	10	40	3.3
MEDIUM FINE	1	2.6	0.22
FINE	0.1	0.26	0.022

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